Power Quality Assessment of Solar Inverters Connected With Utility Grid/Micro-Grid

A Thesis Submitted

in Partial Fulfilment of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

by

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August, 2022

To My Parents

Declaration of Originality

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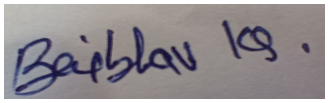
Signature 

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Certificate

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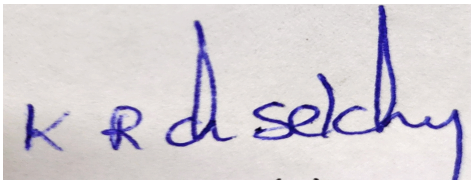

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Abstract

The Interface inverters arbitrate the network impedance based on the source characteristics for efficient solar energy harvesting. The wide impedance arbitration capability of the interface inverter defines the wide operational integrity with the AC network. In the weak grid scenario, the uncompensated grid inductance beyond PCC offers the negative damping for power oscillations at the point of common coupling (PCC) tugs the system towards instability. In this research work, the negative damping influence due to interactions between the system impedance (filter inductance and grid power injection resistance) and AC network impedance (grid inductance) on the inverter closed-loop controller is characterized by observing the natural phase deviations in real and imaginary axis. Through distinguished system's natural response, a novel second-order system impedance model is derived, and proposed current controller gain characterization aiming to achieve positive damping to mitigate the PCC's oscillations. Further tuning of the controller based on the natural response of the derived impedance model accomplishes the enhanced grid injected power quality. The efficacy of the derived system impedance model along with coherence of current controller gain is demonstrated on hardware for enhanced power quality under the stable operating region.Apart from this , a new series solar inverter configuration is proposed to share the power in terms of voltage, unlike parallel inverter configurations. In a single-stage parallel inverter, elevated DC potential and circulating current due to common-mode voltage (CMV) would degrade the solar inverter's life. The proposed topology eases the stress on the DC bus and protects the solar inverter from the issues associated with elevated DC potential (Potential induced degradation effect, switch operating voltage stress, etc.). The inherent boosting capability of the proposed series inverter with two modular inverters is demonstrated through two switching algorithms. In the first switching algorithm, the switching combinations are devised to yield the maximum voltage across the load. The second switching algorithm demonstrates the method of eliminating CMV by choosing the appropriate switching combination of two inverters. The eliminated instantaneous CMV would give the provision of operating proposed topology with common DC bus along with the flexibility of DC bus grounding. For the proposed configuration with devised switching techniques, the closed-loop controller is designed by computing the plant's equivalent characteristic impedance using a state-space model. The effectiveness of the proposed configuration, along with the closed-loop control, is validated through hardware. Also the multi boost solar inverter topologies of three variants are presented for grid connected applications. Since the proposed topologies aim to achieve higher voltage boost at AC side with reduced DC bus potential, it is required to use asynchronous switching strategies, unlike parallel inverter configurations. Although the proposed topologies are advantageous in-terms of improved reliability of solar panels and inverter modules, but instantaneous characteristic impedance imbalance due to asynchronous switching provokes circulating current within the inverter modules. Since the circulating current is undesirable concerning power quality and thermal aspects, in this research work,

the method of instantaneous impedance balance is ensured with the specially designed switching algorithm for proposed topologies. The eliminated instantaneous circulating current provide the flexibility of operating all inverter modules with the common DC bus. The proposed high gain boost configurations and switching methodologies are demonstrated on hardware prototype by pumping 2.4 kW power to the grid.

Keywords: Characteristic impedance, Circulating current, Closed loop controller modeling, Common DC Bus, Common mode voltage, Controller gains, Current THD, Distribution network, Grid-connected solar inverter, Grid impedance, Micro grid, Parallel inverter, Power quality, Reactive power compensation, series inverters, Small signal analysis, Solar inverter, Stability analysis, State space modeling , Virtual inertia, Voltage boost topology, Weak grid,

List of Publications

Patents

1. Baibhav Kumar Gupta, Amol ishwarrao Gedam and K. Ramachandra Sekhar **"suppressing circulating current through sequential switching of modular inverters in grid applications"** Application number- 202011014453, Publication number-41/2021

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Journals

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2. B. K. Gupta, K. R. Sekhar and A. I. Gedam, **"Solar Interfaced Series Inverter With Provision of Common DC Bus Grounding,"** in IEEE Transactions on Industrial Electronics, vol.69,no.4,pp.3656-3666, April 2022, doi:10.1109/TIE.2021.3073303.

3. B. K. Gupta, K. R. Sekhar and A. kumar, **"A Novel Multi Gain Single-Stage Grid-Connected Inverter With Asynchronous Switching for Intra-Inverter Circulating Current Elimination,"** in IEEE Transactions on Power Electronics, 2022, doi: 10.1109/TPEL.2022.3193566.

Conferences

1. K. R. Sekhar, B. K. Gupta and A. I. Gedam, **"The Closed Loop Controller Gain Characterization for Enhanced Current Quality in Solar Inverters Coupled with Weak Grid,"** 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA),2019,pp. 696-701, doi:10.1109/ICRERA47325.2019.8996644

2. B. K. Gupta, A. I. Gedam and K. R. Sekhar, **"A Dual Inverter Based Grid Connected Solar Power Conditioning System With Coordinated Closed Loop Control,"** 2019 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia), 2019, pp.2178-2183, doi:10.1109/ISGT-Asia.2019.8880886

3. B. K. Gupta, K. R. Sekhar and A. I. Gedam, **"Balanced Per-Phase Sequential Switching to Suppress Circulating Current in Grid Connected Modular Solar Inverters,"** 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA), 2019, pp. 686-691, doi: 10.1109/ICRERA47325.2019.8996838

4. A. I. Gedam, B. Kumar Gupta and K. R. Sekhar, **"Evaluation of DC Link Capacitor for Solar Fed Dual Inverter with Zero Sequence Elimination PWM,"** 2019 IEEE PES GTD Grand International Conference and Exposition Asia (GTD Asia), 2019, pp. 667-672, doi: 10.1109/GTDAsia.2019.8716014.

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Chapter 1

Introduction

1.1 Single Stage Grid Connected Inverter

In recent times, the single stage solar inverters as shown in are popular to interface solar farms with utility grid. The higher magnitude of energy generated by the solar farms can feed to the grid at defined frequency and voltage with different topology of three phase inverters[1]-[2]. The single-stage grid-connected solar inverters are responsible for tracking the solar farm's maximum power point (MPPT) and converting DC energy into AC at the grid frequency. In a grid-connected Inverter topology, the parallel operated modular single-stage conversion topologies are more popular because of the system capacity, modularity and efficiency. Since the DC-DC conversion stage is eliminated in the single stage conversion system, parallel connected inverter modules are fed from the same DC bus. In this configuration, it is essential to derive higher DC potential compare to conventional two stage conversion system to synthesizes the grid voltage. The higher DC potentials are synthesized in a solar farm by connecting number of solar panels in series. In high wattage solar farms, the higher DC bus potentials demand high voltage rating switching devices and DC capacitors and add substantial stress on inverter components. Since the power electronic switches and DC capacitors defines the reliability and cost of the overall system, it is necessary to protect from excess DC potentials to improve the reliability of the inverter modules. Apart from this,the importance of system impedance integrity for efficient solar energy harvesting, emphasizes the role of interface converters in stabilizing the system impedance accordance with the source and power network characteristics. The impedance arbitration conventionally achieved through interface inverter by adjusting the control parameters in accordance with the injected current patterns[3]-[4]. The limitations with the control parameters demands system stability analysis for wide range of operations. The improper arbitration of impedance due to restrictions with the control parameters invoke power oscillation at PCC, subsequently drag the system to unstable region[5]-[6]. Therefore the issues associated with solar interfaced grid connected inverter

1. Power quality issues in the weak grid scenario due to uncompensated grid inductance after the point of common coupling (PCC).
2. Elevated DC bus potential and its grounding
3. Inter and intra Circulating currents within the inverter modules.

need to be resolved to inject smooth grid power.

1.1.1 Power Quality Issues in Weak Grid Coupled Solar Inverter

In a weak grid scenario, the additional grid impedance further deteriorates stability margins due to offered negative damping to frequencies vicinity to synchronous frequency arises as a consequence of complex interactions between the system control parameters and network impedance [7]-[8]. The frequency oscillations at the PCC distort the reference to the inverter taken through PLL. In general, the synchronous reference frame based PLLs are more popularly used for generating robust reference by shaping the dq-impedance of the inverter[9]. In the past, the researchers have explored PLL dynamics under weak grid scenario along with the control parameters[10]-[11]. Based on the past study, it has been identified that the PLL would bring the negative resistance in the sub synchronous frequency band under weak grid scenario further worsen the stability margins of the system. The influential negative resistance mechanism introduced by the PLL on the system instability is presented comprehensively in [12]-[11]. Further , the self-synchronous phenomenon of grid impedance impact on system stability margins is studied by introducing the non linear PLL model[13]. However, the increased complexity of the current controller with non linear models forced the researchers to reconsider linear PLL models only, reiterated the negative resistance due to reshaping of inverter dq-axis impedance. To overcome the negative resistance at sub-synchronous frequencies, the researchers have introduced the band pass filters to compensate the negative effect with compromised bandwidth[14]. The limited bandwidth of the PLL restrict the current controller significance in dynamic reference tracking and noise rejection. The dynamic response further compromised with defined stability margins of current controller due to cascaded effect[15] & [16]. In [16], the method of introducing the PLL dynamics into the current controller is demonstrated to avoid undesirable interactions of the PLL with the current controller. The additional phase shift with introduced filters in PLL deteriorate the control dynamics of the overall system. The deteriorated dynamic response and additional phase shift significantly impact the system during fault ride through conditions [17]. Considering the trade off with PLL impedance shaping and dynamic response, the researchers have investigated various control methodologies including outer voltage loop control addition [18]-[19],ac-bus voltage controller[20],impedance phase compensation[21] etc without disturbing the PLL gain. These methods are mainly designed to address the frequency oscillations at PCC demanded additional control loops and complex algorithms to address the stability margin, diminishes the role of current controller significantly. Since the current controller parameters effect on the stability margins are not established completely yet, the external loop shaping methods along with the current controller gain compensation got prominence. It is mainly due to unexplored system impedance interaction model that mimicks the actual behaviour of the system under weak grid scenario. But with the accurate system model, external loop shaping methods can be eliminated completely. In this direction, attempts are made to study the system model in weak grid scenario through state space and nyquist impedance based modeling, but with limited parameters[22]. Further, impedance based models are studied using

lumped equivalent circuit to analyse the system stability but the influence of control and circuit parameters are neglected. In [23], a simplified model for the plant or the controller is presented but it makes the system stability analysis cumbersome while realizing the effect of simultaneous variations in the control and plant parameters. In [24], researchers have modelled the interface converter based on positive and negative sequence impedance directly in phase domain and studied independently for stability analysis under single-input single-output system. But this method is not appropriate for wide range grid inductance variations. In literature[22]-[24] it has been identified that the system stability not necessary improved with reduced grid inductance but influenced by both X/R ratio and the grid inductance. The established works so far, described the 'R' with reference to network line resistance. But not explored the influence with reference to grid power injection resistance (V_g/i_g). Further, in the literature it has been identified that the inductance of either side of feedback point influences the system stability but the effect of power injection resistance is not considered to evaluate the stability margins. The work reported in this paper, built around deriving the positive damping for the PCC oscillations through a thorough assessment of system natural response in weak grid scenario. The natural response of the system is influenced by control parameters, impedance of system and their interactions. In stiff grid scenario, the system impedance are compensated to model the controller gains for desired injected power characteristic. Whereas in weak grid scenario, the influence of network impedance need to be assessed in the presence of system impedance to model the controller gains. The interaction between the system impedance (filter inductance and grid injected power resistance), network impedance (grid inductance) and controller gains requires multi dimensional assessment forced past researcher to derive the simplified models. Since the derived existing models are not exactly mimicking the weak grid scenario, it is required to use a secondary controls (PLL shaping, feed-forward damping, additional hardware etc) along with the current controller gain compensation for grid injected current quality shaping [7]-[25]. But with appropriate modeling of weak grid scenario, the current controller gain compensation is sufficient to bring the positive damping to power oscillations at PCC.

1.1.2 Elevated DC Bus Potential and Circulating Current Issues

At present, modular inverters are dominating in the solar interface inverter portfolio, mostly parallel configurations. The modular single-stage parallel inverter is well known for sharing power in terms of current. In a parallel configuration, the DC bus voltage requirement to synthesize the desired AC voltage demanded to connect with utility grid is high, typically 1000 V [26]. Along with elevated DC bus voltages, the parallel inverters are also suffering from the need for operating DC bus in floating condition due to CMV present in the inverter circuit. In parallel inverter topology, all modular inverters are assumed to be identical characteristic impedance and operate with the same switching instances to connect all inverter modules to the same DC bus. But it is improbable that the modular inverters operating in parallel configuration have an identical characteristic

impedance resulting in circulating current [27]-[28] within the inverter modules due to CMV. In parallel configurations, the circulating currents are classified as intra-modular (within the inverter modules) and the inter network (DC-AC) circulating currents. The intra-modular circulating currents result from instantaneous voltage between the AC network (load star-point) and the DC reference point that appear due to instantaneous impedance mismatch. The researchers have identified the impedance mismatch in parallel configuration mainly due to control signal propagation delays and maximum power point impedance variations correspond to solar irradiance. Since the circulating currents affects the grid injected power quality, the researchers have investigated various methods including augmented impedance in zero sequence path and customized control technique to reduce the circulating current.Many researchers have attempted to suppress the circulating current through isolation, introducing a high impedance path in the circuit, and synchronized control in the recent past. In isolation method [29]-[30], the DC bus is isolated from AC bus through a three-phase transformer but increases the system's size and cost. Further researchers have tried to introduce a high impedance path in the circuit through coupled inductor [31]-[32] to reduce the circulating current. Achieved a high impedance path through a coupled inductor can restrict high frequency circulating currents effectively. Whereas the suppression of low-frequency component can be achieved by different control and modulation techniques like a hybrid or modified space vector PWM [33]-[34], selective harmonic PWM [35], multi-carrier PWM method [36]-[37]. To reduce the circulating current provoked due to switching delays, the past researchers have proposed various synchronized control approaches like PI controller for master-slave configuration [38], decentralized controllers, Deadbeat control [39]-[40], zero vector feedforward control [41]. The synchronized approach treats all modular inverters as a single inverter and control all modular units through high frequency bandwidth communication link to achieve the synchronized switching [38]-[41]. The attempts made so far to reduce the circulating currents demands either extra hardware circuitry or complex control algorithm, despite complete elimination of circulating current is not possible. Apart from the intra-modular circulating currents, the inter network circulating current arises mainly due to adopted grounding methods with AC and DC networks. In any distribution power network, the star point of the AC three phase winding is connected to ground to derive the neutral wire of the power network. With grounded AC network, the DC of the interface inverters need to be isolated from the ground to avoid the virtual zero sequence current path between AC and DC networks in case of transformer less configuration. Otherwise galvanic isolation need to be maintained between AC and DC network through transformer to suppress the zero sequence current path. Even with the transformer, the solid DC bus grounding is not advisable considering the circulating currents between the inverter modules and the ground resistivity between AC and DC network. Therefore the industries are preferring either impedance grounding or reducing the the voltage magnitudes correspond to the circulating currents through devoted inverter topologies . Although the impedance grounding address the safety requirements partially,

but considering the reliability of the system, the solid DC grounding is recommended by eliminating circulating currents.

Apart from the instantaneous impedance of the circuit, the DC bus potentials also influences the magnitudes of the circulating current [42]-[43]. The elevated DC bus potentials in the single stage parallel inverter topologies not only deteriorates the performance of the inverter modules but also aggravate the reliability issues of the solar panels due to potential induced degradation(PID) effect [44]-[45]. In a parallel inverter, the DC potentials generated through series solar strings with grounded frames experience a significant voltage buildup across each solar cell. Depending upon the potential buildup across the cell, the leakage current flowing through grounded frames damages the solar cell, overall, affects the reliability of the solar panels. As per the available literature, the PID effect can be minimized by reducing the DC potentials or with appropriate grounding of DC bus [44]. In solar inverters, various methods of DC bus grounding are proposed through cascaded boundary dead beat control [46], isolated AC-DC conversion unit with specialized control unit [45], and zero sequence damping [47]. So far, the proposed methods required extra hardware circuitry to mimic the virtual grounding across the DC bus of the solar inverter. Apart from this, the past study shows that the DC bus's potentials affect the performance of the DC capacitors and the semiconductor switches. To reduce the DC voltage and common mode stress on the DC capacitors/switches, researchers have proposed various methods, including Multilevel inverter [48], current source inverters [49], etc. Owing these issues, the researchers have studied the series injection topologies based on the dual inverter configuration as a grid interface inverters for adopting unique feature of deriving the AC voltage with reduced DC bus potential[50]-[51]. In the motor drive applications, the researchers have concentrated on addressing the motor applications' issues like minimization of bearing current[52], improving motor torque ripple performance[53], etc. In motor applications, the neutral point of the load is floating. In the power network case, the neutral point of the load needs to be grounded, making the circulating current analysis different from the motor applications. Besides, the existing CMV and neutral grounding demand the solar inverter to operate with a floating DC bus that affects the life of solar panels and inverter. Overall, the higher DC bus voltage and the CMV degrade the performance of modular solar interface converters. Although with dual inverter configurations, the voltage responsible for the circulating current can be reduced along with DC bus voltage, but the impedance imbalance arises due to asynchronous switching may worsen the frequency of the circulating current. But the offered degree of freedom with redundant switching states in series injection configurations ensures the desired characteristic realization. In literature, the selection of switching states for dual inverter to realize the grid voltage is demonstrated through coordinated closed loop control[54],sliding mode control [55] etc. Although with the appropriate switching state selection, the series injection with dual inverter requires only half of the DC bus voltage compare to parallel inverter topology to generate the grid voltage, but suffer from the circulating current within the inverter

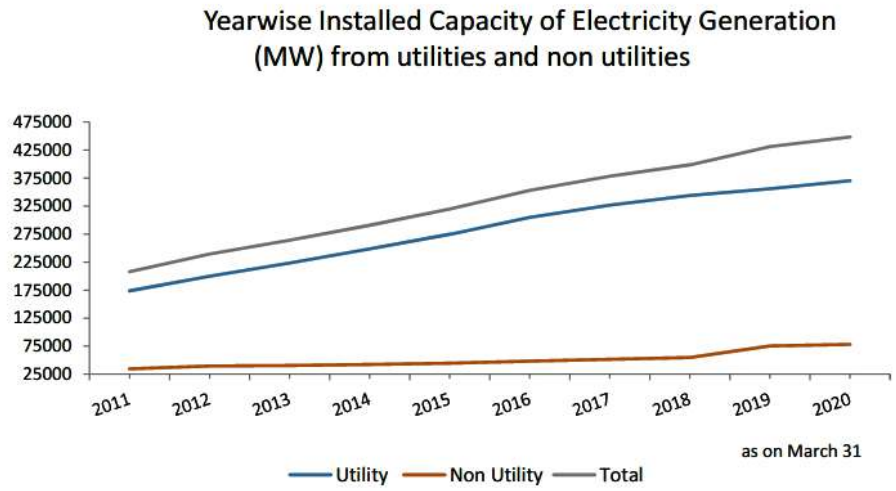
module demands isolated DC bus for both the inverter [56].The circulating currents are mainly due to the resultant voltage between the DC capacitor midpoint and the ground restricting the DC bus grounding. In a dual inverter configuration, the instantaneous voltage between the two inverter's DC negative bus, known as common-mode voltages (CMV), forces the circulating current within the circuit when two inverters connect with the common DC bus. The instantaneous circulating currents are the consequence of CMV arises due to three-phase inverter switching, enforce the zero-sequence harmonic currents circulates within the two inverters in a series inverter configurations. These circulating harmonic currents create a thermal runaway issue in semiconductor switches and the transformer connected for voltage sharing that negatively influences the long-term reliability of the inverter circuit. Considering thermal runaway issues, it is recommended to eliminate the circulating current or use the isolated DC bus for the individual inverter. But, in case of the dual-inverter configuration with isolated DC bus is inefficient due to poor yielding of energy at partial irradiance condition and demands the coordinated control algorithm to access the maximum power across the inverters. To address the problems associated with isolated DC bus, the recent work reported in [56]- [57] demonstrated the selection of switching states of dual inverter to cancel the instantaneous circulating current to employ the common DC bus for both the inverters present in series injection topology but with reduced voltage gain. The concept of instantaneous impedance balance can be further explored to realize the high gain voltage topologies considering the associated technological features like

- Reduced demanded DC potential to realize the grid voltages: Improve the power efficiency of the interface inverter, improve the solar inverter module reliability[58].
- Operate with common DC bus: provide the ease in control to balance the extracted power for wide range of irradiance [56] - [57].
- Provision of DC bus solid grounding : Improve the reliability of the solar panels through reduced PID effect & ensure the strict compliance with safety standards [59]-[60].

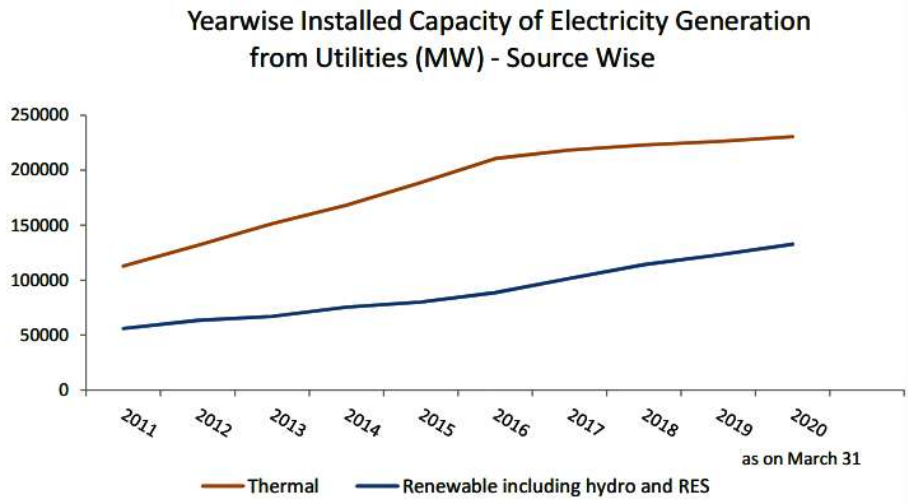
1.2 Motivation

1.2.1 Year-Wise Installed Capacity of Energy Generation in India

As it is shown in Fig.1.1a [61], India's energy requirement is steeply rising from 2011 to 2020. Whereas in generation, the thermal generation captures the maximum share from 2011 to 2020, but the thermal generation curve gets flattened from 2016 to 2020 due to increased generation through renewable sources as it is visible from Fig.1.1b. From Fig.1.2a and Fig.1.2b, it is evident that nation is moving toward renewable energy generation, and the preferably towards the solar due to its abundance and cleanness. On the other hand, Government of India has launched many initiatives to promote clean energy generation, as listed in sub-section 1.2.2 [62].



(a) Year-wise installed capacity of electricity generation in MW (X-axis: Year; Y-axis: Electricity generation in MW)



(b) Year-wise and source-wise installed capacity of electricity generation in MW (X-axis: Year ; Y-axis: Electricity generation in MW)

Figure 1.1: Installed capacity of electricity generation in MW

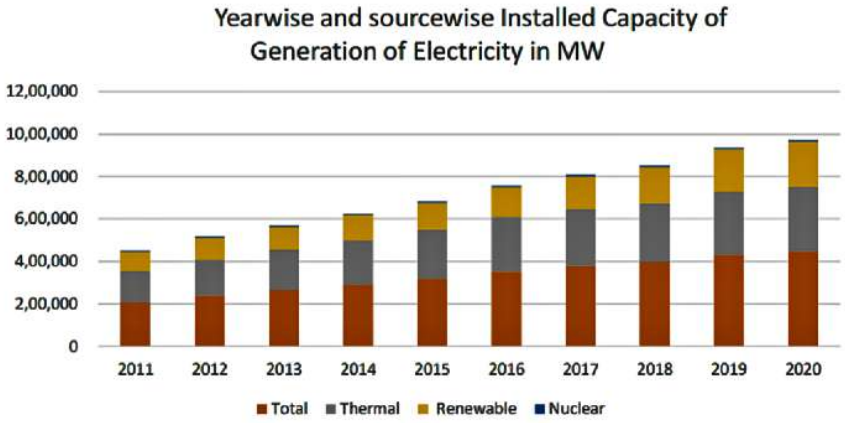
1.2.2 Government Initiatives to Promote Clean Energy Generation

1. Pradhan Mantri kisan Urja Suraksha evam Utthaan Mahabhiyan (PM-KUSUM) scheme for solar pumps where government of India (GoI) has targeted to setup 10,000 MW of decentralized Grid Connected Renewable Energy Power Plants on barren land. GoI planned to install 17.50 Lakh stand-alone solar agriculture pumps and solarisation of 10 Lakh agricultural pumps connected with the grid.

2. Ude Desh ka Aam Nagarik (UDAN) scheme for Airport runway lighting system, Solar integrated technologies for railways and Battery charging station.

3. Deen Dayal Upadhyaya Gram Jyoti Yojana (DDUGJY) for Rural electrification and providing Micro-grid solutions to rural and hilly areas.

4. FAME(Faster Adoption and Manufacturing of Electric Vehicles) to give the boost



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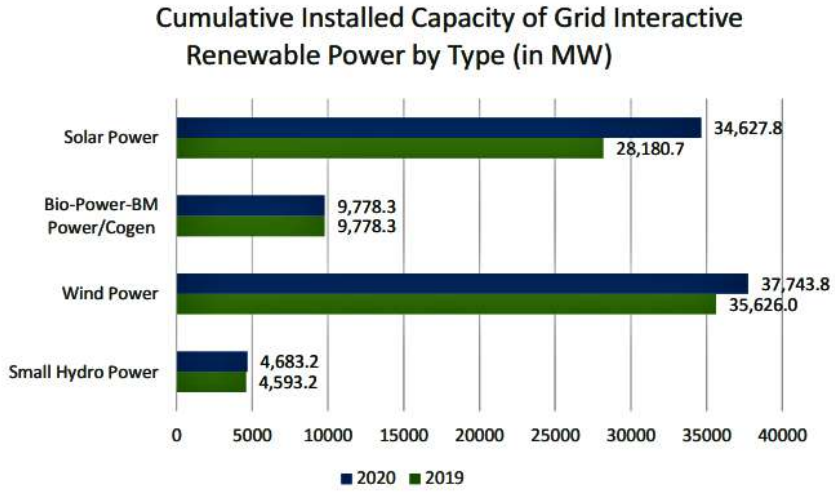


(b) Cumulative installed capacity of grid interactive renewable power by type (in MW) (X-axis: Year ; Y-axis: Electricity generation in MW)

Figure 1.2: Cumulative installed capacity of grid interactive renewable power by type (in MW) (X-axis: Renewable sources ; Y-axis: Energy generation in MW)

towards the faster development and adaptation of electric vehicles in India.

The future needs and criticality of renewable energy adaptation in the generation are the primary motivation behind this work to carry in the field of solar energy generation and integration with the grid.

1.3 Objectives

1. A current controller gain characterization of weak grid coupled solar inverter through impedance interaction modeling

2. To reduce the DC bus potential of the single-stage grid-connected inverter and provides the flexibility of DC bus grounding

3. To eliminate the circulating current within the inverter modules in a single-stage

grid-connected inverter through a novel high gain series inverter with asynchronous switching.

1.4 Organization of the thesis

1. **Chapter 1** deals with an introduction revolving around the power quality issues associated with single-stage grid-connected inverters due to improper arbitration of impedance in weak grid scenarios, elevated DC bus potential, and circulating current within the inverter modules. Later, the Motivation and objectives of the thesis are also furnished along with the organization of the thesis.

2. **Chapter 2** deals around deriving the positive damping for the PCC oscillations through a thorough assessment of system's natural response in a weak grid scenario. The presented work also attempted to derive the equivalent system impedance model by observing the natural interactions between the system and network impedance in the synchronous reference frame. With the obtained natural response through the axis transformation principle, the current controller gain characterization is proposed to accomplish the positive damping for power oscillations at PCC by assessing the controller sampling time effect. The presented work also briefed about accomplishing the grid injected power quality as per IEEE-1547(IEEE-519) standards by tuning of the positive damping towards the natural frequency of identified equivalent system impedance model.

3. **Chapter 3** discusses the new series inverter topology for the single-stage grid-connected inverter. The proposed topology eases the stress on the dc bus and protects the solar inverter from the issues associated with elevated dc potential (potential induced degradation effect, switch operating voltage stress, etc.), DC bus grounding, and circulating current within the inverter modules. The proposed configuration eliminates the common mode voltage (CMV) which is responsible for the circulating current by choosing the two inverters' appropriate switching combinations.

4. **Chapter 4** deals with the high gain voltage solar interface inverter topology aiming to reduce the DC bus voltage requirement further compare to the dual inverter series topology to realize the grid voltage. The grid voltage realization and the corresponding DC bus requirement are demonstrated through three variants of the proposed topology. For all three variants, the independent switching schemes are devised to accomplish the instantaneous per-phase impedance balance while synthesizing the grid voltage. With the devised switching schemes, all proposed variants operate with a common DC bus. Further, the closed-loop controller modeling is demonstrated for the proposed configuration through state space analysis for stable operation at the desired dynamic response.

5. **Chapter 5** presents the conclusion and future scope of the research work.

Chapter 2

A Current Controller Gain Characterization of Weak Grid Coupled Solar Inverter Through Impedance Interaction Modeling

2.1 Single stage grid connected solar inverter configuration

The space vector pulse width modulated (SVPWM) grid connected solar inverter with closed loop control is shown in Fig.2.1. In SVPWM, the DC bus utilization is more compare

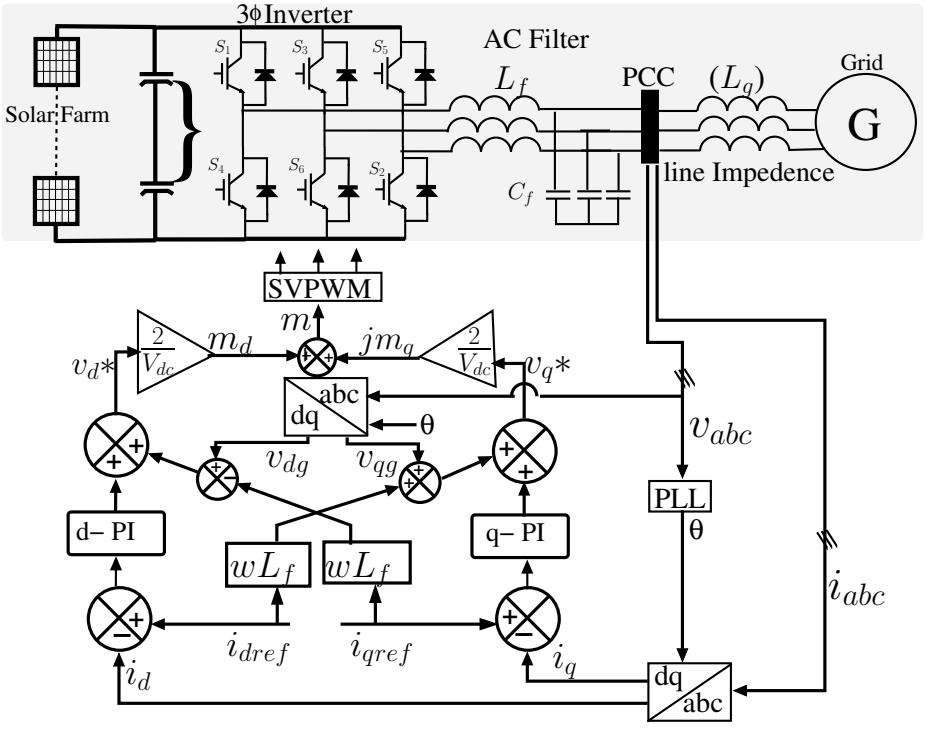


Figure 2.1: The circuit diagram of single stage grid connected inverter

to other PWM techniques including continuous and discontinuous PWMs. With SVPWM the DC bus utilization is approximately 16% more compare to Sine PWMs technique. In the closed loop control, the grid condition assessed by sensing the three phase voltages (v_a, v_b, v_c) and currents (i_a, i_b, i_c) at the PCC. The three phase voltages sensed at PCC

are passed to the PLL to generate the reference angle θ for the interface inverter. The reference angle θ is used to convert the three phase voltages and current on stationary reference frame into two phase synchronous reference (dq) frame. On the translated dq reference frame with grid voltage frequency (ω), v_{qg} is zero and v_{dg} appear to be the DC quantity correspond to the magnitude of the three phase grid voltages. Thus v_{dg} act as reference for the current control loop align in phase with d-axis shown in Fig.2.2. The q-axis is the orthogonal to d-axis represents the reactive power requirement of the system. In the stiff grid scenario the filter inductance L_f is the only inductance connected between the PCC and Inverter. So in order to deliver the desired active power as shown in Fig.2.2 to the grid, the reactive power compensation correspond to filter inductance L_f is given in the feed forward q-current loop shown in Fig.2.1. The current controller generate the corresponding modulation ($m_d + jm_q$) for desired real and reactive power being injected to grid. The PI controller of d-loop and q-loop decides the dynamic response of the complete system. The reference for the d-loop (i_{dref}) can be varied as per the real power being injected to grid, in general (i_{dref}) derived from maximum power point algorithm. In this work, i_{qref} made equal to zero indicates the reactive power deliver to the grid is zero. With this the resultant inverter voltage (v_{inv}) can be represented as:

$$v_{inv} = (V_{dg} - i_{qref}.\omega.L_f + \widetilde{V_{dPI}}) + j(V_{qg} + i_{dref}\omega L_f + \widetilde{V_{qPI}})$$

Considering the discussed criteria, the v_{inv} simplifies to

$$v_{inv} = (V_{dg} + \widetilde{V_{dPI}}) + j(i_{dref}\omega L_f + (\widetilde{V}_{q_{PI}} \approx 0)) \tag{2.1}$$

The phasors correspond to the position of the v_{inv} to deliver the designated active power to the grid is shown in Fig.2.2.

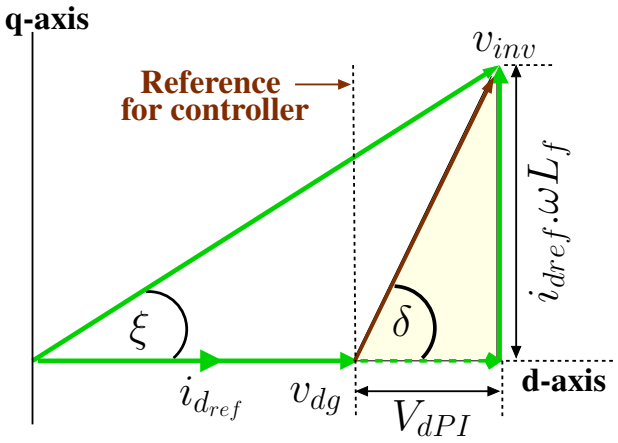


Figure 2.2: The phasor diagram representing the stiff grid scenario

2.2 The system dynamic assessment in weak grid scenario

In the case of weak grid scenario, apart from the filter inductance L_f between the inverter and the PCC, the grid inductance L_g would present between PCC and the grid as shown in Fig.2.3. With the introduced L_g in weak grid scenario, the virtual inertial time constant

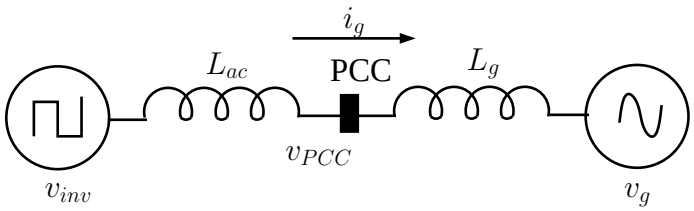


Figure 2.3: The simplified single line diagram to explain the weak grid scenario

of the filter loop can be viewed between the grid and the inverter as $\frac{L_f+L_g}{R_g}$. Here R_g is a virtual resistance correspond the power being injected to grid (V_{dg}/i_{dref}). With the deviated inertial time constant, the real (d-) and reactive (q-) axis deviated by γ angle and can be identified as new (d_w) and (q_w) axis as shown in Fig.2.4a. The axis transformation from d-axis to d_w axis can be represented with new inertial deviation angle correspond to grid injected current due to grid inductance (L_g) and grid resistance (R_g) as:

$$\gamma = tan^{-1}\frac{i_{dref}.\omega.L_g}{i_{dref}.R_g} \qquad ;\gamma = tan^{-1}\frac{\omega.L_g}{R_g} \tag{2.2}$$

In stiff grid scenario with reference to the d- and q-axis, the controller synthesize the δ angle (Fig.2.2) to bring grid injected current in phase with the grid voltage V_{dg} at steady state. Whereas in the case of weak grid, the grid injected current can be derived with deviated inertial angle (γ) as shown in Fig.2.4a with reference to stiff grid voltage (V_{inv}) as:

$$i_{gw} = \frac{V_{inv}cos(\xi+\gamma)cos(\gamma) - V_{dg}}{R_g Cos(\gamma)} \tag{2.3}$$

From (2.3), it is evident that the when L_g equal to zero representing the stiff grid scenario, the i_{gw}=i_g= $\frac{v_{inv}cos\xi - v_{PCC}}{R_g}$. With the deviated current due to γ, the real voltage on the d_w axis can be identified as $v_{inv_{dw}}$=$i_{gw}.R_g$ as shown in Fig.2.4a. Since the real and reactive power reference in d-q domain inline with V_{PCC}, the current (i_{gw}) projections and corresponding power in the synchronous reference frame can be computed as:

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} = \begin{bmatrix} i_{gw} \end{bmatrix} \begin{bmatrix} cos(\gamma) \\ sin(\gamma) \end{bmatrix} ; \begin{bmatrix} P_w \\ Q_w \end{bmatrix} = \begin{bmatrix} V_{PCC} i_{gw} \end{bmatrix} \begin{bmatrix} cos(\gamma) \\ sin(\gamma) \end{bmatrix} \tag{2.4}$$

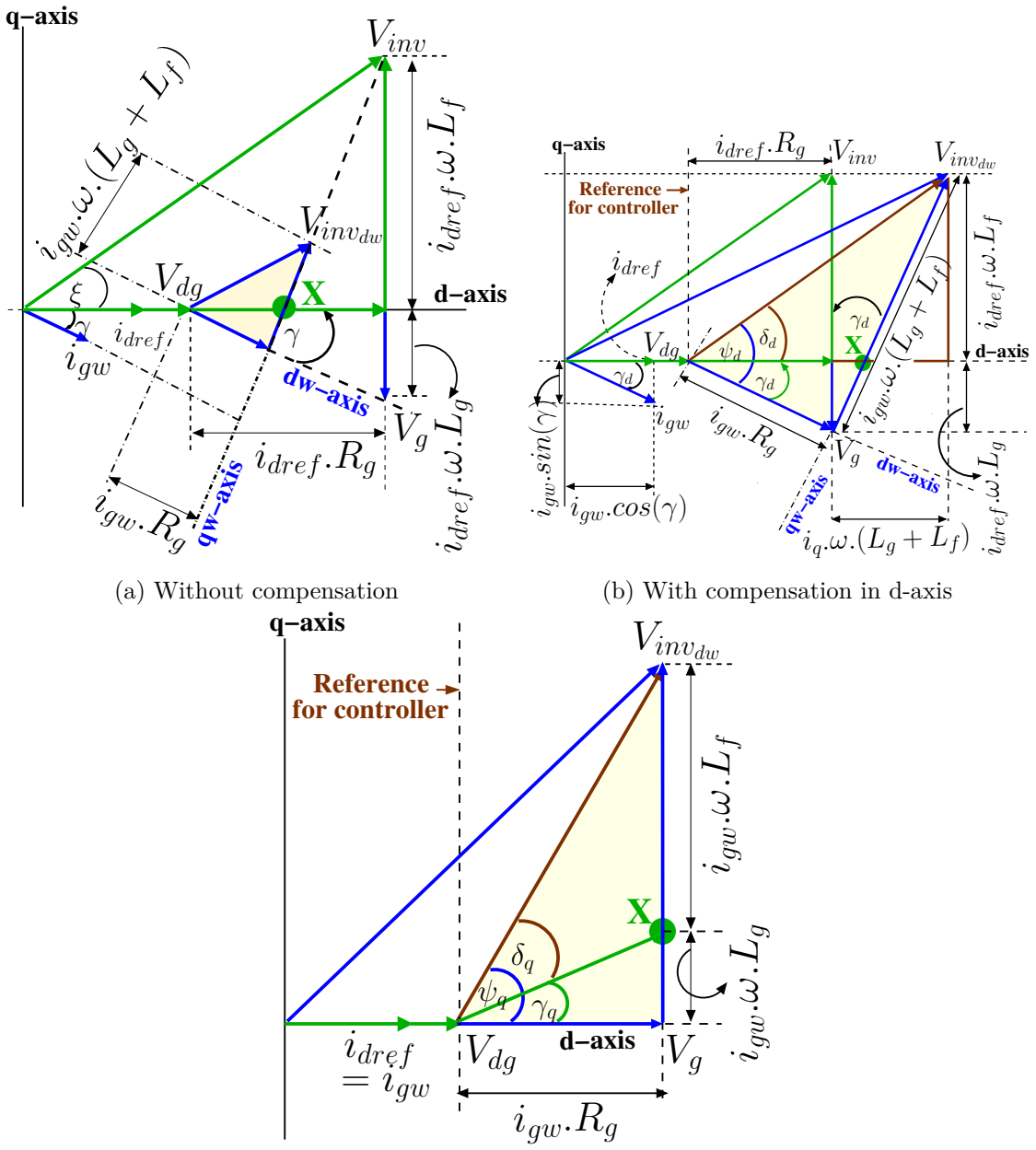
With the deviated current (i_{gw}) the PI controller can be expressed in a weak grid scenario as:

$$V_d^* = V_{d(PCC)} + (i_{dref} - i_{gw}.cos(\gamma))(K_p + K_i/s) \tag{2.5}$$

$$V_q^* = (-i_{gw}.sin(\gamma))(K_p + K_i/s) \tag{2.6}$$

$$V_{inv} = V_d^* + j.V_q^* \tag{2.7}$$

Here the K_p indicates the proportional gain and K_i indicates the integral gain of the PI controller. With the deviated angle γ the controller would try to bring $i_{gw}cos(\gamma)$ (referred onto d-axis) to i_{dref} as depicted in (2.5) in steady state to feed intended active power to the grid. Similarly in the q-axis, as depicted in (2.6), with the $i_{qref} = 0$, the current controller try to bring $i_{gw}sin(\gamma)$ (referred onto q-axis) to zero as per the reactive power reference. As it is shown in (2.5) and (2.6), the the d and q-axis controllers are coupled



(a) Without compensation

(b) With compensation in d-axis

(c) With compensation in q-axis direction

Figure 2.4: The phasor diagram representing the inverter voltage, grid voltage and grid injected current in weak grid scenario

with the angle γ. At steady states, the d-and q-axis controllers would try to reach to corresponding real and reactive power reference. But due to coupling angle γ, the V_{inv} experience the oscillations. The nature of the oscillations are analyzed independently in d- and q-axis with help of phasors depicted in Fig.2.4b and Fig.2.4c respectively. In real power correction as shown in Fig.2.4b, the $i_{gw}.R_g$ extended in the dw axis to match with the real power reference. In this process controller would deviate from v_{inv} (stiff grid with controller reference angle δ shown in Fig.2.2) to $v_{inv_{dw}}$ with angle of δ_d as shown in Fig.2.4b. The deviated angle δ_d can be computed as:

$$\psi_d = tan^{-1}\frac{i_{gw}w.(L_g+L_f)}{i_{gw}.R_g} \quad ; \quad \gamma_d = tan^{-1}\frac{i_{dref}w.L_g}{i_{dref}.R_g}$$
$$\delta_d = tan^{-1}\frac{\omega.L_f.R_g}{R_g^2-\omega^2(L_g.L_f+L_g^2)} \tag{2.8}$$

At the same time the controller in q-loop ($i_{gw}sin(\gamma)$) try to make equal to zero by aligning d_w axis to d-axis. In such case the position of V_{PCC} and v_{inv} variation with reference to stiff grid is shown in Fig.2.4c. In such scenario, the V_{inv} angle of deviation (δ_q) from the stiff grid scenario in q-direction can be computed as:

$$\psi_q = tan^{-1}\frac{i_{dref}w.(L_g+L_f)}{i_{dref}.R_g} \quad ; \quad \gamma_q = tan^{-1}\frac{i_{dref}w.L_g}{i_{dref}.R_g}$$
$$\delta_q = tan^{-1}\frac{\omega.L_f.R_g}{R_g^2-\omega^2(L_g.L_f+L_g^2)} \tag{2.9}$$

When both d-axis and q-axis controllers act together as per the real and reactive power references, the resultant oscillations derived through Fig.2.4b and Fig.2.4c is shown in Fig.2.5. The combined phasors shown in Fig.2.5 shows the voltage and grid injected current oscillations at the PCC. It represent the natural coupling between active and reactive power as depicted with the coupling trajectory shown in Fig.2.5 in a weak grid scenario with reference to coupling angle (γ) as depicted in (2.4). From (2.8) and (2.9), it is evident that the oscillations at the PCC with reference to grid injected current i_g, the resultant system transfer function can be modeled as:

$$G(s) = \frac{R_g.e^{-st}}{(L_g.L_f+L_g^2)(s^2+\frac{R_g.L_f.s}{L_g.L_f+L_g^2}+\frac{R_g^2}{L_g.L_f+L_g^2})} \tag{2.10}$$

The G(s) can be written in the form of $\frac{\omega_n^2 e^{-st}}{R_g(s^2+2\delta\omega_n s+\omega_n^2)}$. where $\omega_n = \frac{R_g}{\sqrt{L_g.L_f+L_g^2}}$ and $\delta = \frac{L_f}{2.\sqrt{L_g.L_f+L_g^2}}$. With identified weak grid transfer function G(s), the complete closed loop signal flow diagram with the PI controller is shown in Fig.2.6.

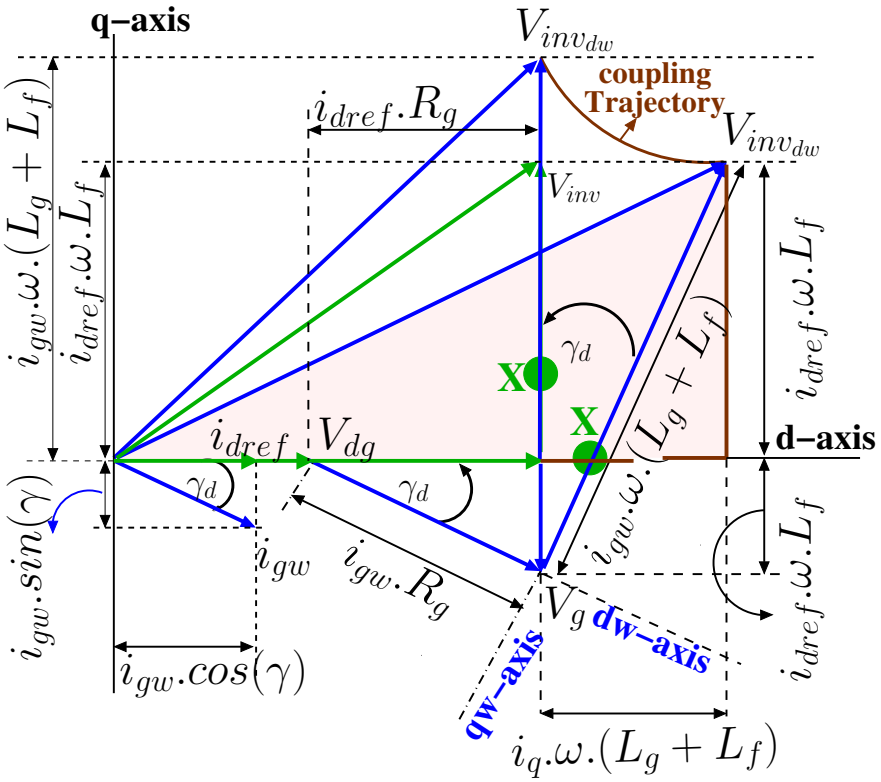


Figure 2.5: The phasor diagram representing inverter voltage oscillations due to coupling between d-axis and q-axis compensation in weak grid scenario

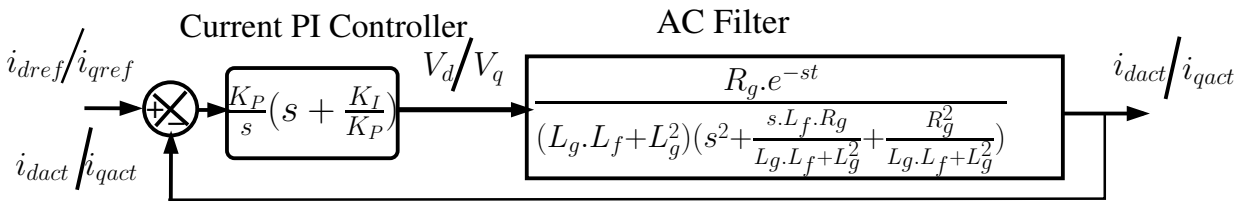


Figure 2.6: The simplified closed loop representation with the identified system transfer function and linear controller

2.3 The PI-controller modeling of plant for stable operation

The characteristic equation of the closed loop system can be derived from Fig.2.6 as:

$$\lambda(s) = 1 + (K_p + \frac{K_i}{s}).\frac{1}{R_g}.\frac{\omega_n^2.e^{-st}}{s^2 + 2\delta\omega_n s + \omega_n^2} \tag{2.11}$$

$$\lambda(s) = R_g.s(s^2 + 2\delta\omega_n s + \omega_n^2) + \omega_n^2(K_p.s + K_i)e^{-st} \tag{2.12}$$

$$\lambda^*(s) = e^{st}.\lambda(s) \quad \textit{and substituting } s = j\omega$$

$$\lambda^*(j\omega) = j\omega R_g(-\omega^2 + j2\delta\omega_n\omega + \omega_n^2)e^{j\omega t} + \omega_n^2(K_p(j\omega) + K_i) \tag{2.13}$$

The characteristic equation can be decomposed into real and imaginary components as:

$$\lambda^*(j.\omega) = \lambda_r(\omega) + j\lambda_i(\omega) \tag{2.14}$$

$$\lambda_r(\omega) = R_g(\omega^3 - \omega\omega_n^2)sin(\omega t) - 2\delta\omega_n\omega^2 R_g cos(\omega t) + K_i.\omega_n^2 \tag{2.15}$$

$$\lambda_i(\omega) = \omega(R_g(\omega_n^2 - \omega^2)cos(\omega t) - 2\delta\omega_n\omega R_g sin(\omega t) + K_p\omega_n^2) \tag{2.16}$$

Here 't' represents the sampling time interval of the controller. From (2.15) and (2.16) it is evident that the roots of the imaginary part ($\lambda_i(\omega)$) of characteristic equation should goes to zero to make real roots. Therefore the tuning of K_p plays a vital role in controlling power oscillations at PCC. Through stability criteria mentioned in [63], the appropriate K_p value can be derived through the roots of the λ_i. To verify the system stability as per [63], the $\lambda^*(s)$ is stable for any value of angle z_0 (ωt) varying from [-∞,+∞] only when .

1. Condition-1 : $E(z_0)$=$\lambda_i'(z_0).\lambda_r(z_0) - \lambda_i(z_0)\lambda_r'(z_0) > 0$

2. Condition-2 : $\lambda_r(z_0)$ and $\lambda_i(z_0)$ have only simple real roots and are interlace

While finding the lower limit of K_p through condition-1 at obvious root $z_0 = 0$, the $E(Z_0)$ can be written as:

$$E(0) = \lambda_r(0).\lambda_i'(0) = K_i\omega_n^2(Rg\omega_n^2/t + K_p\omega_n^2/t) > 0$$
$$\implies K_p > -R_g \quad at \quad \omega_n > 0 \tag{2.17}$$

The upper boundary of the K_p can be found through interlacing roots condition mentioned in condition-2 by making λ_i=0, that implies

$$R_g(\omega_n^2 - (z/t)^2)cos(z) + K_p\omega_n^2 = 2\delta\omega_n\omega R_g sin(z) \tag{2.18}$$

$$f(z) = g(z) \tag{2.19}$$

The (2.18) only can be solved graphically to find the interlace roots in the interval [0,π]. Through the graphical method, the intersection point of $f(z)$ and $g(z)$ gives the value of the K_p at various filter inductance (L_f), grid inductance (L_g) and virtual resistance (R_g). The variations of $f(z)$ and $g(z)$ with reference to the grid parameters (virtual resistance (R_g) and grid inductance (L_g) is shown in Fig.2.7 and Fig.2.8 respectively. In both the graphs the intersection points represents the solution for λ_i at given K_p. The variations of the $f(z)$ and $g(z)$ at different K_P is shown in Fig.2.9 for a given R_g and L_g. As shown in Fig.2.9, with the variations of K_P, the intersection point of $f(z)$ and $g(z)$ varies and at one certain K_p, $f(z)$ just touches $g(z)$ (say K_{P3} in Fig.2.9) defines the upper boundary of the K_p beyond which the system is unstable. Therefore the tangential point of $f(z)$ and $g(z)$ defines the K_p for maximum boundary of the stability region. At tangential condition, the (2.18) can be written as:

$$R_g(\omega_n^2 - (z_u/t)^2)cos(z_u) + K_{Pu}\omega_n^2 = 2\delta\omega_n(Z_u/t)R_g sin(z_u)$$

$$\frac{d}{dz_u}[R_g(\omega_n^2-(z_u/t)^2)cos(z_u)+K_{Pu}\omega_n^2]=\frac{d}{dz_u}[2\delta\omega_n(Z_u/t)R_g sin(z_u)] \tag{2.20}$$

$$\implies R_g(-2Z_u/t^2)cos(z_u)+R_g(\omega_n^2-(Z_u/t)^2)(-sin(Z_u))$$
$$=2\delta\omega_n R_g sin(z_u)/t+2\delta\omega_n(Z_u/t)R_g cos(z_u) \tag{2.21}$$

To determine the upper boundary of K_p, the z_u should be in the interval [0,π] satisfying

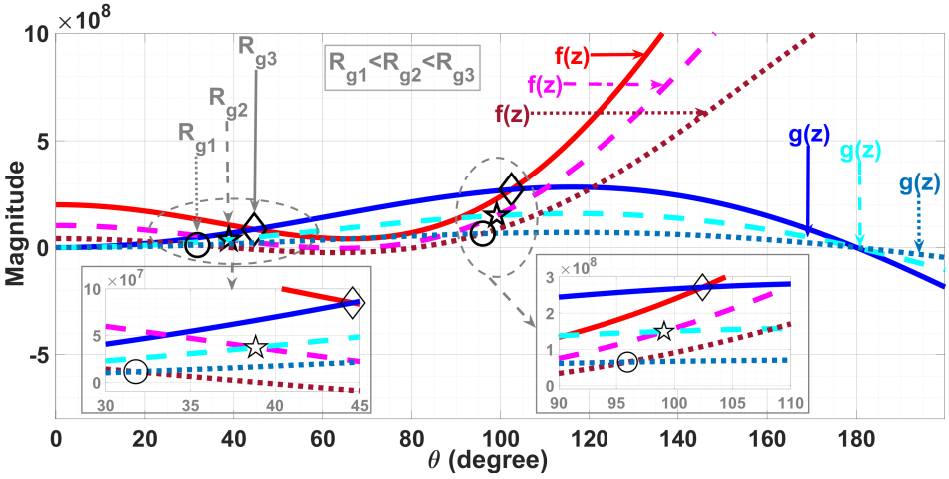


Figure 2.7: The variations of $f(z)$ and $g(z)$ (mentioned in (2.19)) with varying resistance (R_g) at a given filter inductance (L_f) and grid inductance (L_g)

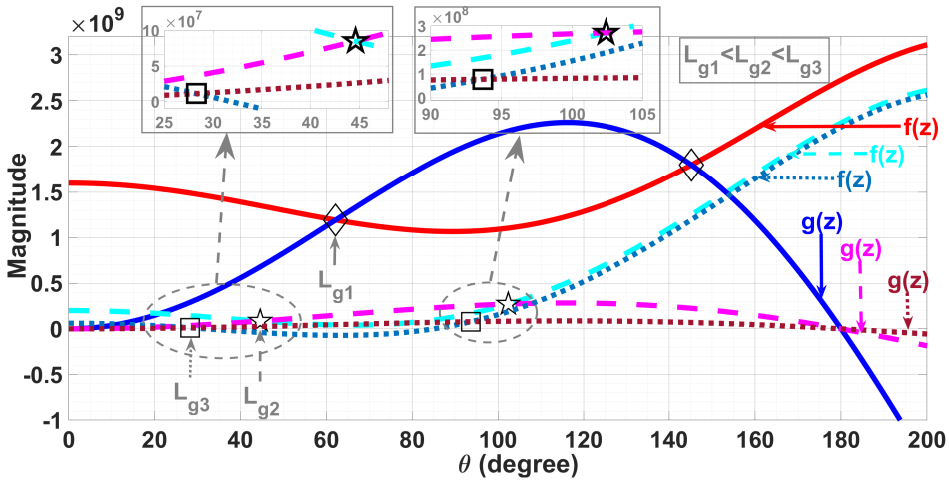


Figure 2.8: The variations of $f(z)$ and $g(z)$ of (mentioned in (2.19)) with varying grid inductance (L_g) at a given filter inductance (L_f) and resistance (R_g)

the $Tan(z_u)$ derived from (2.21) as:

$$\implies Tan(z_u)=\frac{z_u(2R_g+2R_g\delta\omega_n.t)}{R_g(z_u^2-\omega_n t^2-2\delta\omega_n.t)}$$
$$=\frac{z_u(2(N+N^2)+Mt)}{z_u^2(N+N^2)-M^2t^2-Mt} \tag{2.22}$$

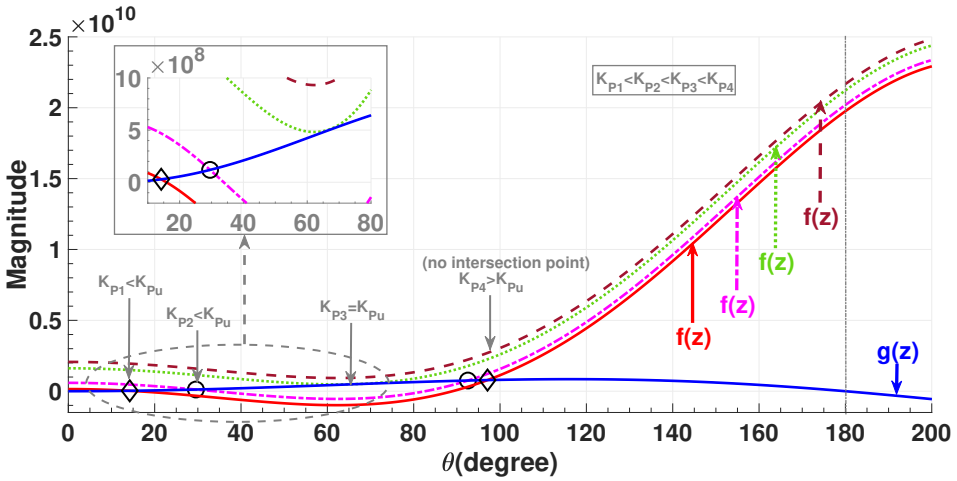


Figure 2.9: The variations of $f(z)$ and $g(z)$ (mentioned in (2.19)) with varying K_p at given grid inductance (L_g),filter inductance(L_f) and resistance (R_g)

where $M = \frac{R_g}{L_f}$ and $N = \frac{L_g}{L_f}$. With varying M and N, the variation of z_u is shown graphically in Fig.2.10. With consideration of computed z_u, the upper boundary of $K_p(K_{Pu})$ can be computed as:

$$K_{Pu} = \frac{2\delta\omega_n R_g(z_u/t)sin(z_u) - R_g cos(z_u)(\omega_n^2 - (z_u/t)^2)}{\omega_n^2}$$
$$= \frac{1}{M}R_g\frac{z_u}{t}sin(z_u) - R_g cos(z_u)(1 - \frac{(\frac{z_u}{t})^2(N+N^2)}{M^2}) \tag{2.23}$$

With this the stable region of the K_p can be defined as $-R_g < K_p < K_{Pu}$. After the determination of roots for the λ_i, pass onto the λ_r exploiting the condition-2 (mentioned λ_i and λ_r root are real and interlace) to compute the value of K_i as:

$$\lambda_r(z_u) = R_g sin(z_u)((\frac{z_u}{t})^3 - (\frac{z_u}{t})\omega_n^2) - 2\delta\omega_n(\frac{z_u}{t})^2 R_g cos(z_u) + K_i.\omega_n^2 \tag{2.24}$$
$$= \omega_n^2(K_i - a(z_u)) \tag{2.25}$$
$$a(z_u) = (\frac{z_u}{t})(\frac{N^2+N}{M^2})(R_g sin(z_u)(\frac{M^2}{N^2+N} - (\frac{z_u}{t})^2) + (\frac{1}{M})(\frac{z_u}{t})^2 R_g cos(z_u) \tag{2.26}$$

As per the necessary and sufficient condition mentioned in condition -2 (preceding section-2.3) reveals that λ_r and λ_i roots are real and interlaced. Thus substituting z_u, the $a(z_u) < 0$ forces the energy function (E)>0 for all $K_i < a(z_u)$ and $K_p < K_{Pu}$. Further to verify derived K_p and K_i limits for necessary and sufficient requirement, the condition-1 (energy function E >0 as depicted in section 2.3) is evaluated as shown in Fig.2.11 with different K_p and K_i. As it is shown in Fig.2.11a, when $K_p < K_{Pu}$ (computed with L_g=14mH, L_f=14mh, R_g=20Ω) at $K_i < a(z_u)$ energy function is positive beyond which, the energy function is negative indicating the system is unstable. Similarly, the K_i variations at K_{Pu} is shown in Fig.2.11b confirms the $K_i < a(z_u)$ the system is stable.

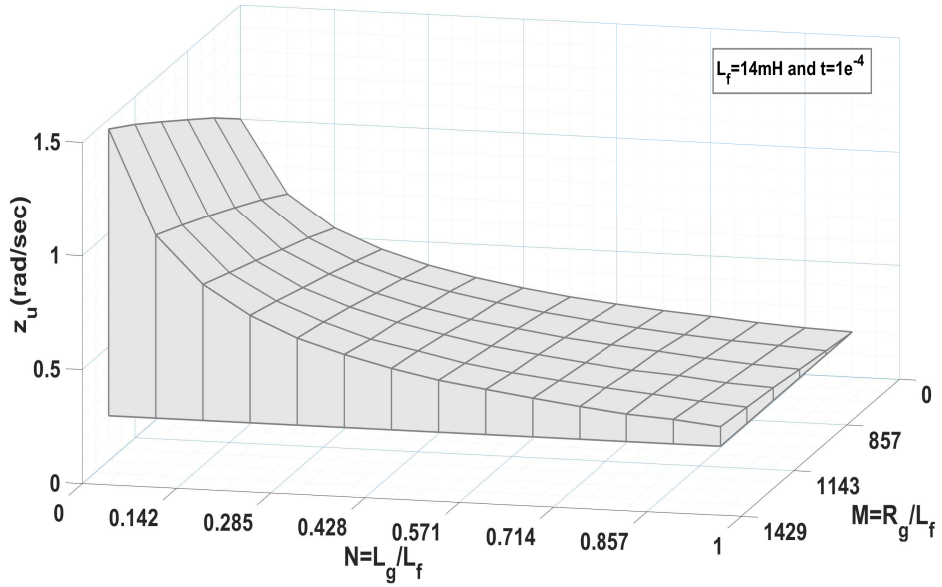
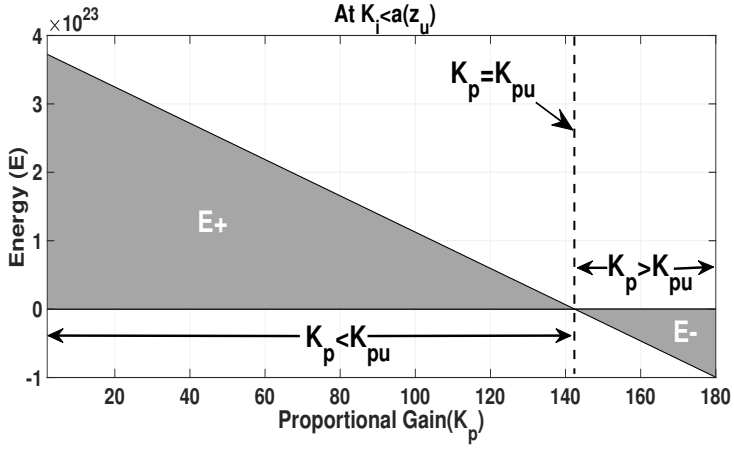
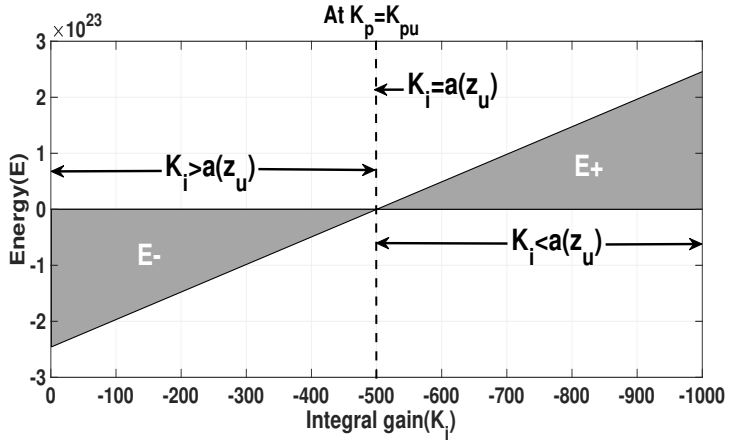


Figure 2.10: The identified z_u boundaries of stable region for different M and N values



(a) E (Energy function) Vs (K_p)



(b) E (Energy function) Vs (K_i)

Figure 2.11: The variation of energy function with reference to controller gains

2.4 The controller gain characterization for enhanced power quality

With the defined boundary of the K_p and K_i for stable operation, further the roots of the λ^* is considered based on the inertial constant of the system. The proposed inertial constant δ_d and δ_q shown in (2.8) and (2.9) respectively vary between 0 to $\pi/2$ when ω varies from 0 to ω_n. Beyond ω_n, $R_g^2 < \omega^2(L_g L_f + L_g^2)$ indicates the system is oscillatory in nature as the imaginary part is dominant compare to real part at $\delta_d > \pi/2$. Therefore in this work, it is proposed to choose the ω_n as the root for λ_i to derive value K_{Po} within the stable region of K_{Pu}.At $(z/t) = \omega_n$ and $z = \delta_d$ *or* δ_q=$\pi/2$, the value of K_p can be derived as:

$$K_{Po} = \frac{2R_g\delta\omega_n^2 sin(\delta_d)}{\omega_n^2} = \frac{R_g}{\sqrt{(N+N^2)}} \tag{2.27}$$

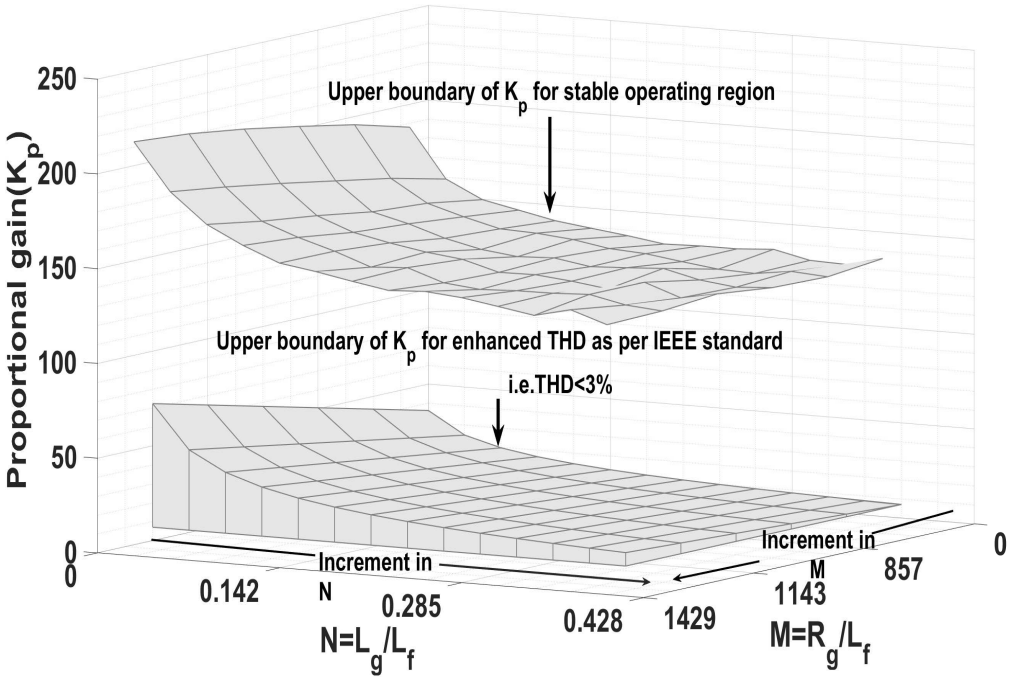


Figure 2.12: The identified proportional gain boundaries of stable region and augmented grid injected current quality region for different M and N values

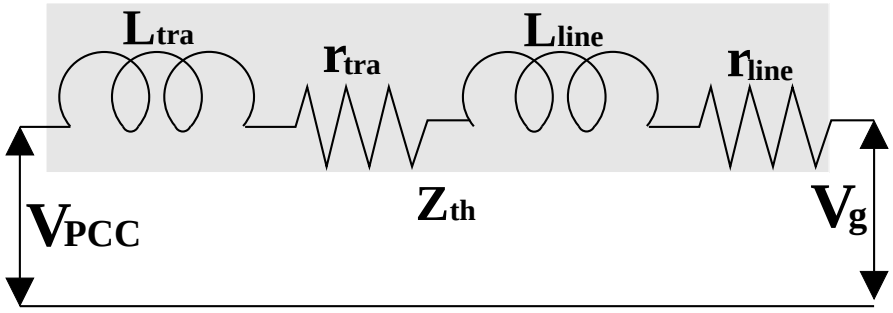
In this work, the proposed proportional gain range for the PI controller is $-R_g < K_p < K_{Po}$ for any M and N value, where K_{Po} is a subset of K_{Pu}. The K_{Pu} and K_{Po} represent the upper boundary of stability region and improved power quality region, respectively, as shown in Fig.2.12. The presented work mainly focused on offered impedance to the oscillation caused by the deviated inertial angle (γ) through controller gains. The efficacy of the derived controller gains to bring the system into positive damping region is explained in subsequent result section by performing lab experiments on the grid connected inverter configuration with mimicked grid inductance L_g.

2.5 Result and Discussion

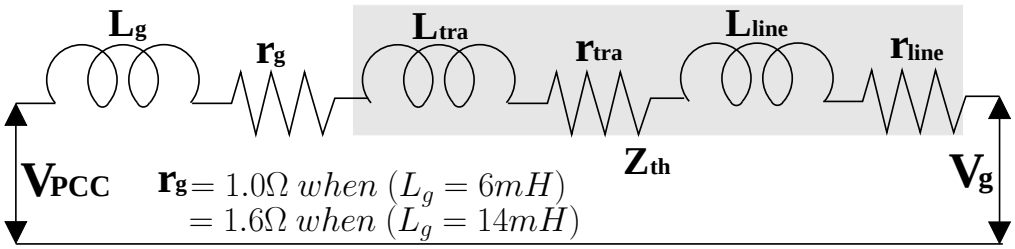
In this work, the grid inductance L_g is mimicked considering the short circuit ratio (SCR) correspond to weak grid scenarios as explained in [25]. The SCR ratio is computed using the typical values of line impedance to derive the weak grid (2<SCR<3) and very weak grid (SCR<2) conditions. In both the cases SCR ratio is computed as:

$$SCR = \frac{V_g^2}{P_{pv_{rated}}.Z_{th}} \tag{2.28}$$

Here V_g is grid voltage at PCC, $P_{pv_{rated}}$ is the inverter rated power injected to the grid, Z_{th} is the thevenin equivalent impedance of the grid seen at the PCC. In general, the Z_{th} includes the line impedance (typically L_{line}=0.0019H/km and r_{line}=0.2153Ω) and transformer impedance (typically L_{tra}=0.004H and r_{tra}= 3Ω) as shown in Fig.2.13.The SCR ratio computed considering 2kM line distance (university campus scenario) as 4 represents the stiff grid scenario shown in Fig.2.13a. The SCR ratio is altered by introducing L_g=6mH and 14 mH after PCC to achive weak grid (2<SCR<3) and very weak grid (SCR<2) scenarios and corresponding single line diagram shown in Fig.2.13b. In Fig.2.13b, the r_g represents the wire resistance of the inductor (L_g). Apart from the grid inductance, the SCR ratio dependant on the grid injected power by the inverter. The two injected power scenarios (R_g=48Ω correspond to 3.4kW and R_g=68Ω correspond to 2.4kW) are considered that makes four test cases as follows to validate the proposed controller gain characterization.



(a) Stiff grid scenario (SCR>3)



(b) Weak grid (2<SCR<3) and very Weak grid (SCR<2)scenario

Figure 2.13: The single line diagram representing the line impedance's between PCC and the grid

1. case-1: $R_g = 48\Omega$ and L_g=14 mH
2. case-2: $R_g = 48\Omega$ and L_g=6 mH
3. case-3: $R_g = 68\Omega$ and L_g=14 mH
4. case-4: $R_g = 68\Omega$ and L_g=6 mH

2.5.1 Hardware validation

With the identified test cases, the proposed controller gain characterization is verified on hardware prototype shown in Fig.2.14 by considering the parameters tabulated in Table-2.1. For identified test cases, the controller gains (K_{p_u}) and (K_{p_o}) are computed using (2.23) and (2.27) respectively and tabulated as depicted in Table-2.2. The two

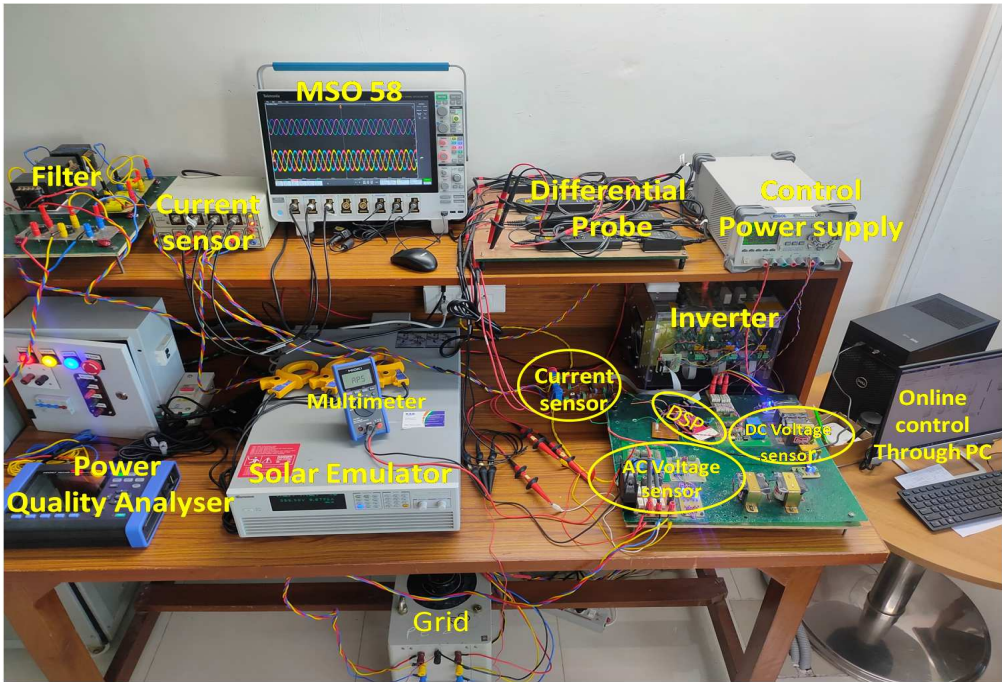


Figure 2.14: The hardware prototype developed in lab for experimental validation

Table 2.1: The operating parameters of the grid connected inverter

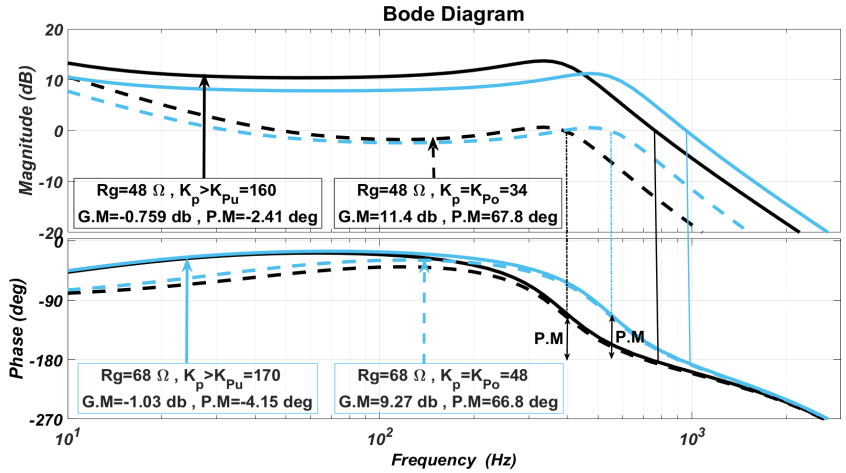
Parameter	Value	Units
Power ($P_{pv_{rated}}$)	3.4	kW
DC operating voltage (V_{dc})	700	Volts
Grid voltage (l-l (RMS)) (V_g)	415	Volts
Fundamental Frequency (f)	50	HZ
Switching Frequency (f_{sw})	8	kHZ
Sampling time (t)	$1e^{-4}$	Seconds
AC filter Inductance (L_f)	14	mH
AC filter Capacitance (C_f)	2.04	μ F
AC Current Ripple	5	%

variations of grid inductance and the grid resistances are considered to validate the

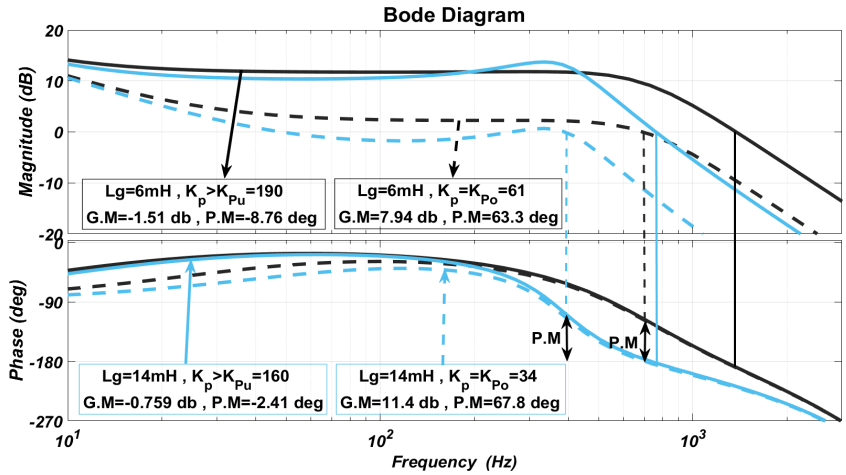
Table 2.2: The tested grid parameters with identified proportional gains

$R_g(\Omega)$	$L_g = 14mH$		$L_g = 6mH$	
	K_{Pu}	K_{Po}	K_{Pu}	K_{Po}
48Ω	154	34	184	61
68Ω	164	48	200	87

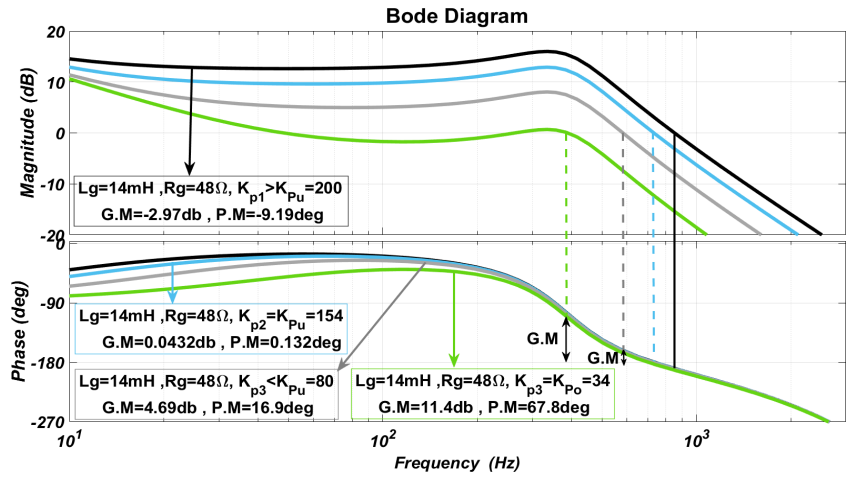
proposed controller gains.For the considered L_g and R_g,the improved phase margin with proposed gain region is validated through the system's (2.11) frequency response with the grid parameter mentioned in Table-2.2. For tabulated values of L_g, R_g and K_p, the frequency response of the system is shown in Fig.2.15. The Fig.2.15a depicts the frequency response of (2.11) with reference to variations of R_g (48Ω and 68Ω mentioned in Table-2.2) at L_g = 14mH with the controller gains $K_p > K_{Pu}$ and the $K_p = K_{Po}$. At R_g=48Ω, the computed K_{Pu} is 154 above which the system is unstable with observed phase margin of -2.41°as shown in Fig.2.15a. For the same L_g and R_g at $K_p = K_{Po} = 34$ (shown in Table-2.2), the system is stable with the improved phase margin of 67.8°as shown in Fig.2.15a (dashed black line). Similarly at same $L_g = 14mH$ with $R_g = 68\Omega$, the system is unstable above the K_{Pu} and gradually bring the system to stable region with improved phase margin from -4.15°to 66.8°when $K_p = K_{Po} = 48$ as shown in Fig.2.15a with blue color. In the other variation the R_g kept constant at 48Ω, the frequency response of the system is observed for $L_g = 14mH$ and $L_g = 6mH$ as shown in Fig.2.15b. In both the cases as it is evident from Fig.2.15b, at $K_p > K_{Pu}$ (computed in table-2.2), the system is unstable. With the tuned K_p to $K_{Po} = 34$ in case of $L_g = 14mH$ and 61 in case of $L_g = 6mH$ respectively improves the system stability with improved phase margin of 67.8°and 63.3°. For clear understanding, the effect of K_p on the phase margin is illustrated through Fig.2.15c at L_g=14mH and R_g=48Ω. The four values of K_p has choose representing as 200 ($> K_{Pu}$), 154 ($= K_{Pu}$), 80($< K_{Pu}$) and 34 ($= K_{Po}$) as shown in Fig.2.15c. As it is shown in Fig.2.15c, the system is unstable above K_{Pu} and between K_{Pu} to K_{Po}, it is observed that the phase margin improves gradually under stable operating condition from 0.132°to 67.8°. The improved margin ensures improved power quality of the system.Further the computed controller gains (Table-2.2) are tested on grid connected inverter prototype with the above mentioned test cases. The grid injected current and the corresponding harmonic spectrum for all test cases are shown in Fig.2.16 with the controller gains (K_P) equal to 140, 87, and 34. In test case-1, correspond to $R_g = 48\Omega$, the grid injected current reference (I_{dref}) maintained at 4.8 Amps at grid voltage of 415 V (l-l RMS). With L_g=14mH, the system is at verge of stability at K_P=140 with maximum harmonic oscillations concentrated at the frequency of 400Hz as depicted in left trace of Fig.2.16a. Whereas with the K_P= 87, the magnitude of the harmonics concentrated at 400Hz reduces significantly proves the controller gain impact on the system power oscillations. Further at $K_P = 34$ indicates the computed gain in this case for the improved power quality ensures the complete elimination of current harmonics at 400Hz as shown in right trace of Fig.2.16a brings overall current %THD less than 3%. However in case-2, the



(a) L_g=14 mH, R_g=48 Ω (black) and 68 Ω (blue) with $K_P > K_{Pu}$ (solid line) and $K_p = K_{Po}$ (dashed line)



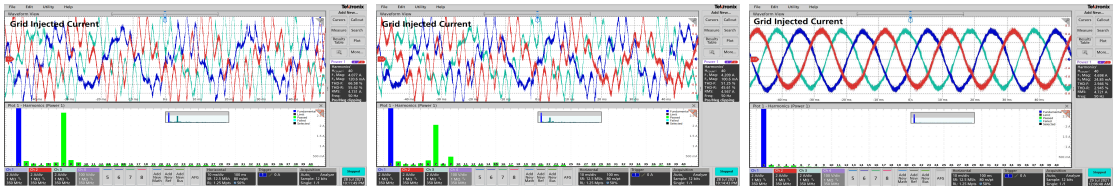
(b) R_g =48 Ω, L_g=6 mH (black) and 14 mH (blue) with $K_P > K_{Pu}$ (solid line) and $K_p = K_{Po}$ (dashed line)



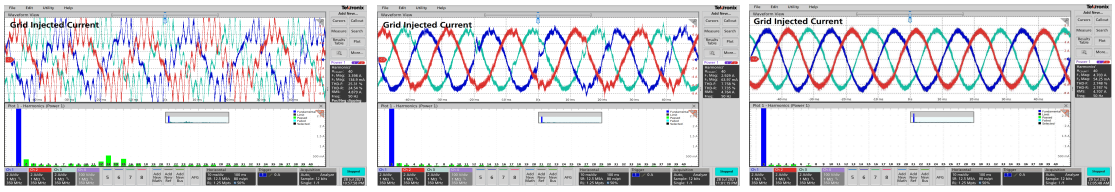
(c) L_g=14mH and R_g=48 Ω with varying K_p

Figure 2.15: Frequency response of the closed loop system shown in Fig.2.6

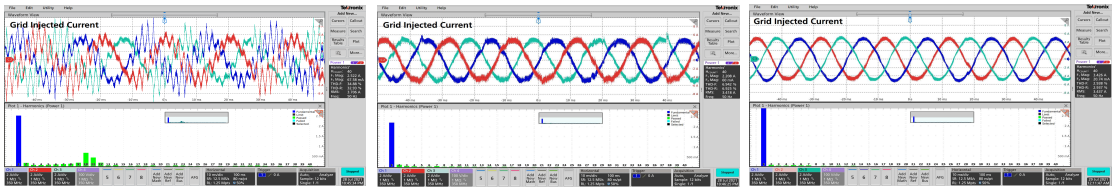
L_g reduced to 6mH, the computed K_{Pu} and K_{Po} are 184 and 61. Thus, when the system operate with K_P=140 shown in left trace of Fig.2.16b, the current harmonics shifted right



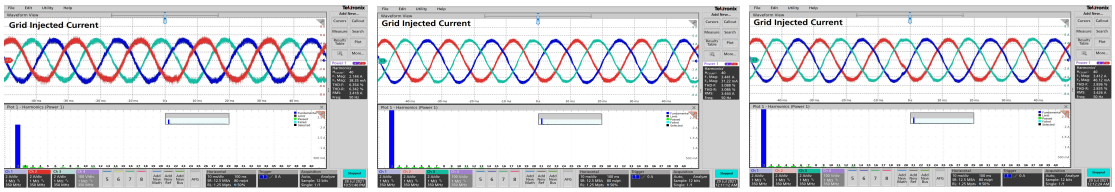
(a) Case-1 with $K_p = 140$ (Left trace), 87 (Middle trace) and 34 (Right trace)



(b) Case-2 with $K_p = 140$ (Left trace), 87 (Middle trace) and 34 (Right trace)



(c) Case-3 with $K_p = 140$ (Left trace), 87 (Middle trace) and 34 (Right trace)



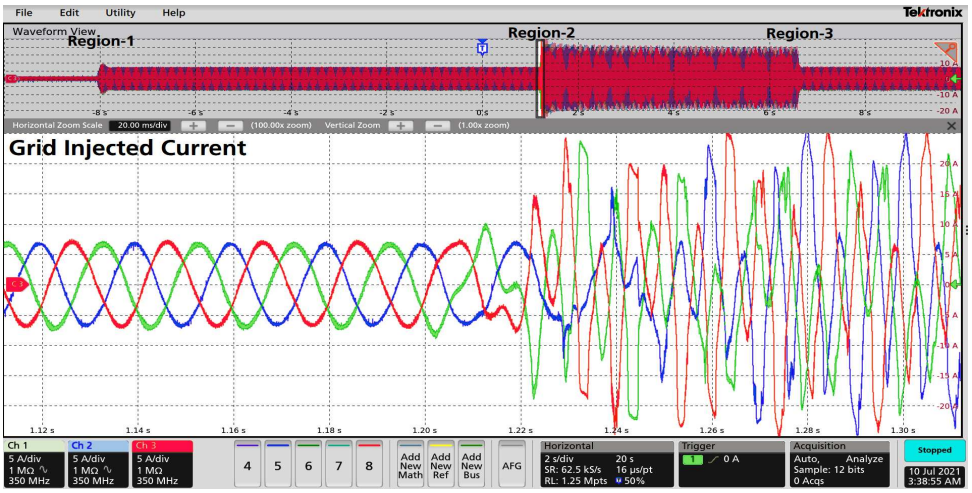
(d) Case-4 with $K_p = 140$ (Left trace), 87 (Middle trace) and 34 (Right trace)

Figure 2.16: The profile of Grid injected current (top)and corresponding current harmonic spectrum (bottom bottom)

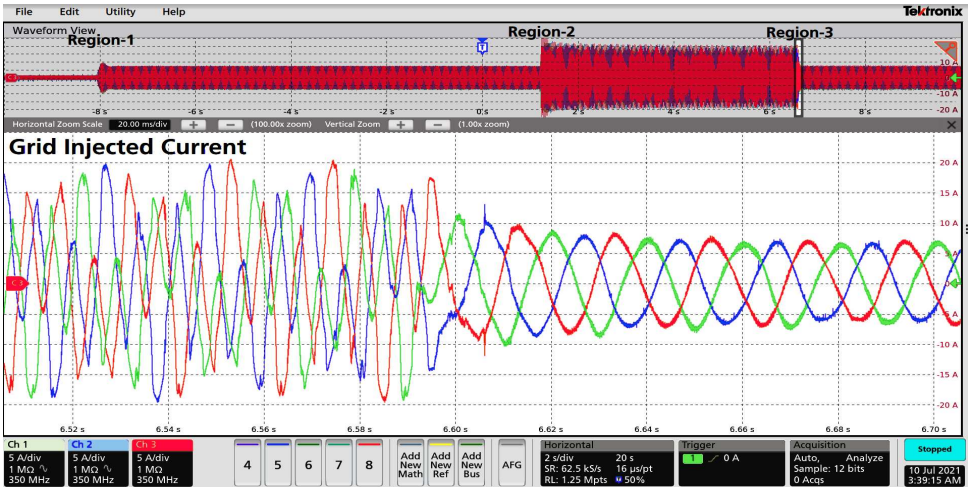
(around 700 Hz) in spectrum compare to case-1. The corresponding grid injected current oscillations depicted in top left trace of Fig.2.16b is lesser compare to case-1 for same K_P. Similarly the corresponding grid injected current profiles observed in middle and right trace of Fig.2.16b are better compare to case-1 (middle and right trace of Fig.2.16a) when the current controller operate with same K_P of 87 and 34 respectively. In other variations, the R_g value has been changed from 48Ω to 68Ω by changing I_{dref} to 3.4 Amps. In this scenario, with $L_g = 14mH$, the corresponding K_{Pu} and K_{Po} are computed as 164 and 48. Since $L_g = 14mH$ similar to case-1, the harmonics of grid injected current can be observed at 550 Hz, but with reduced magnitude at K_p=140 as shown in left trace of Fig.2.16c. Similarly at the K_P= 87 and 34, the grid injected current profiles are significantly improved due to increased damping compare to case-1. The improved damping can be observed through current %THD respectively as 6.9% and 2.9% from middle and right trace of Fig.2.16c compare to case-1 (51.25% and 2.95%) respectively at K_p= 87 and 34. In case-4, the L_g is decreased to 6mH at R_g = 68Ω with widened K_{Pu} = 200 and K_{Po} = 87 compare to above three cases, the profile of grid injected current is harmonic free as shown in left, middle and right trace of Fig.2.16d. Here it can also be observed that the %THD is 3% with K_p = 87 confirming the efficacy of

proposed controller gain for enhanced power quality by observing the natural impedance interactions.

Further the dynamics of the oscillations are shown in Fig.2.17a by introducing L_g = 14mH at t=1.21 sec. The corresponding %THD can be observed 67% (of fundamental). At t=6.67, the controller gain shaping is initiated and adjusted correspond to computed K_{Po} = 34, the corresponding dynamics in the oscillation can be observed as shown in Fig.2.17b. From Fig.2.17, it is clear that the dynamic tuning K_P for improved power quality is feasible and corresponding space plot representing oscillation in d-q domain without and with proposed controller gains shown in left and right trace of Fig.2.18.



(a) With introduced L_g at t=1.21 sec using uncompensated controller gains



(b) With controller gain characterization at t=6.60 sec

Figure 2.17: The dynamic response of the grid injectd current in weak grid scenario with corresponding gain characterization

It is clearly evident from left trace of Fig.2.18, the oscillations in X-Y plane representing coupling between real and reactive power as explained in preceding section with the phasors (Fig.2.4). With the proposed controller gains, the inverter is stabilized to deliver the reference power to the grid as shown in right trace of Fig.2.18.

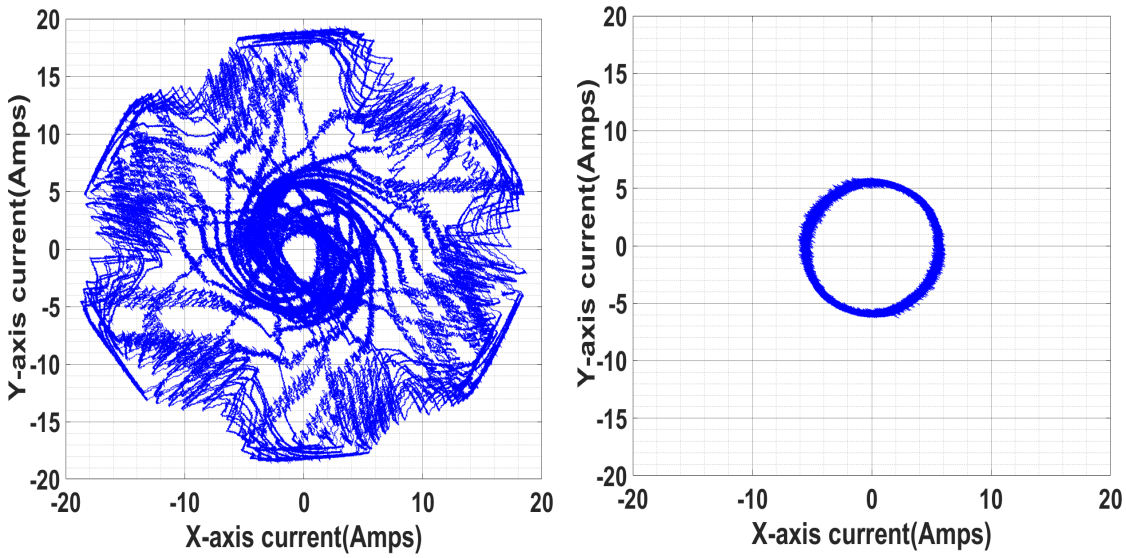


Figure 2.18: The grid injected current space plot (X-Y plot) in weak grid scenario without (left) and with (right) PI controller gain compensation

2.5.2 The demonstration of proposed controller gain characterization on IEEE-13 bus system

The proposed controller gain characterization is verified on IEEE-13 bus system considering the parameters tabulated in Table-2.1 with grid inductance L_g=14mH at the injected power of 3.4kW (corresponding $R_g = 48\Omega$) represents the case-1. As it is shown in Fig.2.19, the solar inverter is integrated at node-13 through line transformer after PCC. To mimic the weak grid scenario, $L_g = 14mH$ is introduced between the transformer and

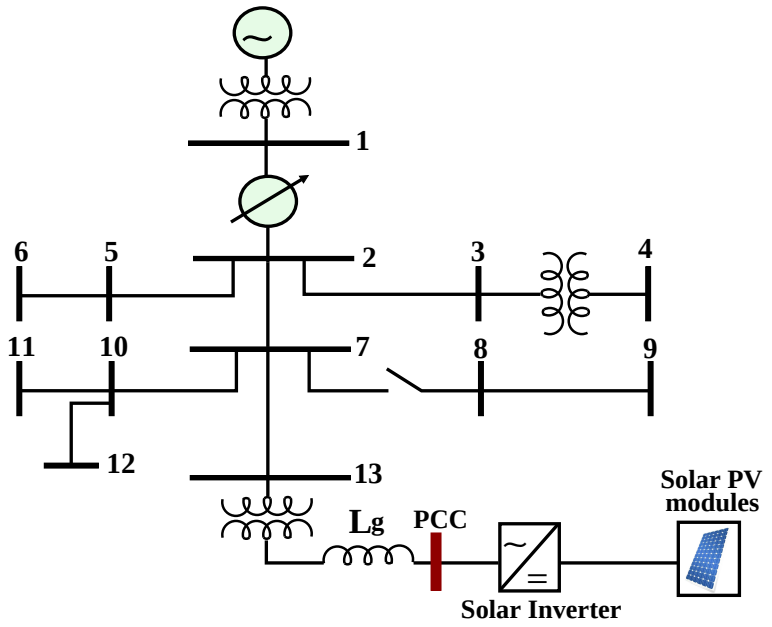
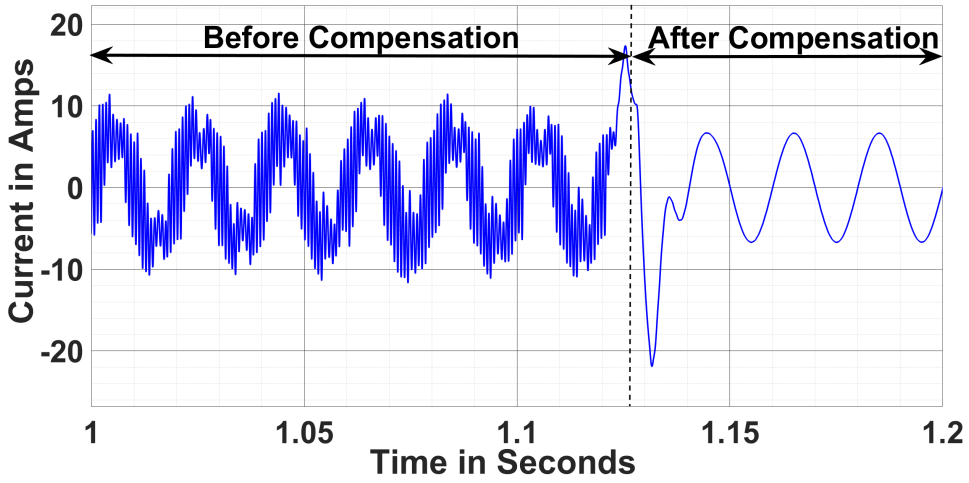


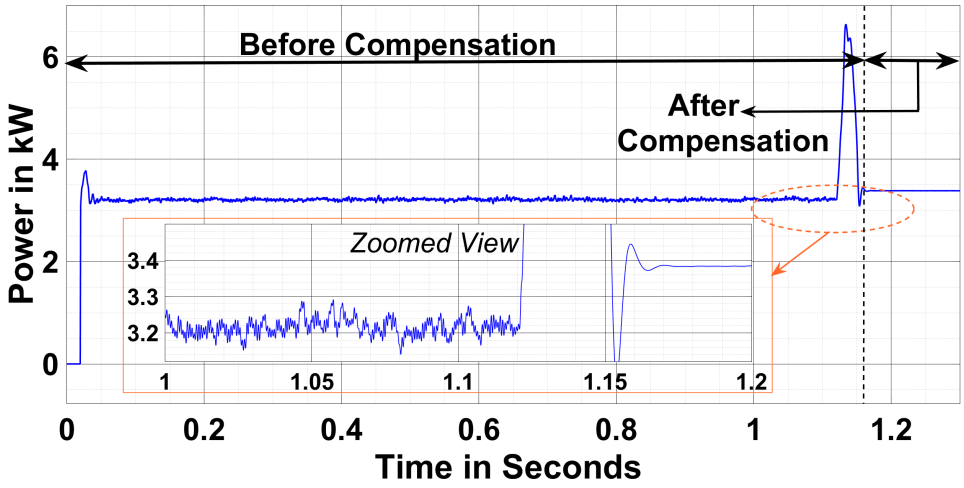
Figure 2.19: The single line diagram of standard IEEE-13 bus system with solar inverter integrated at node 13

PCC.With the considered L_g, the inverter injected current and corresponding power at

PCC with and without compensation is shown in Fig.2.20a and Fig.2.20b respectively.The proposed current controller gain compensation is initiated at t=1.12 sec as shown in Fig.2.20.



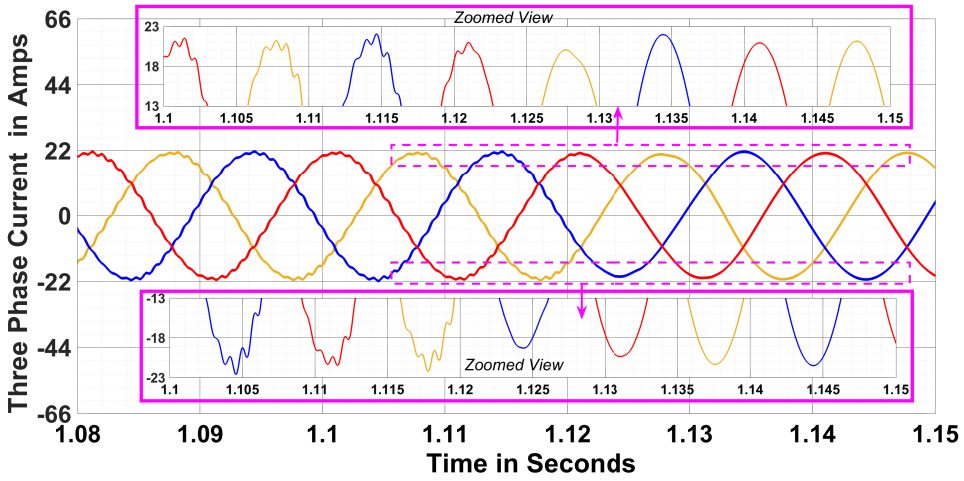
(a) The per-phase grid injected current



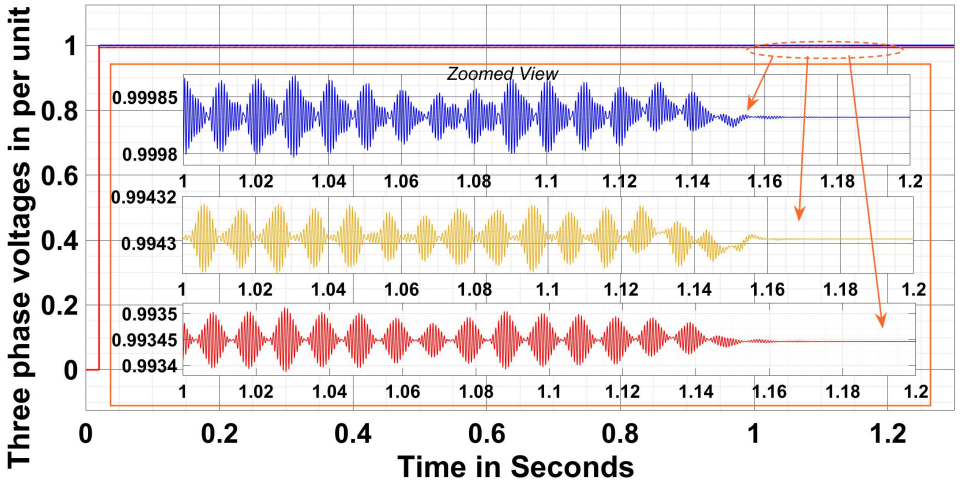
(b) Grid injected Power

Figure 2.20: The solar inverter injection parameters at PCC considering the grid inductance L_g =14mH without and with proposed controller gain characterization

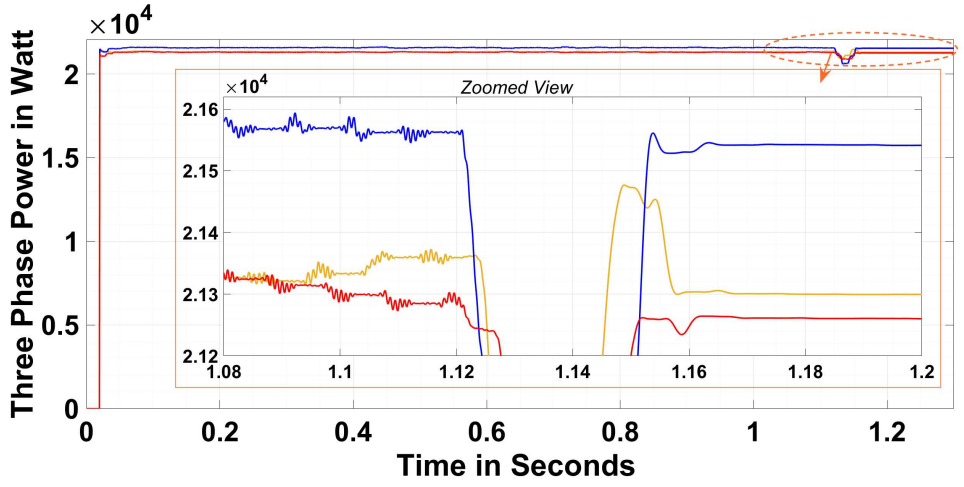
With the initiated controller gain characterization, the grid injected power quality is improved with the achieved current %THD of below 3% as per IEEE-1547(IEEE-519) standards. Further to observe the effect of the proposed controller gain characterization on the solar inverter integrated node (node-13 of Fig.2.19),the three phase current, the per-unit three phase voltage and the three phase power at node-13 considering the unbalance load is presented in Fig.2.21a,Fig.2.21b and Fig.2.21c respectively. From Fig.2.21, it is evident that, the the proposed controller gain characterization is efficient in improving the power quality of the grid injected power in both balanced and unbalanced loading conditions.



(a) Three Phase Current



(b) Three Phase Voltages in Per-unit



(c) Three Phase Power

Figure 2.21: Three Phase Current,voltages and power at node 13

2.5.3 The % THD comparison at different grid inductance with varying controller gains

Finally, the grid injected current %THD variations at PCC for different L_g at $R_g = 48\Omega$ is depicted in Fig.2.22 by varying the K_p value. From the Fig.2.22, it is clearly evident that the computed K_{Po} correspond to L_g using (2.27) is validated to shape the power quality at the PCC as per IEEE-1547 standards.

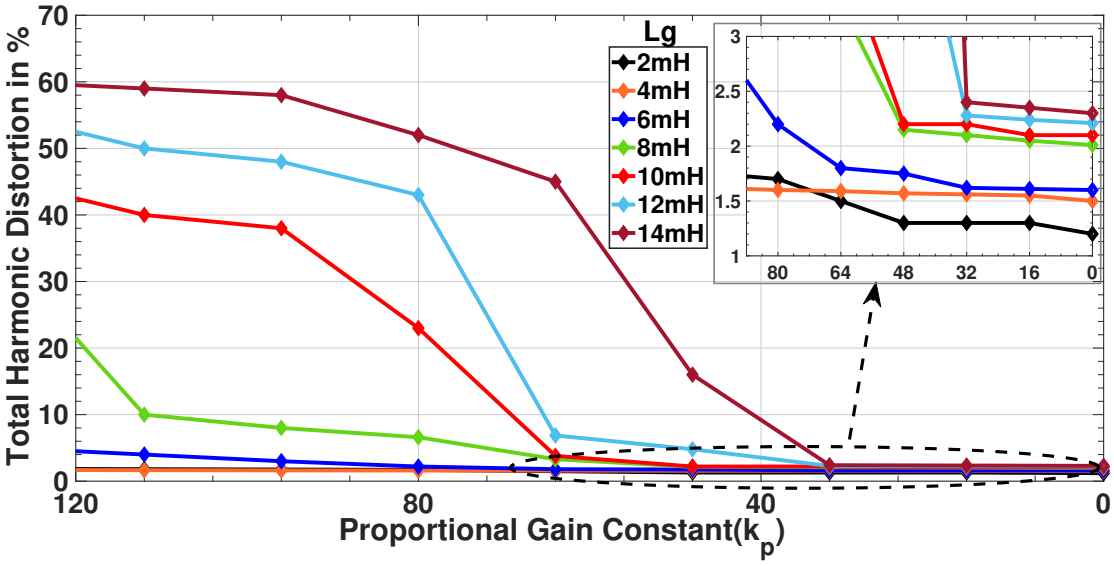


Figure 2.22: The grid injected current %THD variations with varying grid inductance(L_g) and controller gain K_p

2.6 Conclusion

In this work, the grid parameters' effect on the inertial time constant of the grid-connected solar inverter is assessed through mathematical modeling. It is identified that the coupling angle between the real and reactive power due to uncompensated grid inductance exhibit the oscillation in the voltage and current at the PCC with the magnitude directly proportional to the grid inductance. Further, the effect of the coupling angle on the current controller is assessed through phasors and identified that the deviation between the natural and desired inertial time constant coupled through decaying exponential function correspond to natural frequency of the derived impedance model. By observing the phase deviations, the corresponding controller gain has modeled to bring positive damping to the PCC oscillation at various grid inductance's. The modeled controller gain constant corresponds to the grid inductance evaluated critically through simulations and hardware and observed that, with the computed gains at natural frequency of the derived impedance model, the %THD of the grid injected current is always less than 3% as specified by IEEE standards.

Chapter 3

Solar Interfaced Series Inverter with Provision of Common DC bus Grounding

3.1 Series inverter configuration

The proposed solar series inverter configuration consists of two three-phase inverters connected in series through a transformer primary winding. The transformer secondary winding connected to the power network consists of loads, as shown in Fig.3.1. The voltage

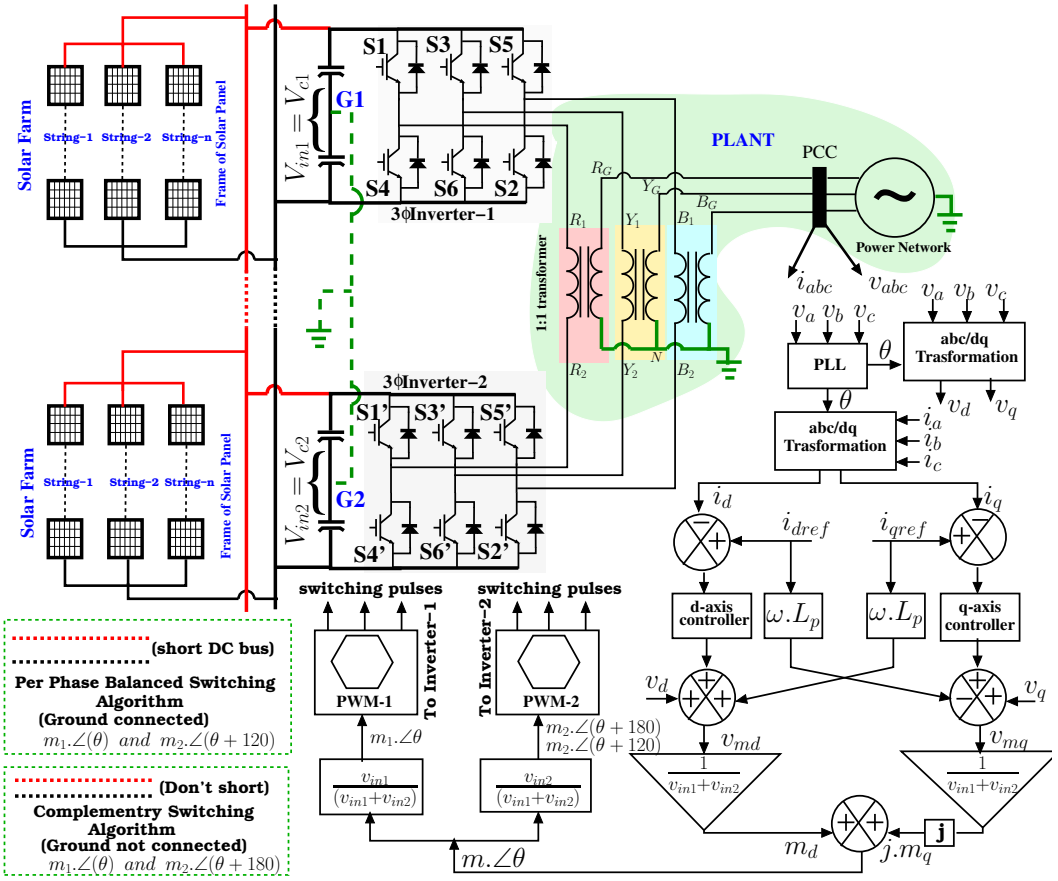
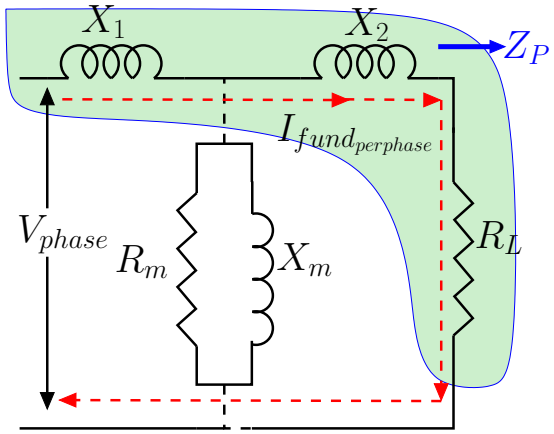


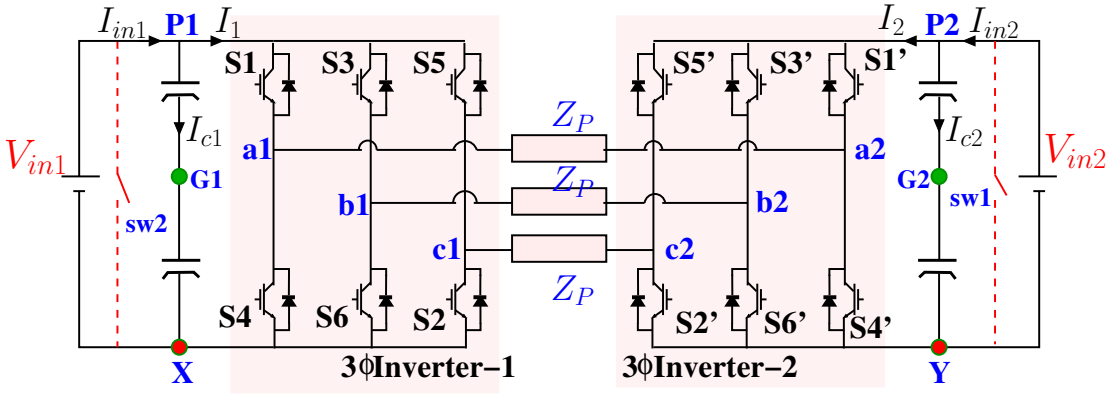
Figure 3.1: Proposed series inverter topology with closed-loop current controller

and fundamental frequency of the plant (transformer and the load) are controlled by the two series inverter through the closed-loop control. The closed-loop controller is modeled

by referring all secondary impedance to the transformer primary with a 1:1 ratio. The translated per phase impedance of the load onto the primary is shown in Fig.3.2a. Here X_1 and X_2 are the primary and secondary impedance of the transformer. R_m and X_m represent the magnetizing resistance and impedance of the core;R_L can be seen as load resistance in islanding mode and virtual resistance (V_g/i_g) in grid connected mode. Here V_g is grid voltage and i_g is grid injected current. By neglecting the core losses and winding



(a)



(b)

Figure 3.2: (a) Equivalent per phase impedance of the plant referring onto the primary of the transformer (b) The equivalent power circuit with per phase equivalent impedance

resistance, the circuit (plant) impedance referred onto the primary side can be expressed as:

$$Z_p(perphase) = R_L + J(X_1 + X_2) \tag{3.1}$$

With translated impedance, the equivalent power circuit of the proposed topology can be viewed as shown in Fig.3.2b. For this configuration, two switching algorithms

1. Complementary switching methodology
2. Per phase balanced switching methodology

are proposed to boost the output voltage and provide DC bus grounding feasibility, unlike

conventional parallel inverters. The parallel inverter performance in terms of DC bus voltage requirement and CMV behavior is presented in the subsequent sub-section and later compared with the proposed topology.

3.1.1 Operational evaluation of conventional parallel inverters

In parallel inverter configuration [26], two inverters are connected in parallel with AC load to share the current. Since two inverters are connected in parallel, the load experience the voltage similar to inverter-1 or inverter-2 as both inverter switch simultaneously with the same switching state. For instance, the inverter-1 switch with switching state 100 (a-phase top switch, b-phase, and c-phase bottom switches of inverter-1 are turn ON), the inverter-2 also switches with the same switching state-100 to share the current. Since the two inverters connected in parallel, the fundamental voltage synthesized across the load using active and null vectors of two inverters shown in Fig.3.3a result in the same voltage magnitude of inverters as depicted in highlighted inner hexagon of Fig.3.3b. In parallel

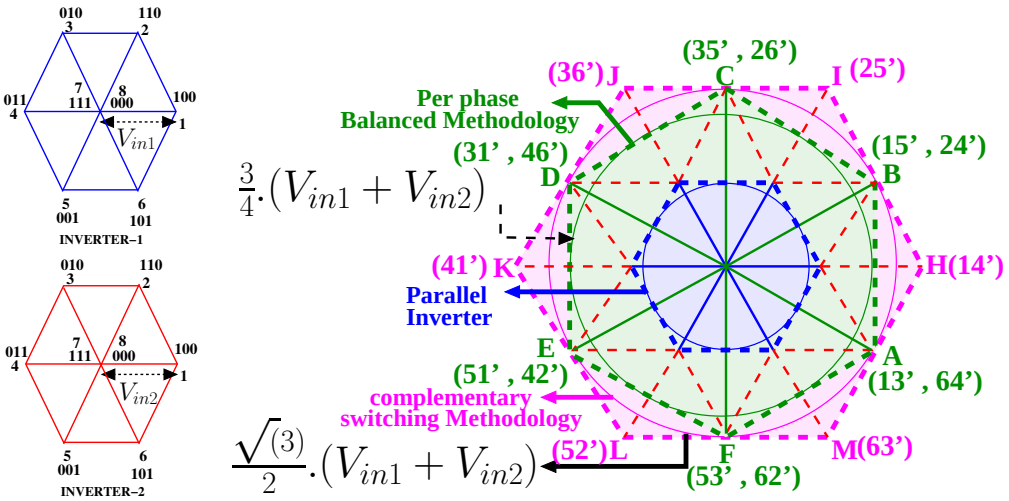


Figure 3.3: (a) Space vector locations of Inverter-1 and Inverter-2 (b) The resultant load space locations of parallel inverter configuration, complementary switching and per phase balanced switching algorithm

inverter configuration, to synthesize 230V AC (per phase RMS), it is required to maintain the minimum of 560V DC (V_{in1}=V_{in2}= 560V) across each inverter. Apart from higher DC bus voltages, the parallel inverters also suffer from the existence of instantaneous CMV. The instantaneous CMV in terms of pole voltages of the inverter can be computed as:

$$V_{CMV} = \frac{v_{a_{xo}} + v_{b_{xo}} + v_{c_{xo}}}{3} \tag{3.2}$$

Here $v_{a_{xo}}$,$v_{b_{xo}}$ and $v_{c_{xo}}$ represent the instantaneous pole voltages of inverter-1 ($x = 1$) and inverter-2 ($x = 2$). Further, to explain the CMV profile intuitively, the CMV appearance with the switching state ’100’ is illustrated in Fig.3.4. The Fig.3.4 illustrate that with the switching state ’100’ of both the inverters, the voltage appears between the DC capacitor

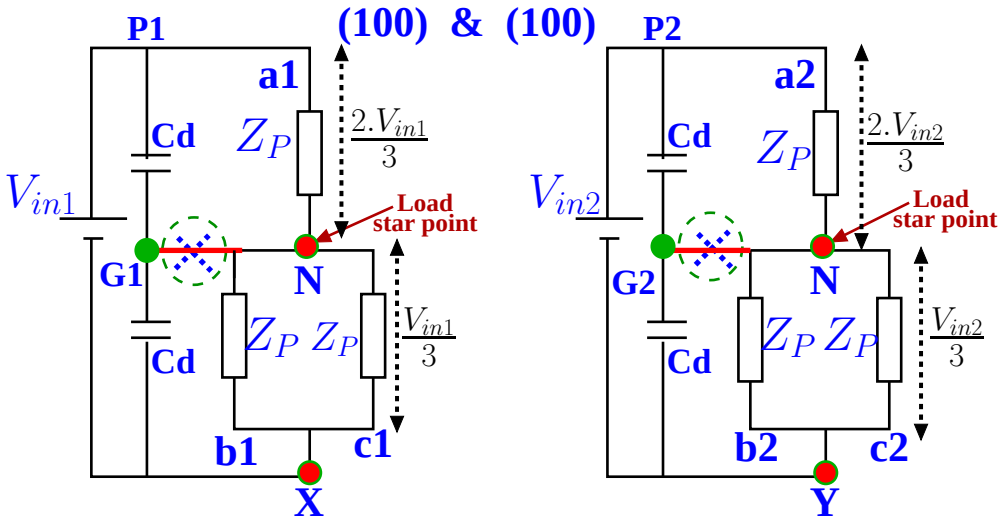


Figure 3.4: The equivalent circuit diagram of parallel inverter with switching state 100 (Inverter-1) and 100 (Inverter-2) to compute CMV

midpoint (G1 or G2) and the load neutral (N) is $V_{in}/6$. Hence the difference in CMV between G1 and G2 is zero, but not concerning ground. From the above discussion, it is evident that with the simultaneous switching, the difference in the common-mode voltages of inverter-1 and inverter-2 is zero gives the flexibility of connecting two inverter DC bus together, assuming ideal switching and identical characteristic impedance of inverters. But it is not possible to connect with the ground due to instantaneous common-mode voltage appear between the inverter negative pole and ground.
Further, to minimize the DC bus potential and CMV elimination, the two PWM techniques are illustrated in the following subsections for the series solar inverter configuration.

3.1.2 The series configuration with Complementary switching

In the proposed configuration shown in Fig.3.2a with the complementary switching algorithm, the two inverters are switched with 180°degree apart to realize the resultant voltage across the load. For instance, inverter-1 is switching with active switching vector 1 (100), and inverter-2 made operate to switch with the switching vector 4 (011) depicted in space locations shown in Fig.3.3a. With the adopted switching states, the resultant load space vector location is at 14' shown in Fig.3.3b. With the selection of active vectors of inverter-1 and inverter-2 of series inverter configuration, the resultant load space locations can be derived as:

$$\begin{aligned}\overrightarrow{V_{load}} = &(s_{a1}V_{a1G1}e^{j0} + s_{b1}.V_{b1G1}e^{j120} + s_{c1}.V_{c1G1}e^{j240}) \\ &- (s_{a2}V_{a2G2}e^{j0} + s_{b2}.V_{b2G2}e^{j120} + s_{c2}V_{c2G2}e^{j240})\end{aligned} \tag{3.3}$$

Here s_{a1}, s_{b1}, s_{c1} and s_{a2}, s_{b2}, s_{c2} are the a-phase, b-phase, c-phase switching states of inverter-1 and inverter-2 respectively. The corresponding pole voltages of inverter-1 and inverter-2 are defined as V_{a1G1}, V_{b1G1} V_{c1G1} and V_{a2G2} V_{b2G2} V_{c2G2}. The operating

trajectory of the resultant load voltage with the complementary switching can be identified from Fig.3.3b as outer hexagon (HIJKLM). From load voltage profile, it is evident that, with the complementary switching the proposed topology yield double the voltage across the load compare to conventional parallel inverter topology. Therefore, the DC bus required to generate the necessary phase voltage of 230V RMS is half compared to the conventional parallel inverter (V_{in1}=V_{in2} =560/2 V). The possible switching locations derived from the two inverters using complementary switching is tabulated in Table-3.1 to synthesize the fundamental voltage across the load. Further, the CMV behavior of

Table 3.1: The proposed solar inverter switching combinations, corresponding resultant load space vector and CMV profile

Complementary Switching Methodology							Per Phase Balanced Switching Methodology						
Switching	Inv-1	Inv-2	Resultant	Equivalent CMV		I_{cir}	Switching	Inv-1	Inv-2	Resultant	Equivalent CMV		I_{cir}
instance	SW	SW	Voltage	Inv-1	Inv-2	current	instance	SW	SW	Voltage	Inv-1	Inv-2	current
14'	100	011	$2.V_{in}\angle 0$	$\frac{-V_{in}}{6}$	$\frac{V_{in}}{6}$	$\frac{-V_{in}}{Z_P}$	13'	100	010	$\frac{\sqrt{3}}{2}2.V_{in}\angle 330$	0	0	0
25'	110	001	$2.V_{in}\angle 60$	$\frac{V_{in}}{6}$	$\frac{-V_{in}}{6}$	$\frac{V_{in}}{Z_P}$	15'	100	001	$\frac{\sqrt{3}}{2}2.V_{in}\angle 30$	0	0	0
36'	010	101	$2.V_{in}\angle 120$	$\frac{-V_{in}}{6}$	$\frac{V_{in}}{6}$	$\frac{-V_{in}}{Z_P}$	35'	010	001	$\frac{\sqrt{3}}{2}2.V_{in}\angle 90$	0	0	0
41'	011	100	$2.V_{in}\angle 180$	$\frac{V_{in}}{6}$	$\frac{-V_{in}}{6}$	$\frac{V_{in}}{Z_P}$	31'	010	100	$\frac{\sqrt{3}}{2}2.V_{in}\angle 150$	0	0	0
52'	001	110	$2.V_{in}\angle 240$	$\frac{-V_{in}}{6}$	$\frac{V_{in}}{6}$	$\frac{-V_{in}}{Z_P}$	51'	001	100	$\frac{\sqrt{3}}{2}2.V_{in}\angle 210$	0	0	0
63'	101	010	$2.V_{in}\angle 300$	$\frac{V_{in}}{6}$	$\frac{-V_{in}}{6}$	$\frac{V_{in}}{Z_P}$	53'	001	010	$\frac{\sqrt{3}}{2}2.V_{in}\angle 270$	0	0	0

the series configuration with the complementary switching algorithm, the instantaneous switching states of 1 "100" (inverter- 1) and 4' "011" (inverter-2) taken as a switching instance for the explanation.With the switching state 14', the switching pattern of the proposed configuration and corresponding load current paths are shown in Fig.3.5. The equivalent circuit is drawn using Fig.3.5 to compute individual CMV of inverter-1 and inverter-2 by shorting sw1 and sw2, respectively. The equivalent circuit shown in Fig.3.6(a) is drawn using the superposition principle to identify the CMV of inverter-1 and inverter-2 with reference to each other. The left trace of Fig.3.6(a) shows that inverter-1 is switching with 1(100), and inverter-2 DC bus is shorted to compute the CMV. With this switching instance, the computed voltage across the virtual neutral point ($Y - G1$) is $(-)V_{in1}/6$. Similarly, after applying the superposition theorem for the inverter-2 with switching state 4 (011), the equivalent circuit appears to be seen in the right trace of Fig.3.6(a) and CMV appears at ($X - G2$) is $(+)V_{in2}/6$. The unequal instantaneous CMV voltage appears across point Y (representing inverter-2) and X (representing inverter-1) to DC negative demand isolated DC bus for two inverters to cease the circulating current.With the isolated DC bus, the magnitude of the three-phase load current (I_{abc}) with the switching instance 14' is shown in the Fig.3.7a. But in case mid point of the capacitors in both inverter (G1 and G2) connected together, the circulating current pattern concerning the Fig.4.1 is shown in the Fig.3.7b. The magnitude of the circulating current for the proposed configuration can be computed as

$$I_{cir} = (s_{a1} - s_{a2})(i'_a - i_a) + (s_{b1} - s_{b2})(i'_b - i_b) + (s_{c1} - s_{c2})(i'_c - i_c) \tag{3.4}$$

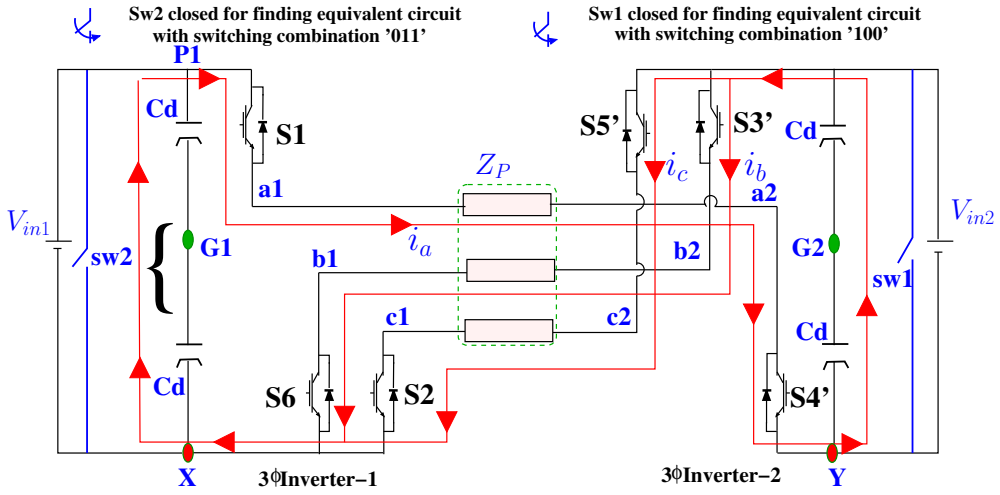


Figure 3.5: The operational state of proposed configuration with switching state 14'

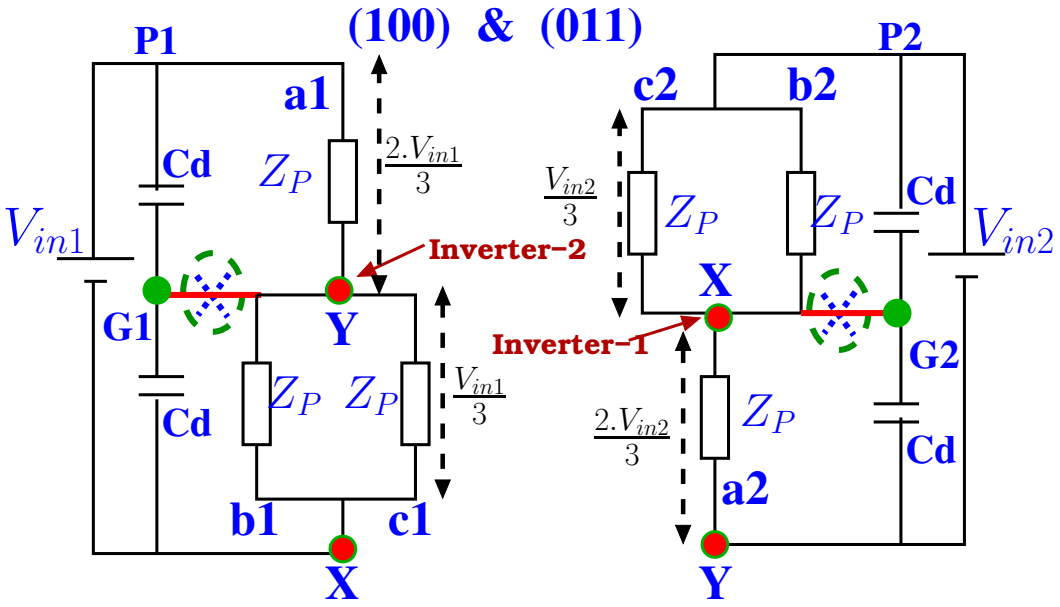
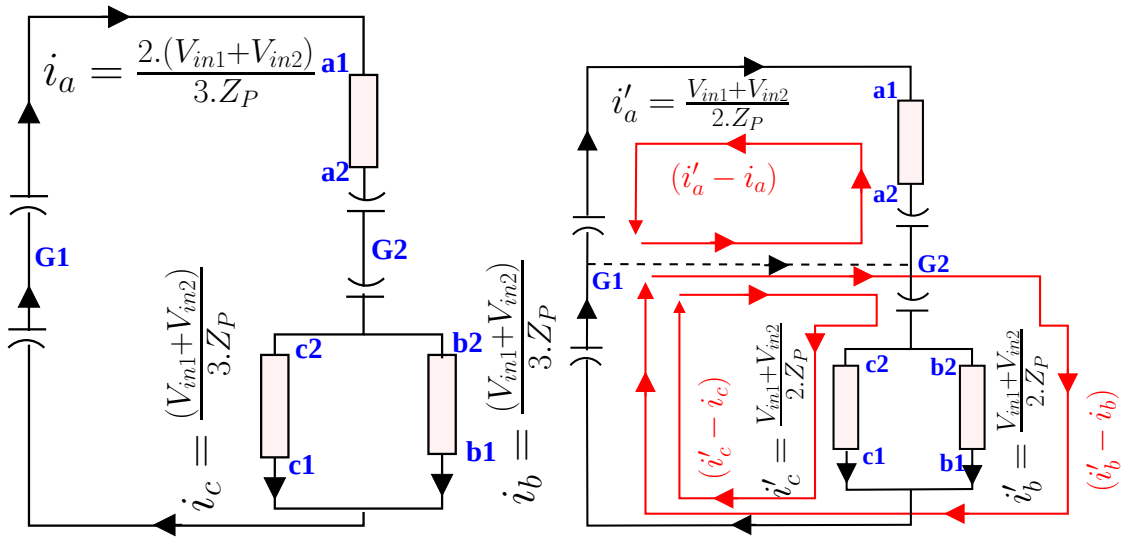


Figure 3.6: The equivalent circuit of proposed configuration with switching state 1 '100' (Inverter-1) and 4' '011' (inverter-2) to compute CMV

i'_a is the a-phase current after shorting the DC bus, i_a is the a-phase current before shorting the DC bus. $i'_a - i_a$ represents the circulating current in a-phase, $(i'_b - i_b)$ represents the b-phase, $(i'_c - i_c)$ represents the c-phase circulating current,respectively. For the switching instance 14' the circulating current can be computed as $-\frac{V_{in1}+V_{in2}}{2Z_p}$. Similarly, the resultant CMV and corresponding circulating current magnitudes for the possible complementary switching combinations are tabulated in Table-3.1. From the CMV profile, it is evident that it is always advised to maintain the isolated DC bus to cease the circulating current with the complementary switching. With per phase switching algorithm proposed in this work for series inverter, the instantaneous CMV can be nullified as explained in the subsequent section.



(a) Without shorting the G1 and G2 (b) With shorting the G1 and G2

Figure 3.7: The load current and the circulating current path of the proposed converter with switching state 14'

3.1.3 The series configuration with per phase balanced switching algorithm

In the case of per-phase balanced switching methodology [57], unlike parallel inverters and complementary switching algorithm, the two inverters are switched 120° apart. For instance, inverter-1 is switched with the switching state 1(100), the inverter-2 is switched with the switching state- 3 (010) (+120°) or 5 (001) (-120°) (Fig.3.3(a)). With the devised switching states, the load voltage space location can be computed using (3.3) as A (13') or B (15') depicted in Fig.3.3(b). The possible switching states with per phase balanced switching algorithm of both the inverter and corresponding resultant load space locations are tabulated in Table-3.1 and corresponding trajectory (ABCDEF) is depicted in Fig.3.3(b). With the per phase switching algorithm, the resultant load voltage boost can be seen through the Fig.3.3(b) that the load voltage trajectory ABCDEF lies between the parallel inverter (42% higher) and the complementary switching algorithm with proposed topology (14% lower). Therefore to generate the 230V AC (RMS) it is required to maintain the DC bus voltage of 325V (V_{in1}= V_{in2}= 325V). With the switching state 13', the switching pattern of proposed configuration and corresponding load current paths are shown in Fig.3.8. The equivalent circuit is drawn using Fig.3.8, similar to the complementary switching algorithm to compute individual CMV of inverter-1 and inverter-2 by shorting $SW1$ and $SW2$, respectively. With the mentioned switching states, the resultant circuit to compute CMV is as shown in Fig.3.9(a). From Fig.3.9(a) it is evident that the voltage appears between Y-G1 (Inverter-1) and X-G2 (Inverter-2) is zero, Similarly for all possible switching states tabulated in Table-3.1, the CMVs are zero. With this, it is clear that the per phase balanced switching algorithm with devised switching combinations gives the flexibility of connecting the DC bus to the ground. Since the CMV

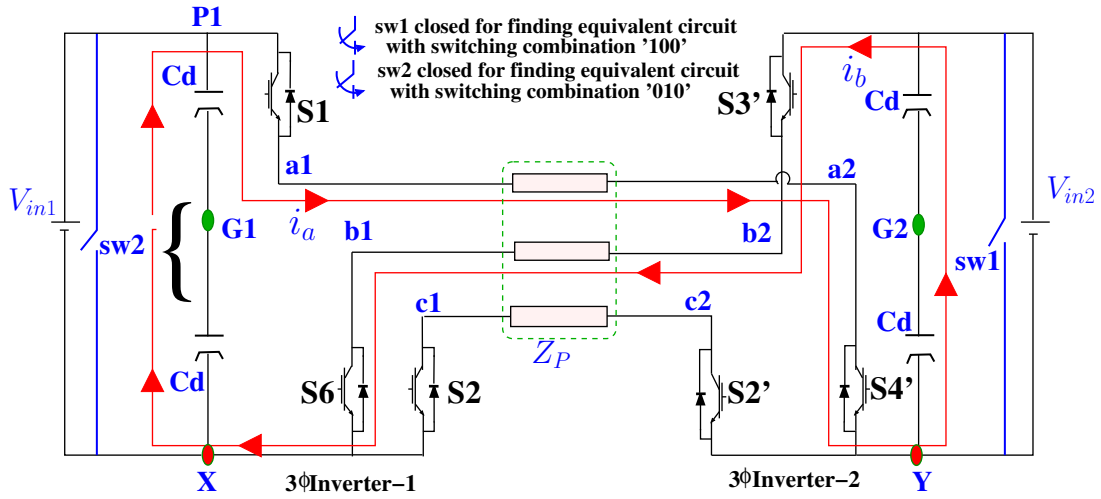


Figure 3.8: The operational state of proposed configuration with switching state 13'

is zero for all switching combinations, the circulating current appears to be zero even with the common DC bus (joining X and Y) as shown in Table-3.1.For a switching instance 13', currents flowing through the load with and without shorting the DC bus is shown in Fig.3.10. From the Fig.3.10 it is evident that the magnitude of the current flowing in the load phases remains same in both the cases (with and without shorting the DC bus) indicates the complete elimination of the CMV.

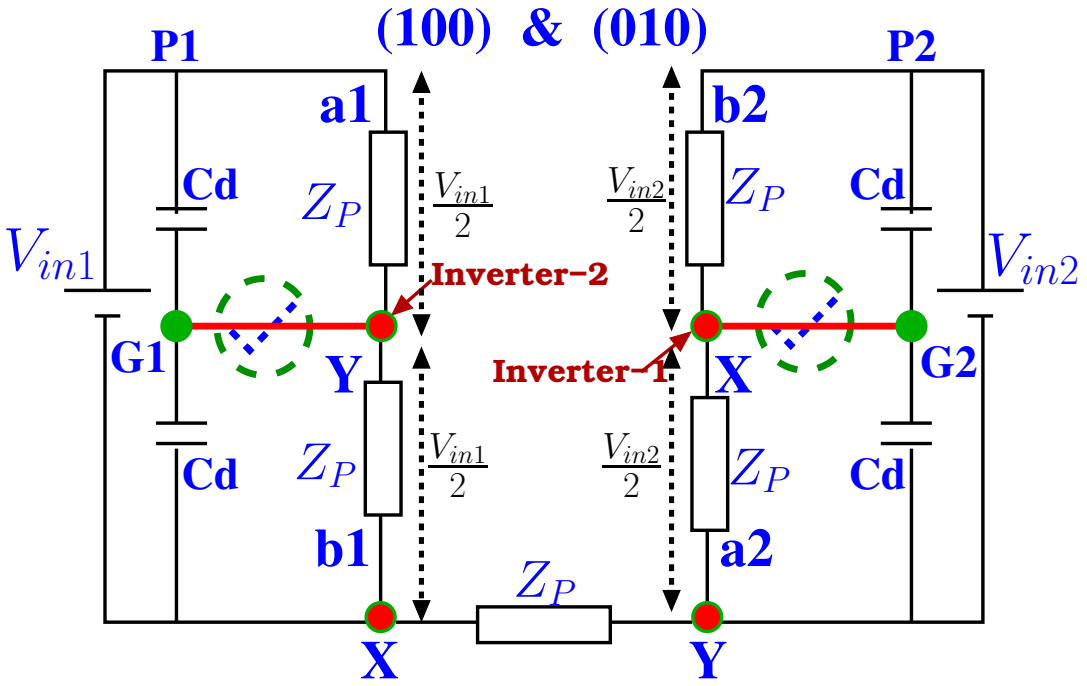
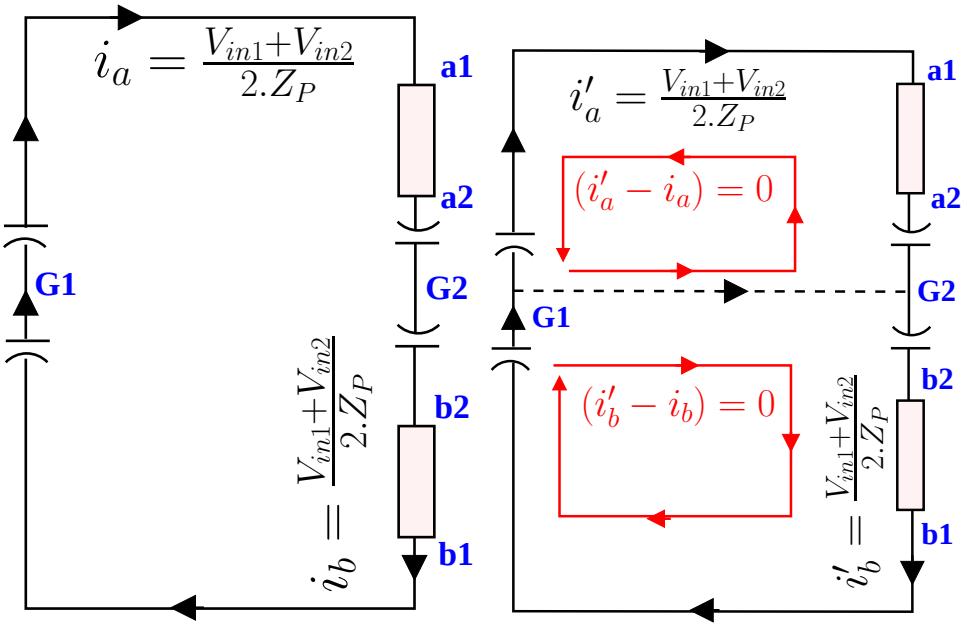


Figure 3.9: The equivalent circuit of proposed configuration with switching state 1 '100' (Inverter-1) and 3' '010' (inverter-2) to compute CMV

From the preceding discussion, it is clear that the circulating current experienced by the load is zero with the complementary switching algorithm and the per phase balanced switching algorithm by maintaining isolated DC bus and common DC bus, respectively.



(a) Without shorting the G1 and G2 (b) With shorting the G1 and G2

Figure 3.10: The load current and the circulating current path of the proposed converter with switching state 14'

The closed-loop current controller is designed for the proposed series configuration, as explained in the subsequent section.

3.1.4 Closed-loop current controller design through state space analysis

To model the closed-loop controller for the proposed configuration, the plant impedance derived in (3.1) can be rearranged in terms of real (R_P) and imaginary parts (L_P) as:

$$Z_P = R_P + j.w.L_P; Where\ R_P = R_L; L_P = (L_1 + L_2)$$

The three-phase voltages can be written concerning the simplified per-phase impedance line diagram shown in Fig.3.11 as:

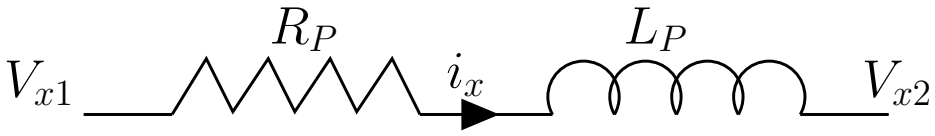


Figure 3.11: Simplified per phase impedance of the plant

$$V_{x_1x_2} = R_P.i_x + L_P.\frac{di_x}{dt};\quad where\quad x = a, b, c \tag{3.5}$$

Where $V_{a_1a_2} = (d_a.V_{in1} + d'_a.V_{in2}); V_{b_1b_2} = (d_b.V_{in1} + d'_b.V_{in2}); V_{c_1c_2} = (d_c.V_{in1} + d'_c.V_{in2});$ $V_{a_1a_2}, V_{b_1b_2}$ and $V_{c_1c_2}$ are the inverter phase voltages. d_a, d_b, d_c and d'_a, d'_b, d'_c are the instantaneous duty ratio of the switch in a phase-leg of inverter-1 and inverter-2 respectively, i_a, i_b and i_c are phase currents of a-phase, b-phase and c-phase respectively.

Further, the phase voltages and currents can be transformed to the synchronous reference frame to obtain the plant model in dq reference frame as:

$$V_d = \frac{3}{2}[V_{a_1a_2}cos(\theta) + V_{b_1b_2}cos(\theta - 120) + V_{c_1c_2}cos(\theta + 120)] \tag{3.6}$$

$$V_q = \frac{-3}{2}[V_{a_1a_2}sin(\theta) + V_{b_1b_2}sin(\theta - 120) + V_{c_1c_2}sin(\theta + 120)] \tag{3.7}$$

$$i_d = \frac{3}{2}[i_acos(\theta) + i_bcos(\theta - 120) + i_ccos(\theta + 120)] \tag{3.8}$$

$$i_q = \frac{-3}{2}[i_asin(\theta) + i_bsin(\theta - 120) + i_csin(\theta + 120)] \tag{3.9}$$

The current variations with time in the synchronous reference frame can be written by taking the time derivative of the load current represented in (4.9) and (4.10) as:

$$\frac{di_d}{dt} = \frac{3}{2}[(\frac{V_{a_1a_2}}{L_P} - \frac{R_P}{L_P}i_a)cos(\theta) + (\frac{V_{b_1b_2}}{L_P} - \frac{R_P}{L_P}i_b) \\ cos(\theta - 120) + (\frac{V_{c_1c_2}}{L_P} - \frac{R_P}{L_P}i_c)cos(\theta + 120) + w.i_q] \tag{3.10}$$

$$\frac{di_q}{dt} = -\frac{3}{2}[(\frac{V_{a_1a_2}}{L_P} - \frac{R_P}{L_P}i_a)sin(\theta) + (\frac{V_{b_1b_2}}{L_P} - \frac{R_P}{L_P}i_b) \\ sin(\theta - 120) + (\frac{V_{c_1c_2}}{L_P} - \frac{R_P}{L_P}i_c)sin(\theta + 120) - w.i_d] \tag{3.11}$$

The (3.10) and (3.11) can be simplified further using (4.7) and (4.8) as:

$$\frac{di_d}{dt} = \frac{V_d}{L_P} - \frac{R_P}{L_P}i_d + w.i_q \tag{3.12}$$

$$\frac{di_q}{dt} = \frac{V_q}{L_P} - \frac{R_P}{L_P}i_q - w.i_d \tag{3.13}$$

The (4.13) and (4.14) represent the rate of change of plant current (state variable) in dq-domain. In the proposed series configuration, the current flowing through the plant is equal to the load current. To obtain the system state-space model, in this work, the input voltages of inverters (V_{in1}=V_{c1} and V_{in2}= V_{c2}) is also considered as a state variable along with the plant current. The input voltage of the individual inverters is the function of individual inverter input currents (I_{in1} and I_{in2}) and the value of DC capacitance connected across the individual DC bus. As it shown in Fig.3.2b, the DC input current is summation of load current and capacitor current. Further the capacitor currents ((I_{c1} and I_{c2})) of inverter-1 and inverter-2 can be expressed in terms of three-phase currents (i_a, i_b *and* i_c) and instantaneous duty as:

$$I_{in1} = I_1 + I_{c1} \quad : \quad I_{in2} = I_2 + I_{c2} \tag{3.14}$$

$$I_{c1} = -(d_a.i_a + d_b.i_b + d_c.i_c) + I_{in1} \tag{3.15}$$

$$I_{c2} = -(d'_a.i_a + d'_b.i_b + d'_c.i_c) + I_{in2} \tag{3.16}$$

The (3.15) and (3.16) in synchronous reference frame can be represented as :

$$I_{c1} = -\frac{3}{2}(d_d.i_d + d_q.i_q) + I_{in1} \tag{3.17}$$

$$I_{c2} = -\frac{3}{2}(d'_d.i_d + d'_q.i_q) + I_{in2} \tag{3.18}$$

Using (3.17) and (3.18) the input (capacitor) voltage variations with respect time can be modeled in dq domain as:

$$\frac{dV_{c1}}{dt} = \frac{1}{C_{dc}}[-\frac{3}{2}(d_d.i_d + d_q.i_q) + I_{in1}] \tag{3.19}$$

$$\frac{dV_{c2}}{dt} = \frac{1}{C_{dc}}[-\frac{3}{2}(d'_d.i_d + d'_q.i_q) + I_{in2}] \tag{3.20}$$

Here dV_{c1}/dt and dV_{c2}/dt represent the rate of change in the input voltage state variable. C_{dc} represents the DC capacitance for inverter-1 and Inverter-2 (assumed equal for both the inverters). d_d, d'_d, d_q and d'_q represents the instantaneous duty of Inverter-1 and Inverter-2 in dq domain respectively. Further to obtain the steady state duty of the two inverters, the rate of change of state variables presented in (4.13), (4.14), (4.15) and (3.20) made equal to zero. At the steady state the average duty for both the inverters and the output current can be obtained as:

$$V_d = (d_d.V_{in1} + d'_d.V_{in2}) \; ; \; V_q = (d_q.V_{in1} + d'_q.V_{in2}) \tag{3.21}$$

$$where \quad V_{in1} = V_{c1} \quad ; \quad V_{in2} = V_{c2}$$

$$D_d = \sqrt{\frac{2.R_P.I_{in1}}{3.V_{in}}} \quad ; \quad D'_d = \sqrt{\frac{2.R_P.I_{in2}}{3.V_{in}}} \tag{3.22}$$

$$D_q = \frac{2.I_{in1}.L_P}{3.V_{in}.D_d} \quad ; \quad D'_q = \frac{2.I_{in2}.L_P}{3.V_{in}.D'_d} \tag{3.23}$$

$$i_d = \frac{2.I_{in1}}{3.d_d} = \frac{2.I_{in2}}{3.d'_d} \tag{3.24}$$

Here V_d and V_q are the combined input voltage of the plant in dq-domain. With the identified state variables, the states space equation can be written as:

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{3.25}$$

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \\ \frac{dV_{c1}}{dt} \\ \frac{dV_{c2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_P}{L_P} & w & \frac{d_d}{L_P} & \frac{d'_d}{L_P} \\ -w & -\frac{R_P}{L_P} & \frac{d_q}{L_P} & \frac{d'_q}{L_P} \\ -\frac{3.d_d}{2.C_{dc}} & -\frac{3.d_q}{2.C_{dc}} & 0 & 0 \\ -\frac{3.d'_d}{2.C_{dc}} & -\frac{3.d'_q}{2.C_{dc}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ V_{c1} \\ V_{c2} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_P} & 0 & 0 & 0 \\ 0 & \frac{V_{in}}{L_P} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{dc}} & 0 \\ 0 & 0 & 0 & \frac{1}{C_{dc}} \end{bmatrix} \begin{bmatrix} d_d + d'_d \\ d_q + d'_q \\ I_{in1} \\ I_{in2} \end{bmatrix} \tag{3.26}$$

$$y(t) = Cx(t) + Du(t) \tag{3.27}$$

$$\begin{bmatrix} V_{in1} \\ V_{in2} \\ i_{od} \\ i_{oq} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ V_{c1} \\ V_{c2} \end{bmatrix} \tag{3.28}$$

Here i_{od} and i_{oq} represent the load current in dq domain. With the defined state space equation in (4.18) and (4.20), the proposed system transfer function matrix can be computed as: $y(s) = [C(SI - A)^{-1}B + D]u(s) = G.u(s)$

$$\begin{bmatrix} V_{in1} \\ V_{in2} \\ i_{od} \\ i_{oq} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} & G_{13} & G_{14} \\ G_{21} & G_{22} & G_{23} & G_{24} \\ G_{31} & G_{32} & G_{33} & G_{34} \\ G_{41} & G_{42} & G_{43} & G_{44} \end{bmatrix} \begin{bmatrix} (d_d + d'_d) \\ (d_q + d'_q) \\ I_{in1} \\ I_{in2} \end{bmatrix}$$

Here $y(s)$ is the output matrix, G is system transfer function matrix, $u(s)$ is input matrix. With the identified transfer function matrix, the equivalent dynamic network model of the proposed configuration can be viewed as shown in Fig.3.12. In this work, the current controller for the proposed configuration is designed by understanding output current variations to the inverter duty and the input voltage. The G_{31} and G_{42} represent the plant's transfer function concerning load current variations. The small-signal model of the current loop in dq-domain is shown in Fig.3.13.

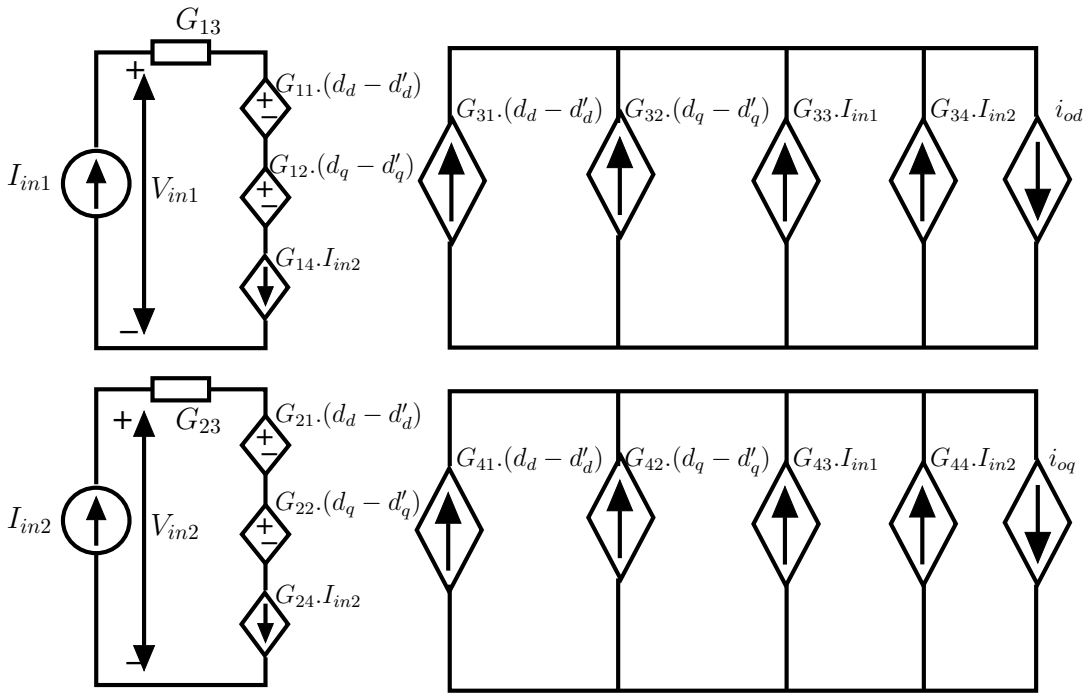


Figure 3.12: Dynamic network model of proposed configuration derived from state space model

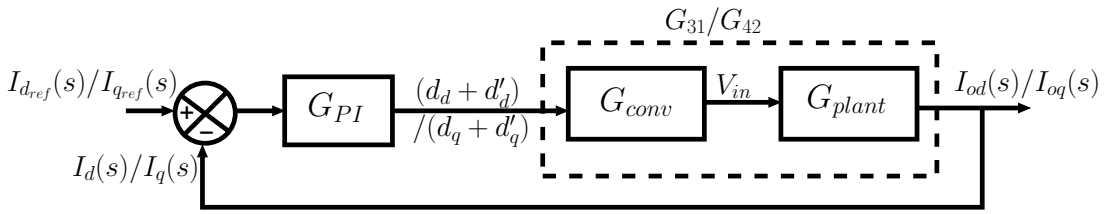


Figure 3.13: Small signal model of inverter to design the controller in dq-domain

For ease in explanation of controller design here it is assumed $V_{in1} = V_{in2} = V_{in}$.

$$G_{conv} = \frac{v_{in}}{(d_d + d'_d)}(in\ d-loop); = \frac{v_{in}}{(d_q + d'_q)}(in\ q-loop)$$

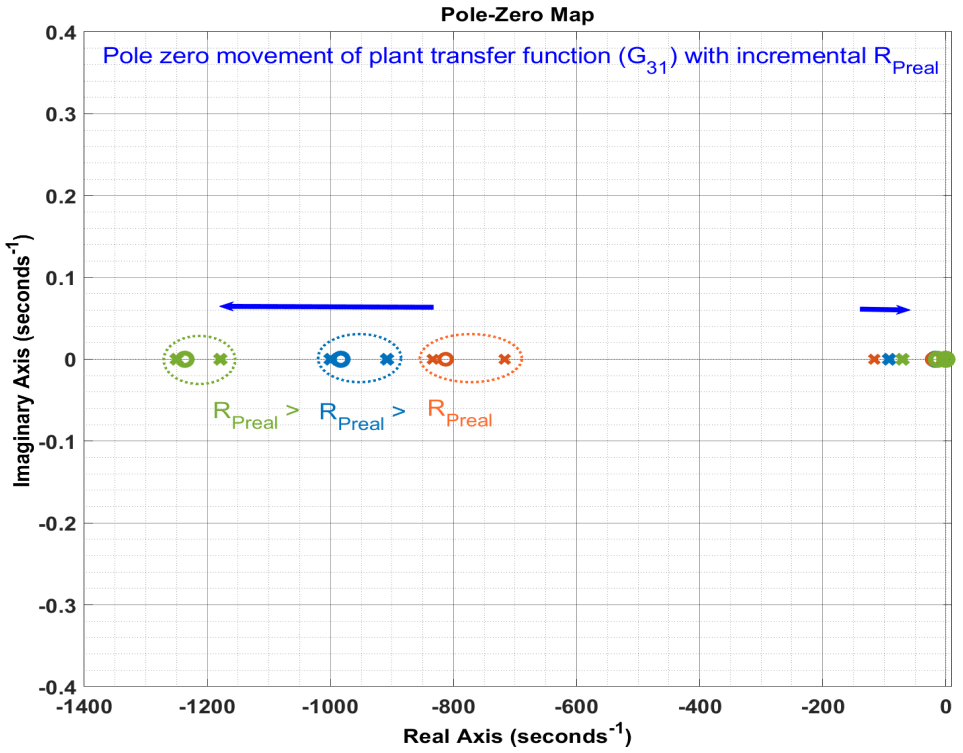
$$G_{plant} = G_{31}(in\ d-loop);\quad G_{42}(in\ q-loop);$$

$$G_{PI}(s) = K_P + \frac{K_I}{s} = \frac{K_P}{s}.(s + \frac{K_I}{K_P}) \tag{3.29}$$

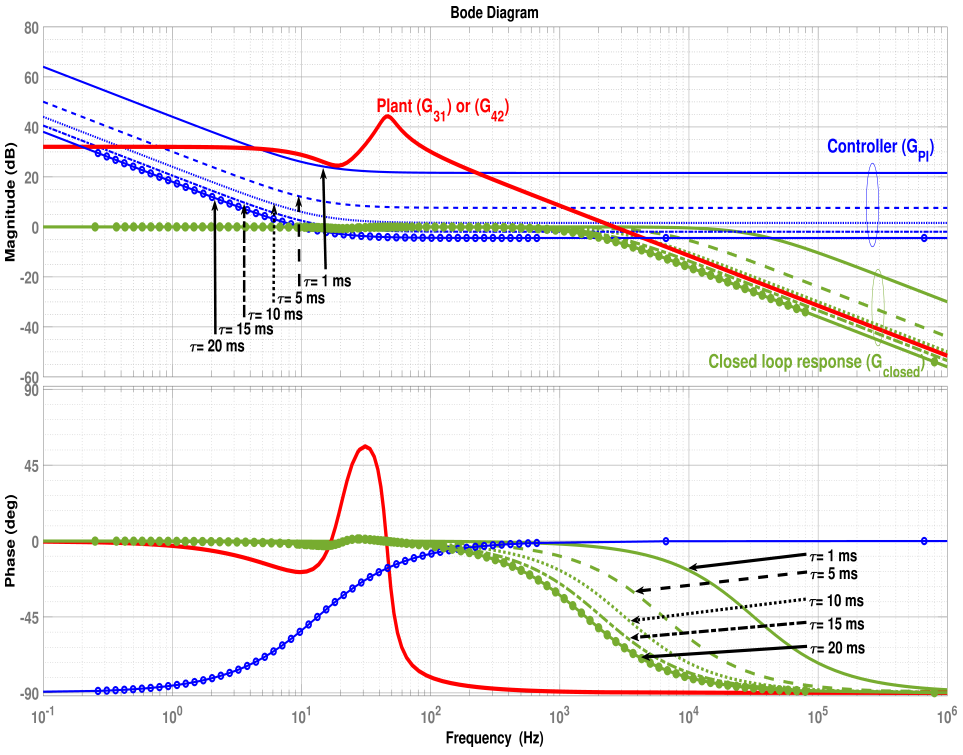
$$G_{open} = G_{PI}.G_{Conv}.G_{plant} \tag{3.30}$$

The pole-zero location of the plant G_{31} with the variation of the load is plotted in Fig.3.14(a). It can be observed from Fig.3.14(a) that the plant G_{31} contains 4 poles and 3 zeros at a specific load. By applying the pole-zero cancellation depending upon the proximity of the pole-zero pair, the G_{31} can be simplified to $\frac{1}{L_P s + R_P}$. With this, the open-loop transfer function can be written as:

$$G_{open} = \frac{K_P}{s}.(s + \frac{K_I}{K_P}).(\frac{1}{L_P s + R_P}) \tag{3.31}$$



(a)



(b)

Figure 3.14: (a) The pole zero location of the plant G_{31} with varying load R_P (b) Frequency response of the plant, controller and closed-loop response of the proposed configuration with varying τ

With the simplified open-loop transfer function, the values of proportional gain (K_P) and

Integral gain (K_I) cab be derived as:

$$K_P = \frac{L_P}{\tau}; K_i = \frac{R_P}{L_P}.K_P; \tau = \frac{L_P}{K_P}; \tag{3.32}$$

τ is the time constant that defines the proposed configuration's desired response in the closed-loop. The bode plot for the closed-loop system with varying τ is depicted in Fig.3.14(b). From the Fig.3.14(b) it is evident that the system is stable throughout the frequency sweep and the controller gain τ (from (3.32)) and corresponding K_P decides the dynamic response of the system.

3.2 Results and Discussions

The hardware prototype of the proposed series solar inverter shown in Fig.3.1 is implemented along with closed-loop control.In hardware set up, each leg of two inverters built with the semikron make IGBT module (SKM75GB12T4) that consist of two IGBT switches (upper and lower) in each module. The gating pulses for each leg is derived through closed-loop control implemented on the C2000 DSP controller (F28379D). Three-phase voltage and three-phase currents are sensed at the point of common coupling (secondary of the transformer) through hall effect based voltage (LV25P) and current (LA55P) sensors to implement the closed-loop control. The lab interface transformer (1:1) having a leakage inductance of 0.21 mH, parallel branch magnetizing inductance (L_m) 8.1H and magnetizing resistance (R_m) is 2645Ω is used in series with two inverter as shown in Fig.3.1. The experiments are conducted by deriving the reference angle θ through a voltage phase-locked loop (PLL). The complete experimental setup is shown in Fig.3.15 and the operating parameters are tabulated in Table.3.2 On the C2000 DSP

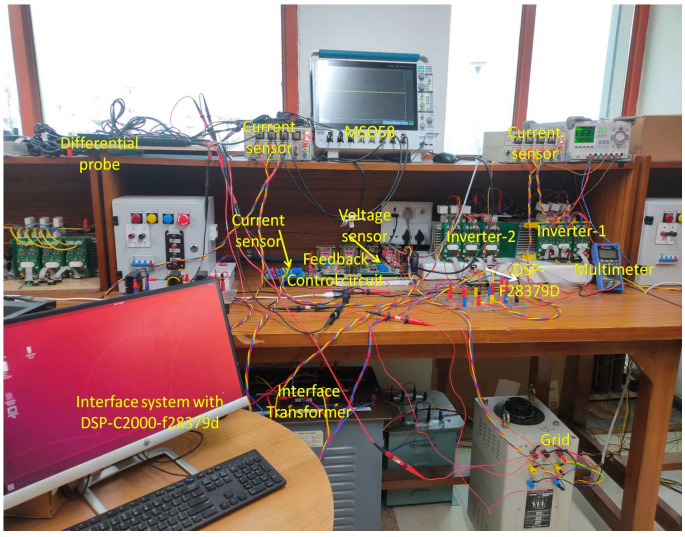


Figure 3.15: Lab hardware prototype of proposed configuration

board, the current controller for desired dynamic response is implemented using the small signal model described in the preceding section. With the designed closed-loop controller,

Table 3.2: Experimental operating parameters of proposed series inverter

Parameter	Value	Units
Power (P)	1.8	kW
DC operating voltage (V_{in1} and V_{in2})	200	Volts
Grid voltage (L-L (RMS)) (V_g)	250	Volts
Fundamental Frequency (f_s)	50	HZ
Switching Frequency (f_{sw})	10	kHZ
AC filter Inductance (L_1=L_2)	3	mH
Leakage inductance(X_1=X_2)(1:1 transformer)	0.21	mH

complementary switching and per phase balanced switching algorithms are used to derive the gating pulses for the modular inverters of the proposed configuration.

In the complementary switching algorithm, two isolated DC bus voltage magnitude of 200 V (($V_{in1} = V_{in2} = 200V$)) are used for each inverters. The corresponding a-phase pole voltages of inverter-1 and inverter-2 are varying between (+/-) 100 shown in the top two traces Fig.3.16.With the two isolated DC buses, the phase voltage appears across the primary of the transformer is shown in the middle trace of Fig.3.16 varying in 5 steps between (+/-)267V, (+/-) 133V, and 0V depending upon the switching states of the series inverters. Whereas in the case of conventional parallel inverters, to obtain the same phase voltage of the load, it is necessary to maintain 400 V DC bus across both the inverters. It is evident that the proposed topology yield double the voltage that of parallel inverter topology with complementary switching algorithm. The CMV's existence between the two inverters is shown in the 4^{th} trace of Fig.3.16. Therefore the isolated DC buses are advised to cease the circulating current. With the isolated DC bus, the three-phase current flowing through the plant is sinusoidal as shown in the bottom trace of Fig.3.16 confirms the CMV trapped between the capacitors midpoint. The per-phase switching algorithm proposed in this work to remove the circuit's CMV is illustrated in Fig.3.17. The first two traces of the Fig.3.17 shows the pole voltages of inverter-1 and inverter-2 varying between (+/-)100, similar to complementary switching algorithm.The third trace represents the a-phase primary voltage of the transformer indicates the direct summation of pole voltages (V_{in1}+V_{in2}) varying between +200V, -200V, and 0V. The magnitude of the phase voltages indicates that with the proposed per phase balance algorithm, the achieved boost across the transformer's primary is 42% higher than the conventional parallel inverter and 14% lesser than the complementary switching algorithm. The 4^{th} trace of the Fig.3.17 shows the CMV profile between the midpoint of the two capacitors of the proposed configuration. Since the CMV is zero, the two inverters are connected to a common DC bus (mid point of the capacitors of inverter-1 and inverter-2 shorted), and corresponding three-phase currents are shown in the bottom trace of Fig.3.17. The three-phase current in the transformer's primary is pure sinusoidal confirms the no circulating current flowing between the inverters even after connecting the DC bus of two inverters. With effective elimination of the circulating current through per phase balanced switching algorithm, the DC bus of the proposed configuration can be grounded effectively.

The small-signal model described in the preceding section to design the closed-loop

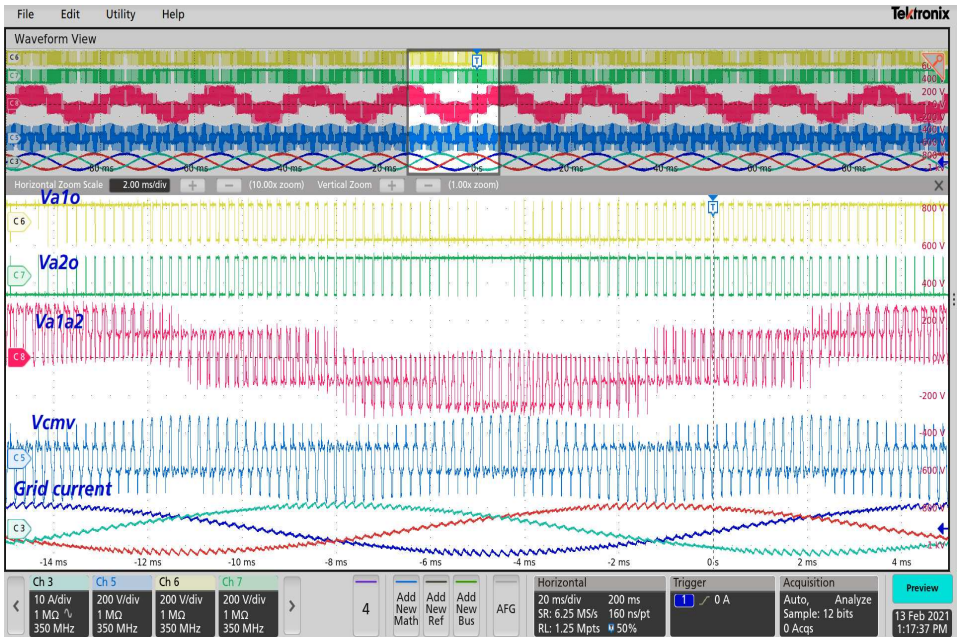


Figure 3.16: Inverter-1 a-phase pole voltage (1^{st} trace), inverter-2 a-phase pole voltage (2^{nd} trace),a-phase voltage across the primary of the transformer (3^{rd} trace), CMV between the mid point of the capacitor(4^{th} trace) and abc- phase primary current (bottom trace) for complementary switching algorithm

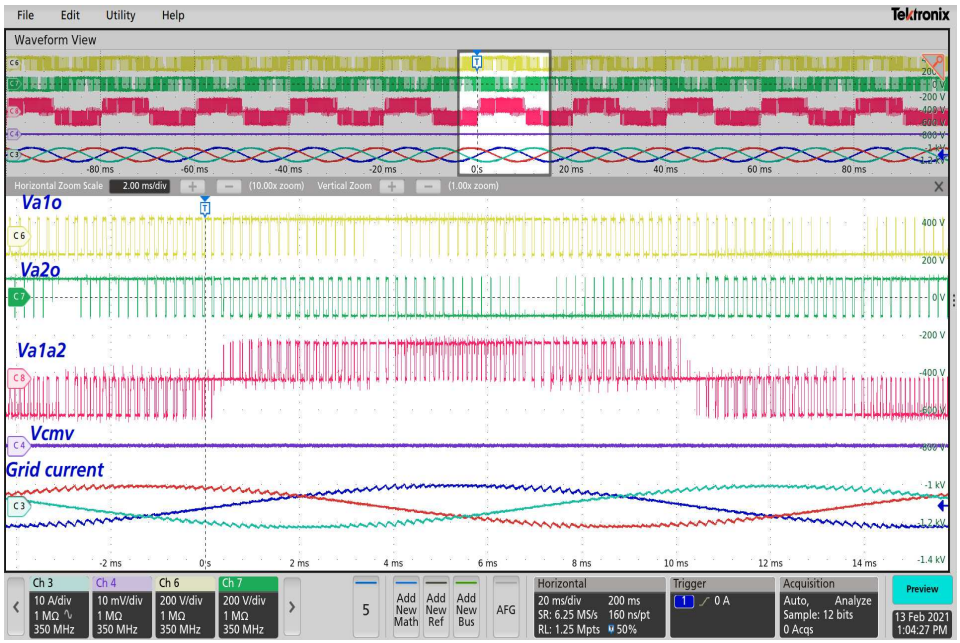


Figure 3.17: Inverter-1 a-phase pole voltage (1^{st} trace), inverter-2 a-phase pole voltage (2^{nd} trace),a-phase voltage across the primary of the transformer (3^{rd} trace), CMV between the mid point of the capacitor(4^{th} trace) and abc- phase primary current (bottom trace) for Per Phase Balanced switching Methodology

controller for the proposed configuration is verified on an experimental setup by feeding 1.8 kW active power to the load. The proposed configuration exhibit sinusoidal current at the load with the prescribed switching algorithms (isolated DC bus in case of complementary switching, common DC bus in case of per phase balanced switching algorithm). The

balanced switching algorithm is used to verify the dynamic response of the system with a designed controller. The current controller performance is demonstrated by changing the active power reference (i_{dref})from 0 to 1.1kW and then 1.1 kW to 1.8 kW, as shown in Fig.3.18 and Fig.3.19,respectively. As demonstrated in section-IID, the characteristic impedance of the plant is used to compute the controller's proportional and integral gains. At 1.1 kW and 1.8kW, the virtual grid resistance R_P (Vg/ig) can be computed as 60Ω and 36Ω respectively, considering the grid line to line voltage of 250 V (RMS). With $K_P = 0.1$ and $K_I = 1000$ calculated using (3.32) at τ =60ms, the grid current derived from series inverter takes approximately 3 cycles to reach a steady state when i_{dref} changed from 0 to 0.6 PU and 0.6 to 1 PU as shown in the left and right trace of Fig.3.18 respectively. Further to demonstrate the improved dynamic response the τ =5ms is considered, and the corresponding controller gains $K_P = 1.2$ and $K_I = 12000$ is computed using (3.32). With the computed gains, the grid injected current attains the steady-state within the quarter cycle as shown in the left and the right trace of Fig.3.19 with the change in active power reference from 0 to 1.1 kW and 1.1kW to 1.8kW, respectively

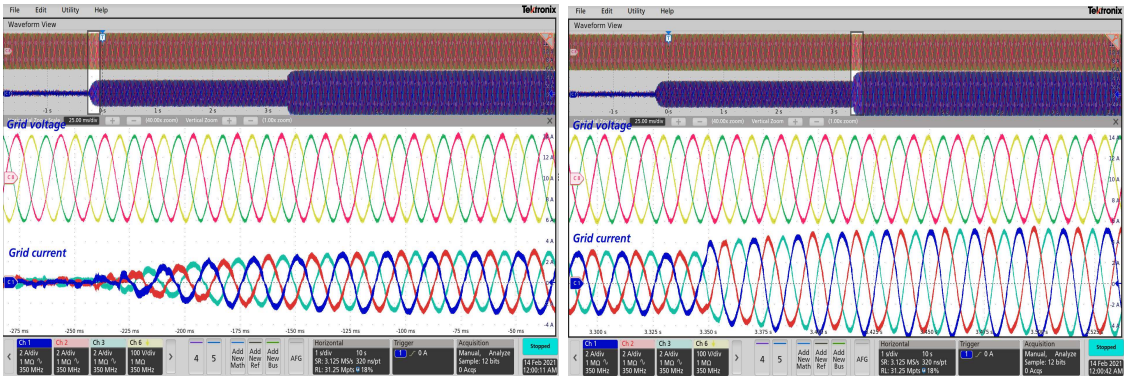


Figure 3.18: Three phase grid voltage(V_{abc})(unit x-axis: 25ms/div; y-axis: 100 volts/div) and grid injected current(I_{abc})(unit x-axis:25ms/div; y-axis: 2 Amps/div) with step change in i_{dref} from 0 to 0.6PU (left trace) and 0.6PU to 1 PU (right trace) considering $\tau = 60$ms and corresponding $K_P = 0.1$ and $K_I = 1000$)

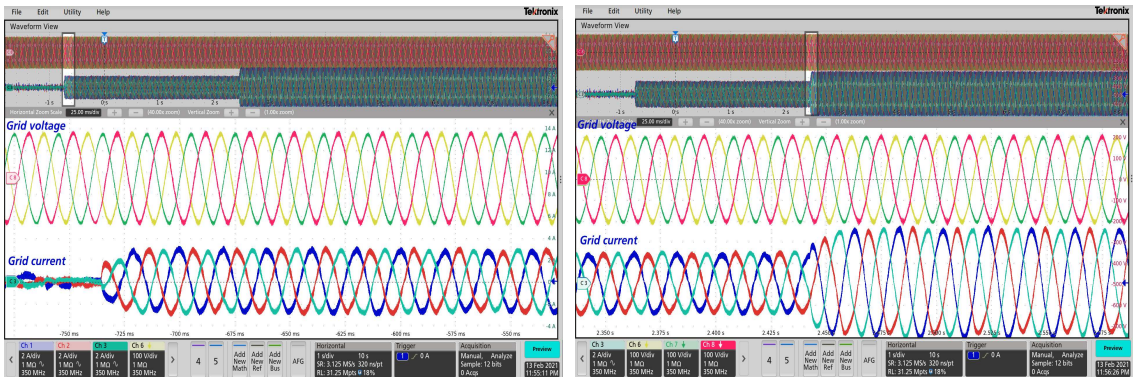


Figure 3.19: Three phase grid voltage(V_{abc}(unit x-axis: 25ms/div; y-axis: 100 volts/div) and grid injected current(I_{abc})(unit x-axis: 25ms/div; y-axis: 2 Amps/div) with step change in i_{dref} from 0 to 0.6PU (left trace) and 0.6PU to 1 PU (right trace) considering $\tau = 5$ms and corresponding $K_P = 1.2$ and $K_I = 12000$)

The efficacy of the closed-loop current control with the change in reactive power reference in grid-connected mode is shown in Fig.3.20. With the reactive power reference change from 0 to 0.2 PU at t=0s, the corresponding leading phase shift in the current from the grid voltage is shown in Fig.3.20 proves the proposed converter efficacy to support reactive power effectively during fault ride through conditions.

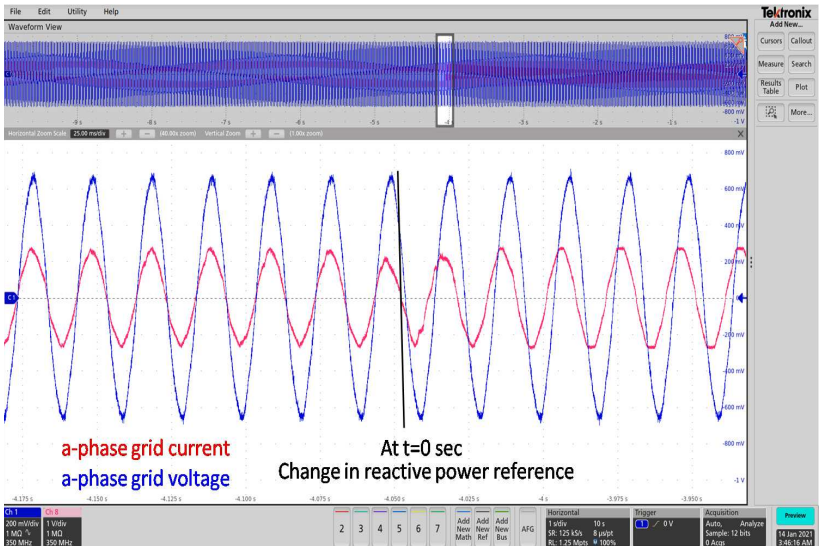


Figure 3.20: a-phase Grid voltage(V_{abc})(unit x-axis: 5ms/div; y-axis: 60 V/div) and a-phase grid injected current(I_{abc})(unit x-axis: 25ms/div; y-axis: 4 Amps/div) with step change in reactive power reference from 0 to 0.2PU

3.3 Conclusion

The proposed work described a series-solar interface inverter operating with two switching algorithms to validate DC bus minimization and CMV elimination efficacy. With the complementary switching algorithm, it has been identified that only 50% DC bus voltage is sufficient to derive the AC bus voltage equivalent to a parallel inverter. Whereas in the per-phase balanced algorithm, the DC bus requirement would be 42% lesser than the parallel inverter. It is also demonstrated that the switching sequence of per phase balanced switching algorithm forces the instantaneous CMV to zero provides the flexibility of DC bus grounding. The described algorithms have been validated experimentally on the proposed configuration for reduced DC bus voltage and eliminations of circulating current by pumping 1.8 kW power to the grid.

Chapter 4

A Novel Multi Gain Grid-Connected Inverter With Asynchronous Switching for Intra-Inverter Circulating Current Elimination

4.1 The Proposed Multi gain voltage solar interface inverter

The proposed topology shown in Fig.4.1 consists of three modules of conventional three-phase inverter connected with the primary of multi tap three phase transformer. The secondary of the transformer connected with the grid at the point of common coupling (PCC). For seamless power transfer to the grid, the synchronous (d-q) reference frame based closed loop controller is employed to synthesize the switching pulse for the inverter modules present in the configuration. The d-q controller is responsible to feed the reference power to the grid by tracking the three-phase grid voltages ($v_{g_{abc}}$) and grid currents ($i_{g_{abc}}$). The real and reactive power references are generated for the current PI controller considering the grid voltage reference angle (θ) obtained from phase locked loop (PLL) correspond to $v_{g_{abc}}$. The reference angle θ is used to convert three phase abc quantities to two phase d-q quantities of grid voltage (v_d and v_q correspond to $v_{g_{abc}}$) and grid injected current (i_d and i_q correspond to $i_{g_{abc}}$). Since θ is derived from $v_{g_{abc}}$, the i_d and i_q represents instantaneous real and reactive power being injected to grid respectively. Through d-PI and q-PI controllers, the modulation correspond to the desired active (i_{dref}) and reactive (i_{qref}) power being injected to the grid are generated as shown in Fig.4.1. The reference modulation is further divided into three parts correspond to individual inverter present in the proposed topology to generate individual switching pulses. Further the modulation separation for the three inverters is based on the three variants of topologies considered in this work. The three variants of configurations differ based on the individual phases of inverter modules connected with the primary of the transformer and secondary connected with the grid. The difference of three variants used in this work shown through a-phase connections as depicted in Fig.4.2 with the primary of the transformer and corresponding secondary connection interfaced with the grid.

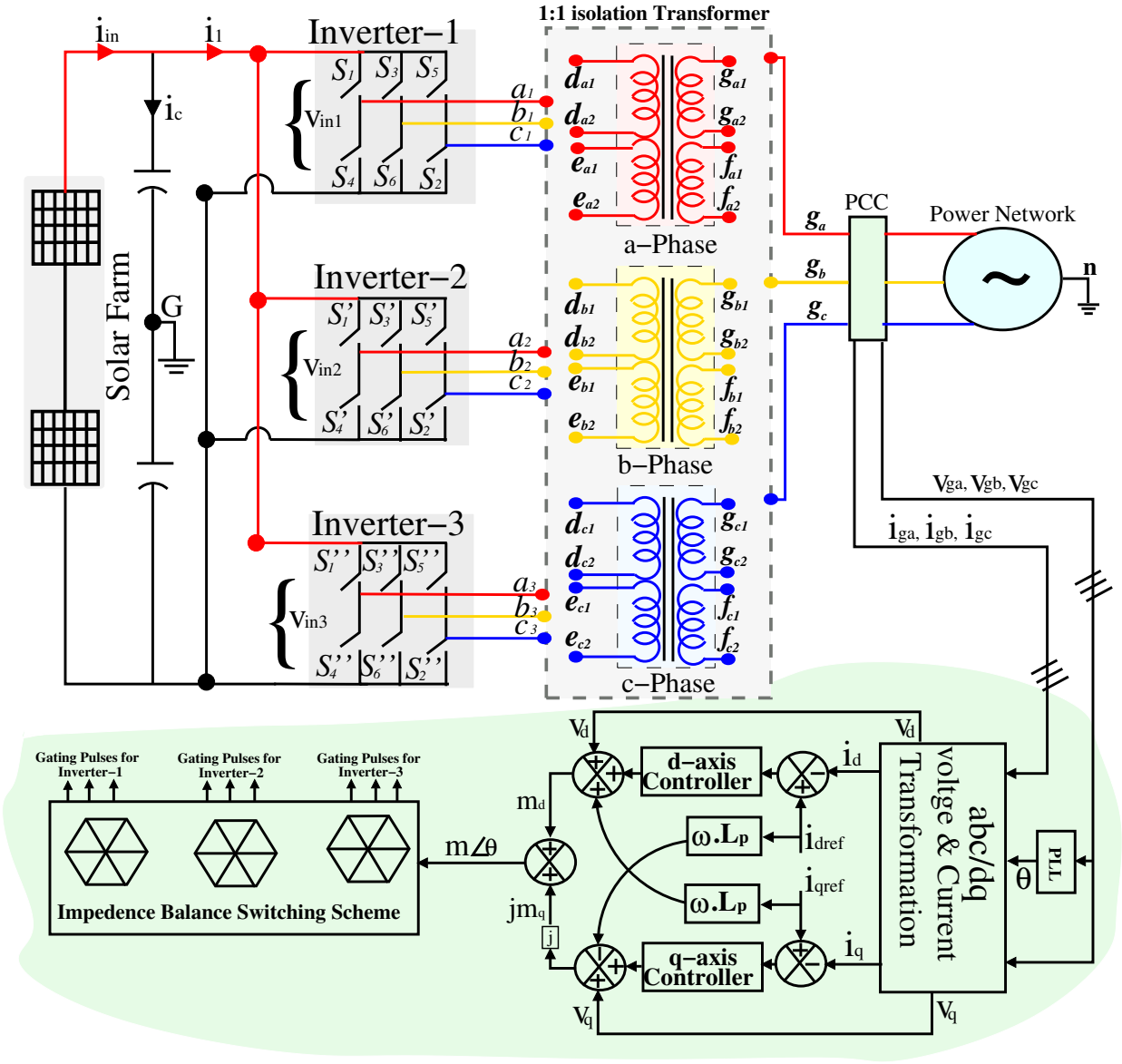


Figure 4.1: The circuit diagram of proposed high voltage gain solar inverter

The three variants of proposed configuration with reference to a-phase connections is explained as

1. **Variant-1**: Primary side (Referring to Fig.4.2a) ⇒ a-phase of Inverter-1 (a_1) connected with first tapping terminal (d_{a1}), a-phase of Inverter-2 (a_2) connected with second and third tapping (d_{a2} and e_{a1}), a-phase of Inverter-3 (a_3) connected with fourth tapping (e_{a2}); Secondary side (Referring to Fig.4.2a) ⇒ Two winding connected in series (g_{a2} connected with f_{a1}) and output is taken across the series winding (between g_{a1} and f_{a2}). The output impedance correspond to injected power to grid is transformed to primary and the corresponding three phase equivalent circuit is shown in Fig.4.3a. The transformed equivalent circuit is used to explain the phenomena of impedance balance in subsequent section. In equivalent circuits, Z_L represents the $R_g + j\omega(L_p + L_s)$.

where;

$$R_g = \frac{v_g(per\ phase\ grid\ voltage)}{i_g(per\ phase\ grid\ injected\ current)}$$

and L_p and L_s are primary and secondary inductance of the transformer.

2. **Variant-2**: The primary side connection is same as that of variant-1 primary connection; Secondary side (Referring to Fig.4.2b)⇒ g_{a2} is shorted with f_{a2} and output is taken across the terminal g_{a1} and f_{a1}. Since the primary side connections of the transformer is identical as that of variant-1, the three phase equivalent circuit shown in Fig.4.3a is also valid for variant-2. However, the secondary side connection decides the DC bus requirement, the DC bus requirement computations compare to variant-1 is explained in subsequent section.

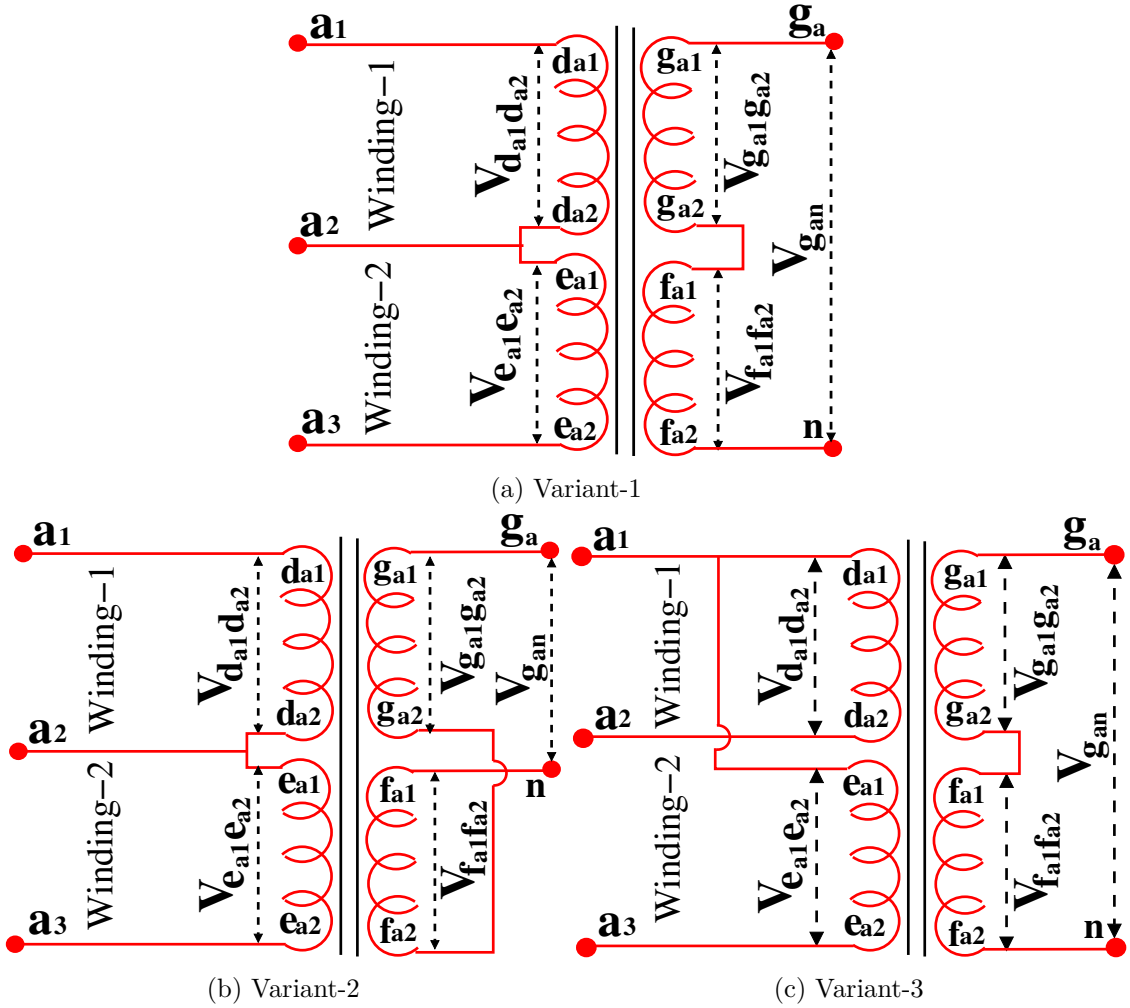
3. **Variant-3**: Primary side (Referring to Fig.4.2c) ⇒ a-phase of Inverter-1 (a_1) connected with first and third tapping terminal (d_{a1} and e_{a1}), a-phase of Inverter-2 (a_2) connected with second tapping (d_{a2}), a-phase of Inverter-3 (a_3) connected with fourth tapping (e_{a2}) ; The secondary side connection is same as that of variant-1 secondary connection. The corresponding three-phase transformed equivalent impedance circuit to demonstrate the impedance balance is shown in Fig.4.3b.

4.2 The grid voltage realization through dynamic impedance balancing

With the proposed variants in this work, the dynamic impedance balancing is possible through careful selection of available switching states of three 3-phase inverters. The resultant output space vector realization with dynamic balancing of impedance is explained in this section. The switching sequence realization for each variant shown in Fig.4.3 is explained through space vector locations.

4.2.1 The switching sequence realization for variant-1 and variant-2

In the case of variant-1 and variant-2, the primary side connections are identical. Therefore the transformed equivalent impedance model are also same as shown in Fig.4.3a. To explain the impedance balance switching scheme for both the variants, an instance of switching state-1 (1 0 0 correspond to a phase top switch -ON, b-phase bottom switch-ON, c-phase bottom switch -ON) is chosen for inverter-1. Similarly, the inverter-2 and inverter-3 are switched with switching state- 3' (0 1 0) and 5" (0 0 1). With the selected switching states, the transformed equivalent impedance circuit can be viewed as shown in Fig.4.4 demonstrate the corresponding per-phase load current path between the three inverter modules. Now to explain the ceased circulating currents with in the inverter modules with the applied switching states, the superposition principle is applied on the individual sources shown in Fig.4.4. The super position theorem applied on individual sources of inverter-1, inverter-2 and inverter-3 separately by shorting other sources and



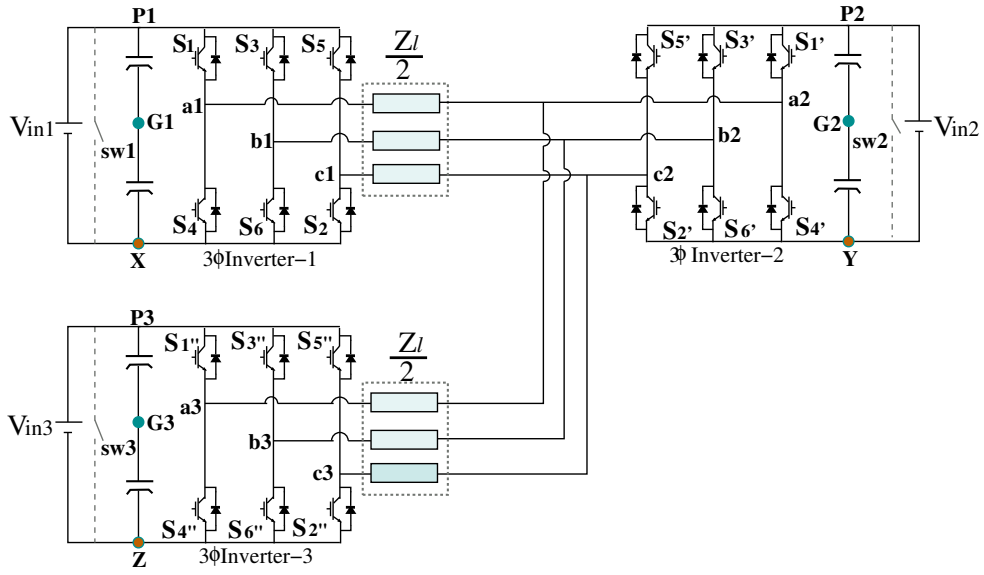
(a) Variant-1

(b) Variant-2

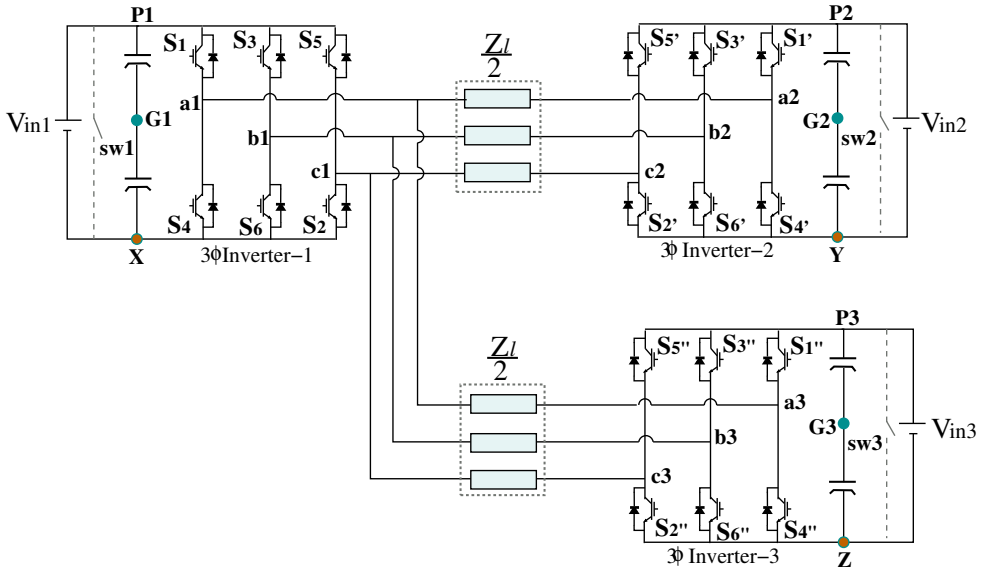
(c) Variant-3

Figure 4.2: The a-phase primary and secondary side interface transformer connections to illustrate proposed variants

corresponding equivalent circuit are depicted in left, middle and right traces of Fig.4.5. In Fig.4.5, X, Y and Z represents the shorted DC potentials of inverter-1, inverter-2 and inverter-3 respectively with applied super position theorem. It is evident from equivalent circuits shown in Fig.4.5 that the respective potential across X,Y and Z is zero represents balanced per-phase impedance across the inverter modules. The per-phase balanced Impedance cancel the influential voltage effect on each other encourages to connect all inverter modules with common DC bus. With the common DC bus, $v_{in_1} = v_{in_2} = v_{in_3}$. Further to explain the AC voltage gain for fixed DC bus voltage , the DC bus voltage magnitude $V_{C_{dc}}$ (conventional DC bus voltage for single stage inverter to synthesize the grid voltage) is considered. With the considered DC bus voltage, the output space vector realization is explained for variant-1 (Fig.4.2a) and variant-2 (Fig.4.2b) through demonstrated switching states 1 3' and 5". The space vector across the winding-1 connected with inverter-1 and inverter-2 can be identified as $\overrightarrow{V_{13'}}$ and $\overrightarrow{V_{3'5''}}$ across winding-2 connected between inverter-2 and inverter-3. Since the primary connections are same for both variants, the space vector realization for winding-1 and winding-2 is same as shown in Fig.4.6a and Fig.4.6b respectively. But correspond to the secondary connections, the



(a) With variant-1 & 2



(b) With variant-3

Figure 4.3: The equivalent circuit realization by transforming grid impedance onto the primary of the transformer

output voltage can be derived as $\overrightarrow{V_{13'}} + \overrightarrow{V_{3'5''}}$ in case of variant-1 (shown in Fig.4.6a) and in case of variant-2, it is $\overrightarrow{V_{13'}} - \overrightarrow{V_{3'5''}}$ as shown in Fig.4.6b. The primary-side space vector realization for both the variants can be mathematically modeled as:

$$\begin{aligned}\overrightarrow{v}_{d_{abc}} &= (\overrightarrow{V_1}) - (\overrightarrow{V_{3'}}) = \overrightarrow{V_{13'}}(Fig.4.6a\ and\ Fig.4.6b) \\ &= m_a \frac{v_{c_{dc}}}{2}(e^{j\theta_t} - e^{j(\theta_t+120^o)}) \\ &= \sqrt{3}.m_a \frac{v_{c_{dc}}}{2} e^{j(\theta_t+330^o)}\end{aligned} \tag{4.1}$$

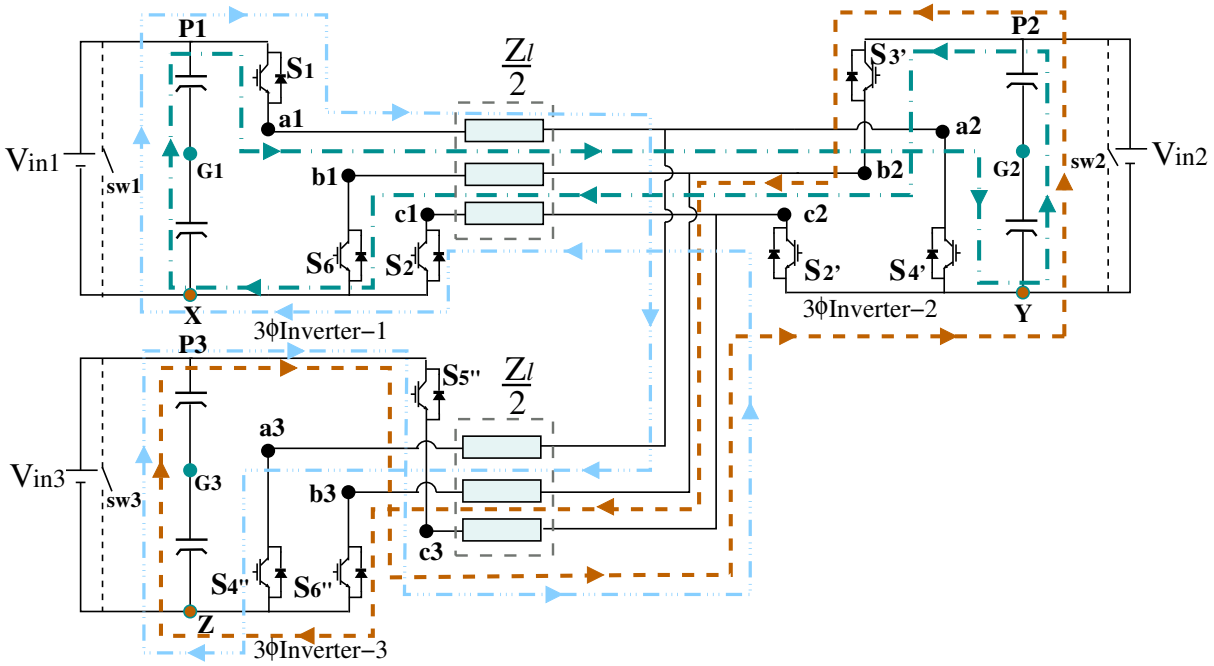


Figure 4.4: The equivalent transformed impedance circuit with switching state 1 3' 5" and corresponding current path for variant-1 & 2

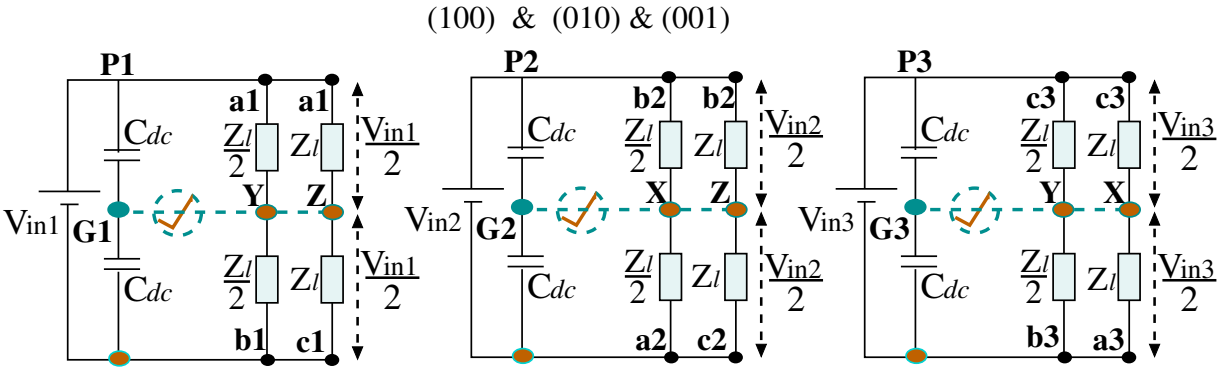


Figure 4.5: The equivalent per phase impedance circuit with applied superposition principle on proposed configuration by keeping inverter-1 (left), inverter-2(middle) and inverter-3 (right) with switching state 13'5"for variant-1 and variant-2

$$\begin{aligned}\overrightarrow{v}_{e_{abc}} &= (\overrightarrow{V_{3'}}) - (\overrightarrow{V_{5''}}) = \overrightarrow{V_{3'5''}} (Fig.4.6a \text{ and } Fig.4.6b) \\ &= m_a \frac{v_{c_{dc}}}{2} (e^{j(\theta_t + 120^o)} - e^{j(\theta_t + 240^o)}) \\ &= \sqrt{3}.m_a \frac{v_{c_{dc}}}{2} e^{j(\theta_t + 90^o)} \end{aligned} \tag{4.2}$$

Here $\overrightarrow{v}_{d_{abc}}$, $\overrightarrow{v}_{e_{abc}}$ are the winding-1 and winding-2 transformer primary voltage space vector with designated switching states (1 3' 5"). With computed $\overrightarrow{v}_{d_{abc}}$ and $\overrightarrow{v}_{e_{abc}}$, the output voltage space vector equivalent to grid voltage at the secondary side correspond to

variant-1 and variant-2 can be modeled as:

For variant-1	**For variant-2**
$\overrightarrow{v}_{g_{abc}} = \overrightarrow{v}_{d_{abc}} + \overrightarrow{v}_{e_{abc}}$	$\overrightarrow{v}_{g_{abc}} = \overrightarrow{v}_{d_{abc}} - \overrightarrow{v}_{e_{abc}}$
$= \frac{\sqrt{3}m_a v_{c_{dc}}}{2} e^{j(\theta_t + 30^o)}$	$= \frac{3m_a v_{c_{dc}}}{2} e^{j(\theta_t - 60^o)}$
$= \beta . e^{j(\theta_t + 30^o)}$	$= \gamma . e^{j(\theta_t - 60^o)}$
$Where; \quad \beta = \frac{\sqrt{3}m_a v_{c_{dc}}}{2}$	$Where; \quad \gamma = \frac{3m_a v_{c_{dc}}}{2}$

(4.3)

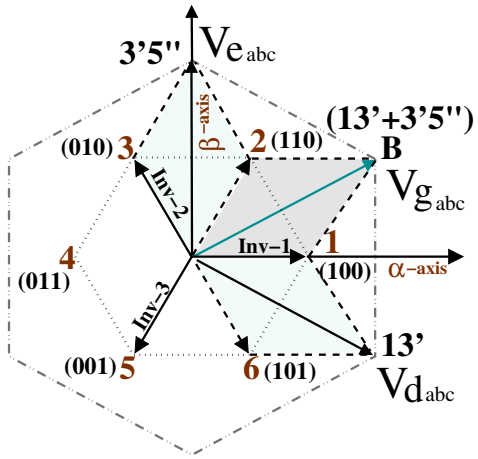
$v_{g_{abc}}$ is the output voltage space vector representing grid voltage. Since the α' is aligned with the inverter-1 a-phase axis (Fig.4.6a), the grid voltage is displaced by 30°in variant-1 and (-)60°in variant-2. From (4.3) it is evident that the resultant output space vector magnitude with variant-1 and variant-2 are $\sqrt{3}$ and 3 times more than the conventional inverter respectively. In other words, to synthesize the grid voltage, the DC bus requirement is 42% lesser than conventional sine-triangle operated inverter in case of variant-1 and 67% lesser in case of variant-2 . Further, the possible switching combination with per phase impedance balance along with the corresponding computed space vector voltage (in 360°) and resultant CMV is depicted in Table-4.1. The identified space vector locations for variant-1 and variant-2 are shown in Fig.4.9a with hexagon vertices "ABCDEF" and Fig.4.9b with hexagon vertices "GHIJKL" respectively.

Table 4.1: The proposed solar inverter switching combinations, corresponding resultant load space vector and CMV profile for variant-1 and variant-2

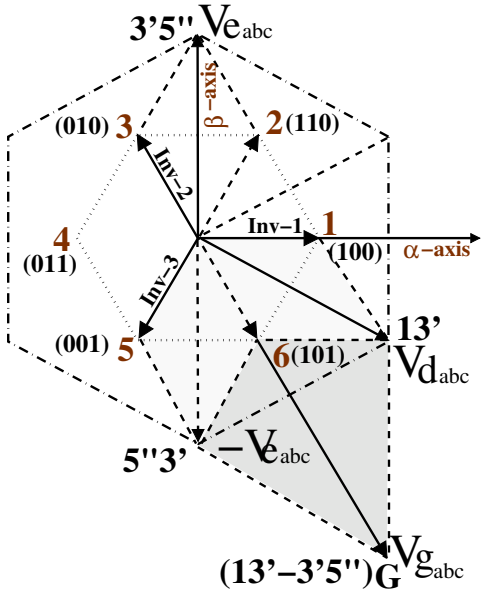
Switching instance Variant-1	Switching instance Variant-2	Inv-1 SW	Inv-2 SW	Inv-3 SW	Resultant Voltage		CMV b/w inverter 1&2 &3
					Variant-1	Variant-2	
13'+3'5"	13'-3'5"	100	010	001	$\beta.\angle 30$	$\gamma.\angle 300$	0
24'+4'6"	24'-4'6"	110	011	101	$\beta.\angle 90$	$\gamma.\angle 0$	0
35'+5'1"	35'-5'1"	010	001	100	$\beta.\angle 150$	$\gamma.\angle 60$	0
46'+6'2"	46'-6'2"	011	101	110	$\beta.\angle 210$	$\gamma.\angle 120$	0
51'+1'3"	51'-1'3"	001	100	010	$\beta.\angle 270$	$\gamma.\angle 180$	0
62'+2'4"	62'-2'4"	101	110	011	$\beta.\angle 330$	$\gamma.\angle 240$	0

4.2.2 The switching sequence realization for variant-3

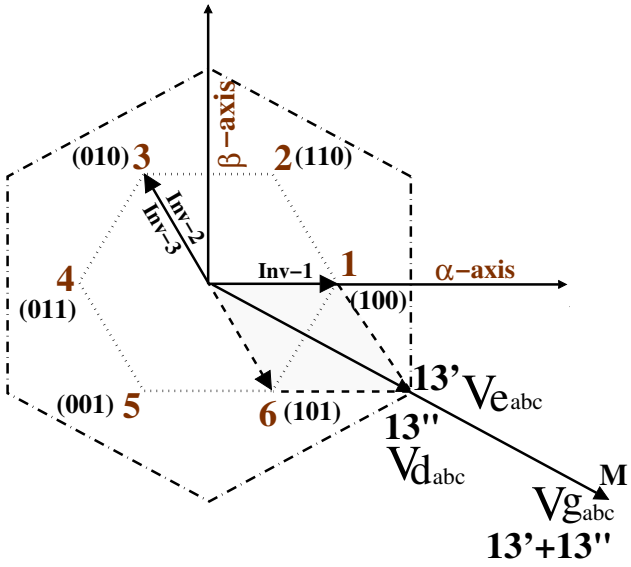
The primary side connection of the transformer in variant-3 as shown in Fig.4.2c is different from the variant-1 and variant-2. Unlike other variants, in variant-3, the



(a) Variant-1 (13'5")



(b) Variant-2 (13'5")



(c) Variant-3 (13'3")

Figure 4.6: The space vector realization with demonstrated switching state

inverter-1 is switched with switching state-1 (1 0 0) and other two inverters switched with the switching state-3 (0 1 0) to accomplish dynamic per-phase impedance balancing. With the introduced switching states (13'3"), the transformed equivalent impedance circuit along with the current path between the inverter modules can be seen as shown in Fig.4.7. Similar to variant-1 and variant-2 the superposition principle is applied to demonstrate circulating current elimination through impedance balance. After applying the superposition principle on individual inverters, the impedance distribution of corresponding phases across the DC bus can be seen as shown in Fig.4.8. As it is shown in Fig.4.8, with the equally distributed impedance, the points X,Y and Z correspond to inverter-1, inverter-2 and inverter-3 (the short circuit points) experiences the same voltage as that of the capacitor mid point (zero considering capacitor mid point is the reference

for the circuit) of individual source. Since the influential effect of one source on the other is zero, the common DC bus can be employed for all the inverter present in the proposed configuration.

Further to demonstrate the DC bus voltage requirement to realize the grid voltage with variant-3, the space vector across winding-1 is $\overrightarrow{V_{13''}}$ and winding-2 is $\overrightarrow{V_{13''}}$ as shown in Fig.4.6c are realized considering the switching state (13'3"). With presented switching state, both winding experiences the same phase voltages as shown in Fig.4.6c can be mathematically modeled as:

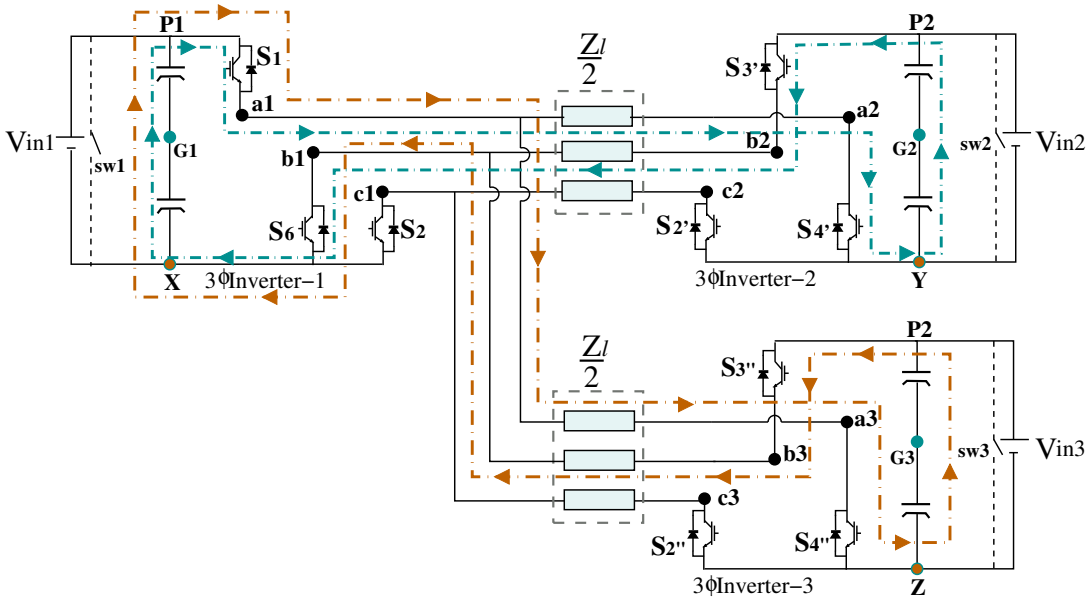


Figure 4.7: The equivalent transformed impedance circuit with switching state 1 3' 3" and corresponding current path for variant-3

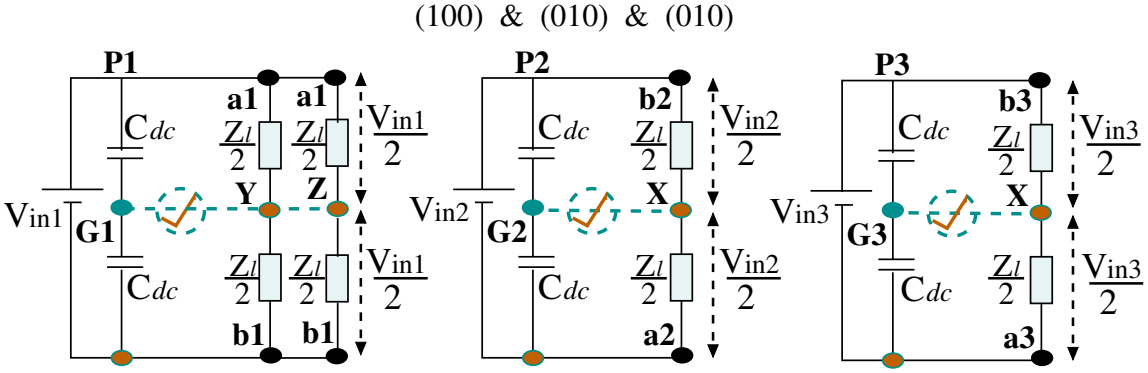
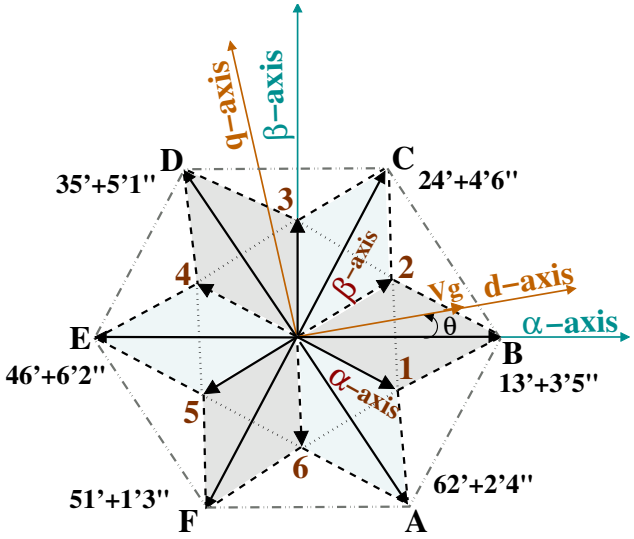
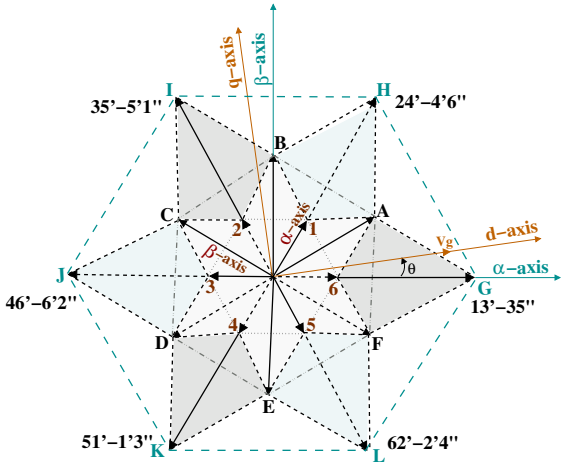


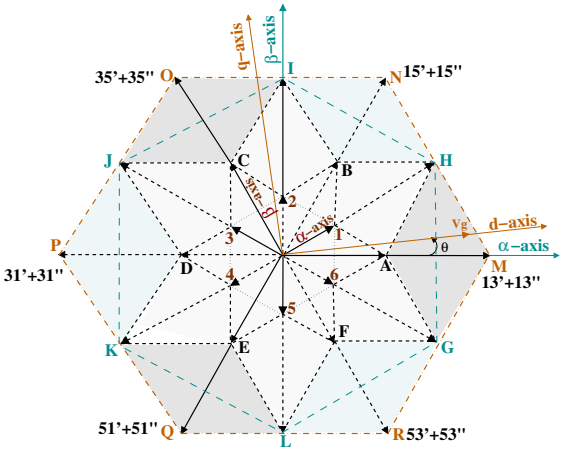
Figure 4.8: The equivalent per phase impedance circuit with applied superposition principle on proposed configuration by keeping inverter-1 (left), inverter-2(middle) and inverter-3 (right) with switching state 13'3"for variant-3



(a) For variant-1



(b) For variant-2



(c) For variant-3

Figure 4.9: The space vector locations to realize the grid space vector correspond to per-phase impedance balance

$$\begin{aligned}
&\overrightarrow{v}_{d_{abc}} = (\overrightarrow{V_1}) - (\overrightarrow{V_{3'}}) = \overrightarrow{V_{13'}};\ \overrightarrow{v}_{e_{abc}} = (\overrightarrow{V_1}) - (\overrightarrow{V_{3''}}) = \overrightarrow{V_{13''}} \\
&\overrightarrow{v}_{d_{abc}} = \overrightarrow{v}_{e_{abc}} = m_a \frac{v_{c_{dc}}}{2}(e^{j\theta_t} - e^{(\theta_t+120^o)}) \\
&\qquad = \sqrt{3}.m_a \frac{v_{c_{dc}}}{2} e^{j(\theta_t-30^o)}
\end{aligned} \tag{4.4}$$

With the realized primary side space vector, the resultant space vector at the output is shown in Fig.4.6c represented with $\overrightarrow{v}_{g_{abc}}$ can be computed as:

$$\begin{aligned}
&\overrightarrow{v}_{g_{abc}} = \overrightarrow{v}_{d_{abc}} + \overrightarrow{v}_{e_{abc}} = \sqrt{3} m_a v_{c_{dc}} e^{j(\theta_t-30^o)} \\
&\overrightarrow{v}_{g_{abc}} = \lambda.e^{j(\theta_t-30^o)} \qquad ;Where\ \lambda = \sqrt{3} m_a v_{c_{dc}}
\end{aligned} \tag{4.5}$$

Similar to the demonstrated switching state (13'3") all possible balanced impedance switching combinations are identified as shown in Table-4.2 to realize the space vector

in 360°and corresponding output space vector locations across the secondary of the transformer are depicted as shown in Fig.4.9c with hexagon vertices "MNOPQR". To derive the switching pulses for the individual inverter in closed loop with the sensed grid voltage $v_{g_{abc}}$ by taking θ (on α axis) as reference, the inverter-1 is displaced by 30°as explained in (4.5) and inverter-2 and inverter-3 space vector is displaced by 120° from inverter-1. In this configuration, from (4.5) it is evident that the synthesized magnitude of grid voltage with proposed variant is $2\sqrt{3}$ times more compare to grid voltage synthesized with single inverter. In other-words, the DC requirement to synthesize the grid voltage is 71% lesser than conventional single stage inverter.

Table 4.2: The proposed solar inverter switching combinations, corresponding resultant load space vector and CMV profile for variant-3

Switching instance	Inv-1 SW	Inv-2 SW	Inv-3 SW	Resultant Voltage	CMV b/w inverter 1&2 &3
13'+13"	100	010	010	$\lambda\angle 330$	0
15'+15"	100	001	001	$\lambda\angle 30$	0
35'+35"	010	001	001	$\lambda\angle 90$	0
31'+31"	010	100	100	$\lambda\angle 150$	0
51'+51"	001	100	100	$\lambda\angle 210$	0
53'+53"	001	010	010	$\lambda\angle 270$	0

4.3 The closed loop controller design through state space modeling

With computed DC bus requirement for 3 variants and the switching angle deviation for individual inverter with reference to grid voltage, the combined closed loop controller is modeled in this section. To design the closed loop controller, the primary impedance of each variant is transferred to secondary to model equivalent impedance and identified that the resultant impedance model is same for all three variants. In such scenario, the proposed configuration per-phase equivalent impedance can be modeled as:

$$Z_L = R_g + j.w.(L_p + L_s)$$

Where R_g is resistance correspond to injected power, L_p and L_s are primary and secondary winding inductance referred on to secondary side. With the computed equivalent impedance model, the three phase grid voltages ($v_{g_{an}}$,$v_{g_{bn}}$ and $v_{g_{cn}}$) can be expressed

as:

$$v_{g_{xn}} = R_g i_x + (L_p + L_s)\frac{di_x}{dt}; \quad Where\ x = a, b, c: \tag{4.6}$$

Further, the three phase grid voltages and grid injected currents are transformed to the synchronous reference frame $(d-q)$ to derive the plant model as:

$$v_d = \frac{2}{3}[v_{g_{an}} cos(\theta) + v_{g_{bn}} cos(\theta - 120) + v_{g_{cn}} cos(\theta + 120)] \tag{4.7}$$

$$v_q = \frac{-2}{3}[v_{g_{an}} sin(\theta) + v_{g_{bn}} sin(\theta - 120) + v_{g_{cn}} sin(\theta + 120)] \tag{4.8}$$

$$i_d = \frac{2}{3}[i_{g_a} cos(\theta) + i_{g_b} cos(\theta - 120) + i_{g_c} cos(\theta + 120)] \tag{4.9}$$

$$i_q = \frac{-2}{3}[i_{g_a} sin(\theta) + i_{g_b} sin(\theta - 120) + i_{g_c} sin(\theta + 120)] \tag{4.10}$$

Further to obtain the state space model, the rate of change of state variable (grid injected current mentioned in (4.9) and (4.10)) can be expressed as:

$$\begin{aligned}\frac{di_d}{dt} &= \frac{1}{L_p + L_s}[\frac{2}{3}(v_{g_{an}} cos(\theta) + v_{g_{bn}} cos(\theta - 120) + v_{g_{cn}} cos(\theta + 120))] \\ &- \frac{R_g}{L_p + L_s}[\frac{2}{3}(i_{g_a} cos(\theta) + i_{g_b} cos(\theta - 120) + i_{g_c} cos(\theta + 120))] + \omega i_q \end{aligned} \tag{4.11}$$

$$\begin{aligned}\frac{di_q}{dt} &= \frac{1}{L_p + L_s}[-\frac{2}{3}(v_{g_{an}} sin(\theta) + v_{g_{bn}} sin(\theta - 120) + v_{g_{cn}} sin(\theta + 120))] \\ &- \frac{R_g}{L_p + L_s}[-\frac{2}{3}(i_{g_a} sin(\theta) + i_{g_b} sin(\theta - 120) + i_{g_c} sin(\theta + 120))] - \omega i_d \end{aligned} \tag{4.12}$$

By substituting (4.7) and (4.8), the (4.11) and (4.12) can be further simplified as:

$$\frac{di_d}{dt} = \frac{v_d}{L_p + L_s} - \frac{R_g}{L_p + L_s} i_d + w.i_q \tag{4.13}$$

$$\frac{di_q}{dt} = \frac{v_q}{L_p + L_s} - \frac{R_g}{L_p + L_s} i_q - w.i_d \tag{4.14}$$

Along with the grid injected current, the other state variable input voltage $v_{c_{dc}}$ variations can be modeled as:

$$\frac{dv_{c_{dc}}}{dt} = \frac{1}{C_{dc}}[-(m_d.i_d + m_q.i_q) + i_{in}] \tag{4.15}$$

Here C_{dc} is the equivalent DC capacitance across the DC bus.m_d and m_q are instantaneous duty of Inverters in d-q domain respectively. I_{in} is the sources current shown in Fig.4.1. Further to evaluate the steady state duty of proposed configuration, the state variables presented in (4.13), (4.14) and (4.15) made equal to zero. At the steady state, the average

duty of inverters and the output current can be obtained as:

$$v_d = k.n.m_d v_{c_{dc}} \;\; ; \;\; v_q = k.n.m_q v_{c_{dc}} \;\; ; i_d = \frac{i_{in}}{m_d} \tag{4.16}$$

$$M_d = \sqrt{\frac{i_{in} R_g}{k.n.v_{c_{dc}}}} \quad ; \quad M_q = \frac{i_{in}.\omega(L_p + L_s)}{M_d.k.n.v_{c_{dc}}} \tag{4.17}$$

Here it can be observed that, with the proposed variants, the DC bus requirement changes to synthesize the grid voltage. Correspondingly k varies in (4.16) and (4.17) as $\frac{\sqrt{3}}{2}$, $\frac{3}{2}$ and $\frac{2\sqrt{3}}{2}$ for variant-1, 2 and 3 respectively.Similarly n represent the voltage gain compared to conventional inverter, varies in (4.16) and (4.17) as 2, 3.53 and 4.01 for variant-1, 2 and 3 respectively. With the identified state variables, the state space equation can be written as:

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{4.18}$$

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \\ \frac{dv_{c_{dc}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_g}{L_p+L_s} & w & \frac{k.n.m_d}{(L_p+L_s)} \\ -w & -\frac{R_g}{L_p+L_s} & \frac{k.n.m_q}{(L_p+L_s)} \\ -\frac{m_d}{C_{dc}} & -\frac{m_q}{C_{dc}} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_{c_{dc}} \end{bmatrix} + \begin{bmatrix} \frac{k.n.v_{in}}{(L_p+L_s)} & 0 & 0 \\ 0 & \frac{k.n.v_{in}}{(L_p+L_s)} & 0 \\ 0 & 0 & \frac{1}{C_{dc}} \end{bmatrix} \begin{bmatrix} m_d \\ m_q \\ i_{in} \end{bmatrix}$$

$$y(t) = Cx(t) + Du(t) \tag{4.19}$$

$$\begin{bmatrix} v_{in} \\ i_{od} \\ i_{oq} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_{c_{dc}} \end{bmatrix} \tag{4.20}$$

Here i_{od} and i_{oq} represent the grid injected current in dq domain. From (4.18) - (4.20), the proposed system transfer function matrix can be written as:

$$y(s) = [C(SI - A)^{-1}B + D]u(s)$$

$$\begin{bmatrix} V_{in} \\ i_{od} \\ i_{oq} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} \begin{bmatrix} m_d \\ m_q \\ i_{in} \end{bmatrix} \tag{4.21}$$

$$[y(s)] \quad = \quad [G] \quad [u(s)] \tag{4.22}$$

Here $y(s)$ is the output matrix, G is system transfer function matrix, $u(s)$ is input matrix. With state space model derived for the plant shown in (4.21), the effect of inverter duty on grid injected current can be identified from (4.21) on d- axis and q-axis as a transfer function G_{21} and G_{32} respectively. The transfer function of G_{21} and G_{32} can be expressed

as:

$$G_{21} = N1/D1 \quad ; \quad G_{32} = N2/D2 \tag{4.23}$$
$$N1 = (V_{in}.k.n(C_{dc}(L_p + L_s)s^2 + C_{dc}R_g s + k.m_q^2.n))$$
$$D1 = D2 = C_{dc}(L_p + L_s)^2 s^3 + 2C_{dc}(L_p + L_s)R_g s^2 + C_{dc}(L_p + L_s)^2 w^2 s + k.m_d^2.n(L_p + L_s)s$$
$$+ k.m_q^2.n(L_p + L_s)s + C_{dc}R_g^2 s + k.m_d^2.n.R_g + k.m_q^2.n.R_g)$$
$$N2 = (V_{in}.k.n(C_{dc}(L_p + L_s)s^2 + C_{dc}R_g s + k.m_d^2.n)$$

By neglecting the DC bus capacitance C_{dc} effect to design the current controller, the (4.23) can be written as:

$$\begin{aligned} D1 = D2 &= k.n(m_d^2 + m_q^2)(L_p + L_s)s + k.n(m_d^2 + m_q^2)R_g \\ &= k.n(m_d^2 + m_q^2)(L_p + L_s)(s + \frac{R_g}{L_p + L_s}) \\ N1 &= (k.n.m_q)^2 V_{in} \quad ; \quad N2 = (k.n.m_d)^2 V_{in} \\ G_{P_d} &= \frac{G_{21}}{V_{in}} = \frac{i_{od}}{m_d.V_{in}} \quad ; \quad G_{P_q} = \frac{G_{32}}{V_{in}} = \frac{i_{oq}}{m_q.V_{in}} \end{aligned} \tag{4.24}$$

With derived transfer function, the small signal flow diagram can be represented as shown in Fig.4.10. The plant transfer function in synchronous reference frame (SRF) can be expressed as:

$$G_{P_d} = \frac{k.n.m_q^2}{(m_d^2 + m_q^2)(L_p + L_s)(s + \frac{R_g}{L_p + L_s})} \tag{4.25}$$

$$G_{P_q} = \frac{k.n.m_d^2}{(m_d^2 + m_q^2)(L_p + L_s)(s + \frac{R_g}{L_p + L_s})} \tag{4.26}$$

For the plant, the current PI controller is defined as:

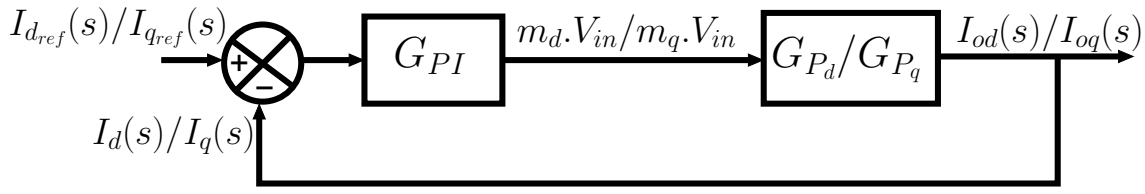


Figure 4.10: Small signal flow diagram of proposed configuration in dq-domain

$$G_{PI}(s) = K_p + \frac{K_i}{s} = \frac{K_p}{s}.(s + \frac{K_i}{K_p}) \tag{4.27}$$

With the PI controller, the open loop transfer function in SRF can be written as:

$$\begin{aligned} G_{ol} &= G_{P_d}.G_{PI}(for\ d-axis)\ or\ G_{P_q}.G_{PI}(for\ q-axis) \\ G_{ol} &= \frac{G}{(M_d^2+M_q^2)(L_p+L_s)s}.\frac{(s+\frac{K_i}{K_p})}{(s+\frac{R_g}{L_p+L_s})} \\ where;\quad G &= K_p.k.n.M_q^2(for\ d-axis) \\ G &= K_p.k.n.M_d^2(for\ q-axis) \end{aligned} \tag{4.28}$$

Here M_d and M_q are steady state modulation index derived from (4.17). With this, the closed loop transfer function of the system can be derived as:

$$\begin{aligned} G_{cl} &= \frac{G_{ol}}{1+G_{ol}} \\ G_{cl} &= \frac{G}{(M_d^2+M_q^2)(L_p+L_s)s+G} \\ G_{cl} &= \frac{1}{1+\frac{1}{G}(M_d^2+M_q^2)(L_p+L_s)s} \end{aligned} \tag{4.29}$$

The controller gain K_i is identified through the concept of pole zero cancellation by identifying the dominant poles and zeros through (4.28) and K_p can be obtained based on the desired dynamic response of closed loop system through (4.29).

$$K_i = \frac{R_g}{L_p+L_s}.K_p \quad ; \quad K_p = \frac{(M_d^2+M_q^2).(L_p+L_s)}{k.n.\tau.M_d^2} \tag{4.30}$$

With identified controller gain, the pole zero locations of the closed loop system at different R_g is shown in Fig.4.11. Although the system is stable at different R_g as evident from Fig.4.11, the values of K_p and K_i influences the dynamic performance of the system as demonstrated through the step response of the closed loop system (depicted in (4.29)) shown in Fig.(4.12). In subsequent section, the dynamic response of the proposed configuration at different controller gains is demonstrated through hardware results.

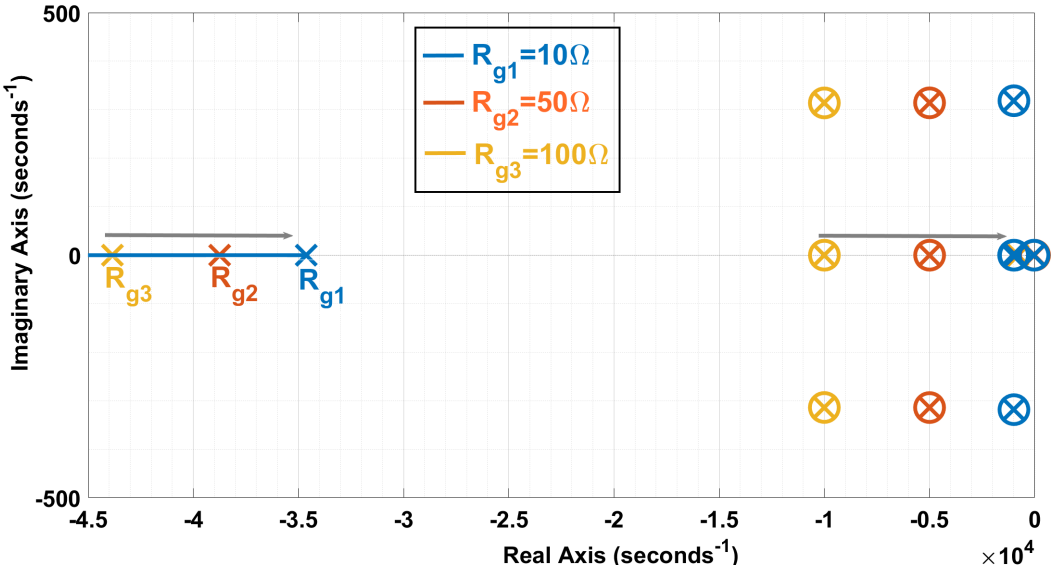


Figure 4.11: The closed loop Pole-Zero distribution with varying load R_g and chosen K_p and K_i for desired system response

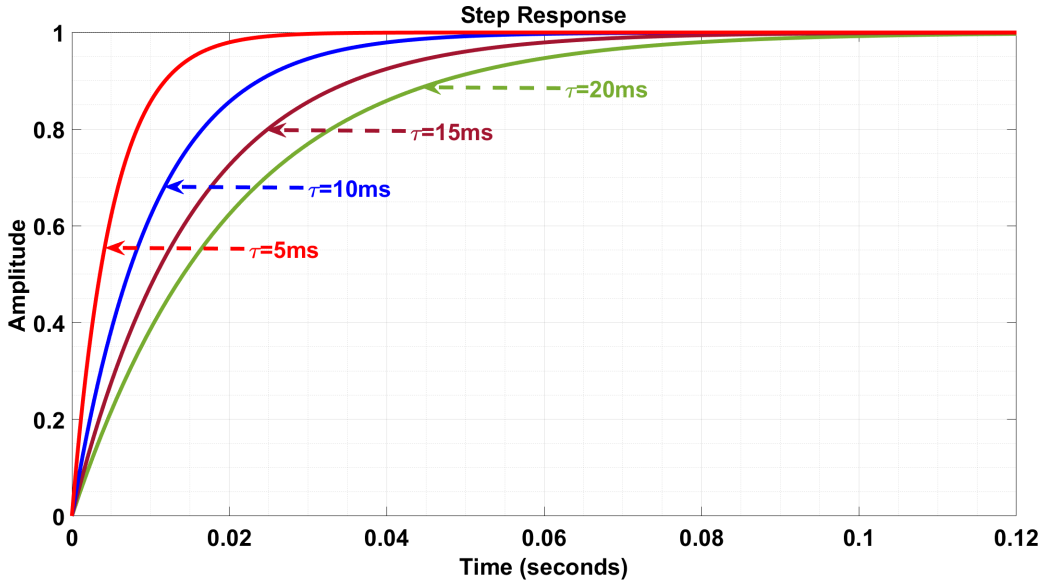


Figure 4.12: The Step response of closed loop system at different time constant(τ) with adjusted controller gains K_p and K_i

4.4 Result and Discussion

The proposed variants of high gain boost configurations are realized as explained in Fig.4.2 by connecting three semikron make IGBT based three phase inverter modules with the primary of three phase transformer. The secondary of the transformer connected with the grid forms PCC. The experimental setup to validate all proposed variants with reference to grid injected power, circulating current and DC bus requirement is shown in Fig.4.13 and corresponding operating parameters are tabulated in Table-4.3. The switching pulses with reference to grid for all the three inverters is derived through closed loop control implemented on C2000-F28379D micro-controller board. The Hall effect based voltage

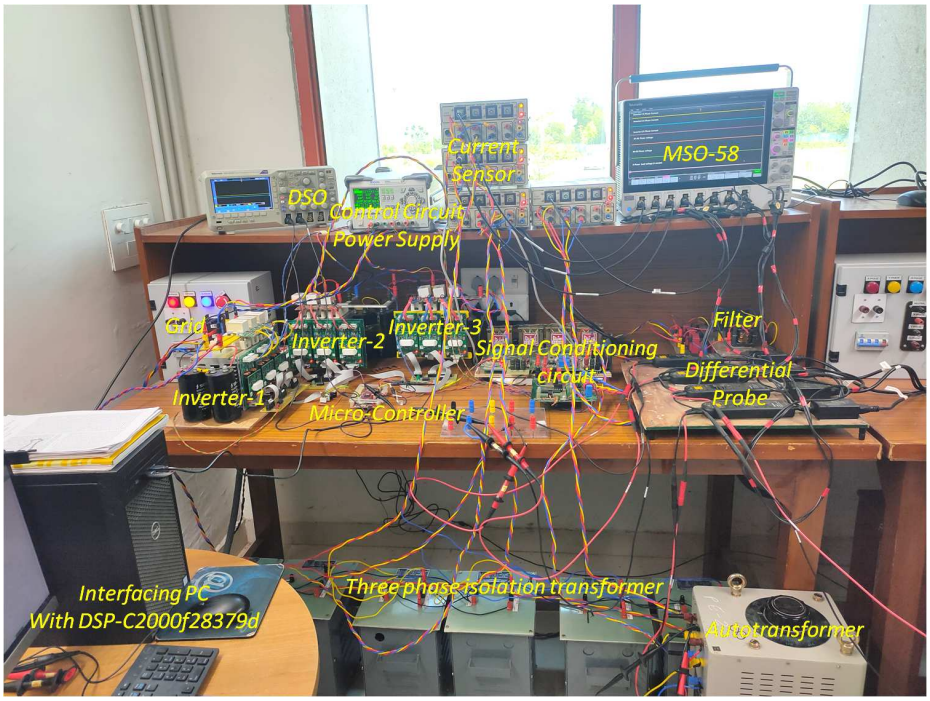


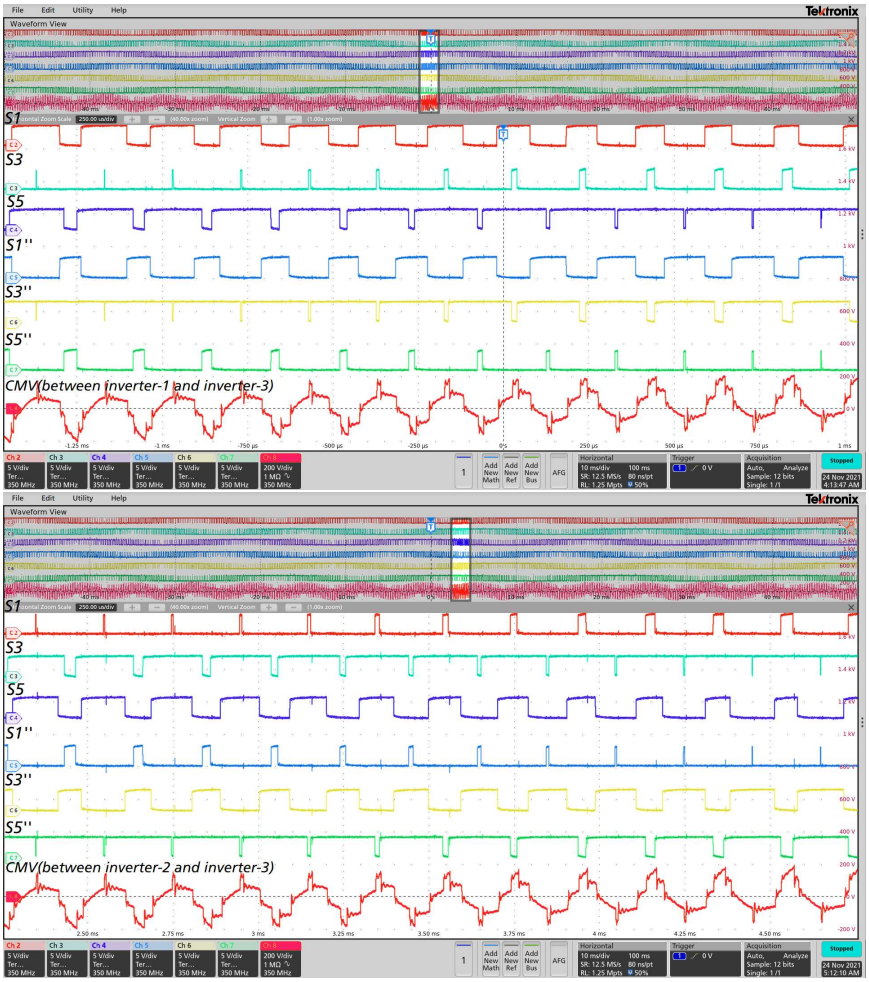
Figure 4.13: Lab-hardware set-up of proposed configuration

Table 4.3: Experimental operating parameters of proposed Configuration

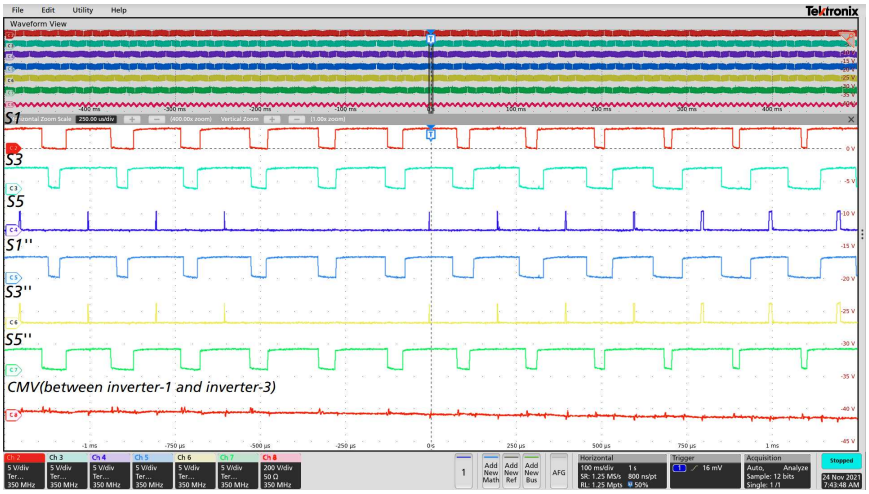
Parameter	**Value**	**Units**
Power (P)	2.4	kW
Grid phase voltage (RMS) (V_g)	115	Volt
	188(variant-1)	Volt
DC operating voltage (V_{in})	109(variant-2)	Volt
	94(variant-3)	Volt
Fundamental Frequency (f_s)	50	HZ
Switching Frequency (f_{sw})	10	kHZ
AC filter Inductance (L_p=L_s)	5	mH
Leakage inductance(1:1 transformer)	0.21	mH

(LV25P) and current (LA55P) sensors are employed to sense three phase grid voltage and grid injected current at PCC to implement the closed loop control. The switching pulses generation for proposed configurations with reference to common mode voltage elimination is demonstrated as shown in Fig.4.14 and Fig.4.15. To demonstrate the CMV elimination with proposed configuration variants clearly, the inverter-1 and inverter-2 (Fig.4.1) switched with the switching sequence mentioned in Table-4.1 and Table-4.2 for variant-1 and variant-3 respectively and third inverter switched with the conventional SVPWM in both the variants. With this switching sequence, the CMV measured between inverter-1 and inverter-3 is shown in top trace of Fig.4.14 for variant-1 and top trace of Fig.4.15 for variant-3. Similarly CMV between inverter-2 and inverter-3 for variant-1 and Variant-3 is shown in middle trace of Fig.4.14 and Fig.4.15 respectively. Further the efficacy of CMV elimination PWMs proposed for all the three inverters derived in this work for variant-1 and variant-3 is shown in bottom trace of Fig.4.14 and Fig.4.15

respectively.

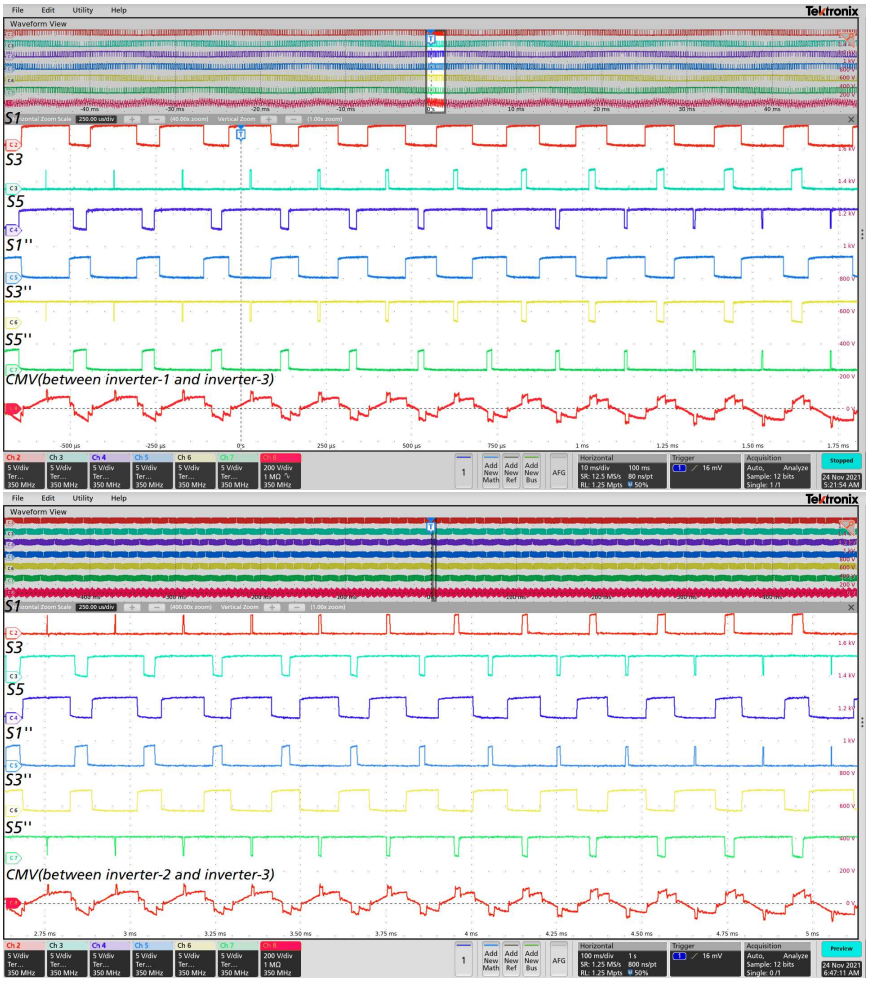


(a) The switching states of inverter-1 and inverter-3 (left) & Inverter-2 and inverter-3 (right trace) and corresponding CMV when inverter-3 switched with conventional SVPWM

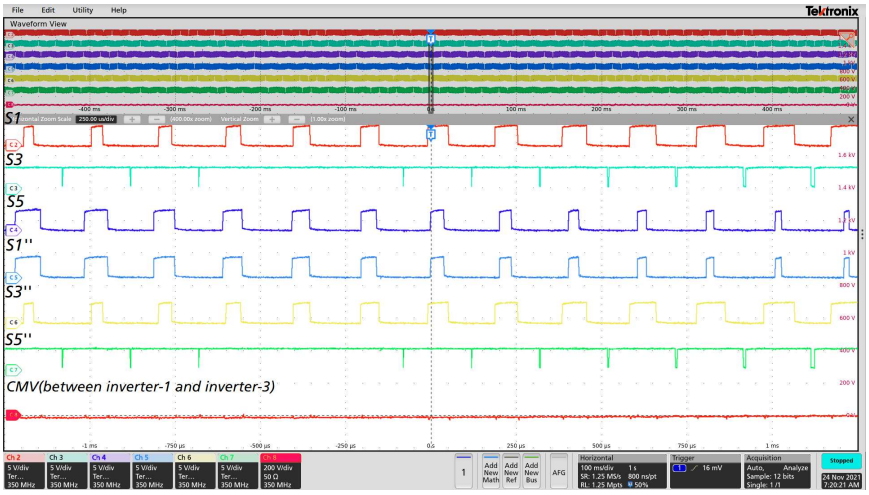


(b) The switching states of inverter-1 & inverter-3 with the proposed switching sequence and corresponding CMV(equal to zero)

Figure 4.14: The top six traces represents switching pulses of inverters (X-axis : 0.25mS/div and Y-axis:5V/div) and the bottom trace represents the common mode voltage (X-axis:0.25ms/ div and Y-axis:200V/div) of Variant-1



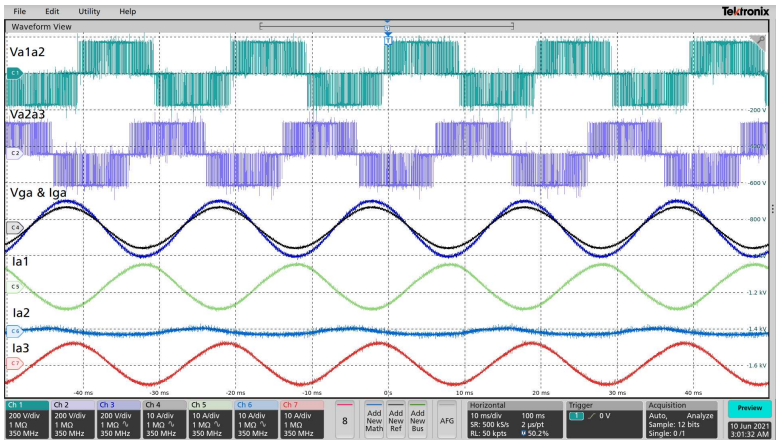
(a) The switching states of inverter-1 and inverter-3 (left) & Inverter-2 and inverter-3 (right trace) and corresponding CMV when inverter-3 switched with conventional SVPWM



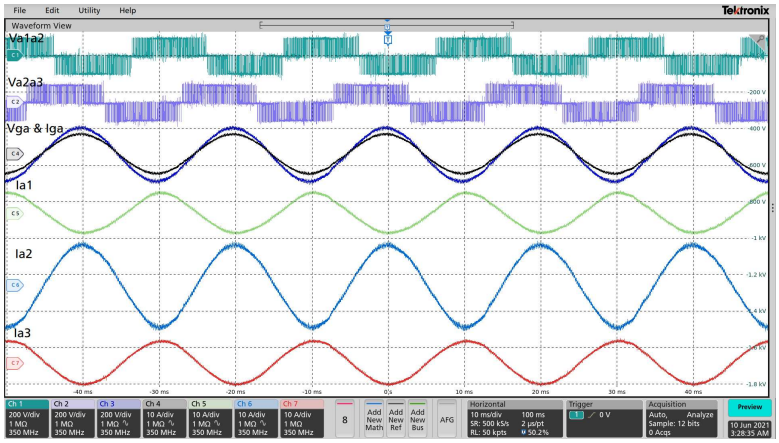
(b) The switching states of inverter-1 & inverter-3 with the proposed switching sequence and corresponding CMV(equal to zero)

Figure 4.15: The top six traces represents switching pulses of inverters (X-axis : 0.25mS/ div and Y-axis:5V/div) and the bottom trace represents the common mode voltage (X-axis:0.25ms/div and Y-axis:200V/div) of variant-3

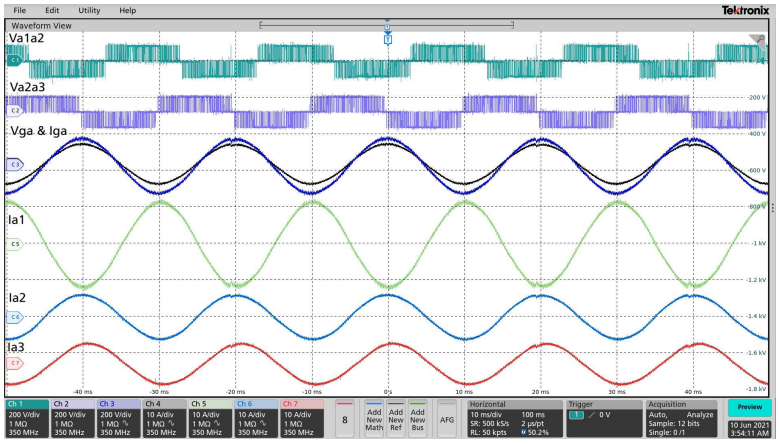
Initially to demonstrate the DC bus requirement to synthesize the grid phase voltage of



(a) Experimental results for variant-1



(b) Experimental results for variant-2



(c) Experimental results for variant-3

Figure 4.16: The transformer primary Winding-1 a-phase voltage($V_{a_1a_2}$)(1^{st} trace,unit x-axis: 10 ms/div; y-axis: 200 volts/div), Primary winding-2 a- phase voltage ($V_{a_2a_3}$)(2^{nd} trace ,unit x-axis: 10 ms/div; y-axis: 200 volts/div), a-phase grid voltage(unit x-axis: 10 ms/div; y-axis: 200 volts/div) and grid injected current(unit x-axis: 10 ms/div; y-axis: 10 Amps/div) (3^{rd} trace), a-phase primary current of inverter-1 (4^{th}), inverter-2 (5^{th} trace) and inverter-3 (bottom trace,unit x-axis: 10 ms/div; y-axis: 10 Amps/div) of proposed configuration

115 V RMS with all three variants are shown in Fig.4.16. As it is shown in Fig.4.16a, with variant-1 the AC phase voltage of 115 V is derived from the DC bus voltage of 188

Volts. With the impedance balanced switching states employed to three inverter modules, the a-phase voltage across transformer primary winding-1 and winding-2 varies between +/-188 volts as shown in 1^{st} and 2^{nd} trace of Fig.4.16a. In case of variant-2, depending upon the secondary transformer connections, the DC bus requirement is only 109V to generate the grid voltage of 115 V phase RMS. The corresponding voltage across winding-1 and 2 vary between +/-109 V as shown in 1^{st} and 2^{nd} trace of Fig.4.16b. Whereas in the case of variant-3, the DC bus requirement is further reduced to 94 Volts to derive the grid voltage of 115 V phase (RMS) and corresponding primary side winding voltages depicted in 1^{st} and 2^{nd} trace of Fig.4.16c. The a-phase grid injected current correspond to 1.5 kW (active power) with reference to a-phase grid voltage for all three variants are shown in third trace of Fig.4.16. Further, the current flowing through a-phase of the individual inverters at the primary of the transformer are shown in bottom three trace of Fig.4.16a for variant-1, Fig.4.16b for variant-2, Fig.4.16c for variant-3 with common DC bus. For all three variants, The primary side transformer currents are sinusoidal confirms no circulating currents flowing between the inverter modules even after employing the common DC bus. The consolidated performance comparison for all the three variants with reference to DC bus utilization and the circulating currents are tabulated in Table-4.4.

Table 4.4: Comparison of proposed variants

Parameter	variant-1	variant-2	variant-3
Power (P)	1.5kW	1.5kW	1.5kW
Grid phase voltage (RMS) (V_g)	115V	115V	115V
DC operating voltage (V_{in})	188V	109V	94V
Winding-1 phase Voltage(RMS)	115V	66V	58V
Winding-2 phase Voltage(RMS)	115V	66V	58V
DC bus requirement compared to conventional inverter	58%	33%	29%
Circulating current	No	No	No

Consequently the design efficacy of the closed loop controller modeled through state space analysis is demonstrated by varying active and reactive power reference for the proposed configuration. Since the controller gains and corresponding dynamic performance of the system depend only on the characteristic impedance, the closed loop performance of the variant-2 is demonstrated exclusively considering the fact all three variants exhibit same characteristic impedance. To understand the controller dynamic response, the active power reference (i_{dref}) is changed from 0 to 1.5kW and followed by 1.5 kW to 2.4 kW (shown in Fig.4.17 and Fig.4.18). As it is explained in previous section, the controller dynamics can be varied by changing the corresponding controller gains. Considering the transfer function G_{21} and G_{32}, the two sets of controller gains correspond to dynamic response 60ms and 5ms are derived as $K_p = 0.0957$ & $K_i = 259$ (for set-1) and $K_p = 0.4$ & $K_i = 1034$ (set-2) respectively. With the set-1 controller gains the system attains the steady state according to reference within 3 cycles as shown in Fig.4.17. Similarly with set-2, the dynamic response is faster and attains the steady state value within quarter cycle as shown

in Fig.4.18. Apart from the real power reference, the efficacy of controller with reference reactive power dynamics validated by changing the reactive power reference from 0 to 0.2 p.u at t=225ms. With the step change in reactive power reference, the controller dynamic response in adjusting reactive power is shown in Fig.4.19.

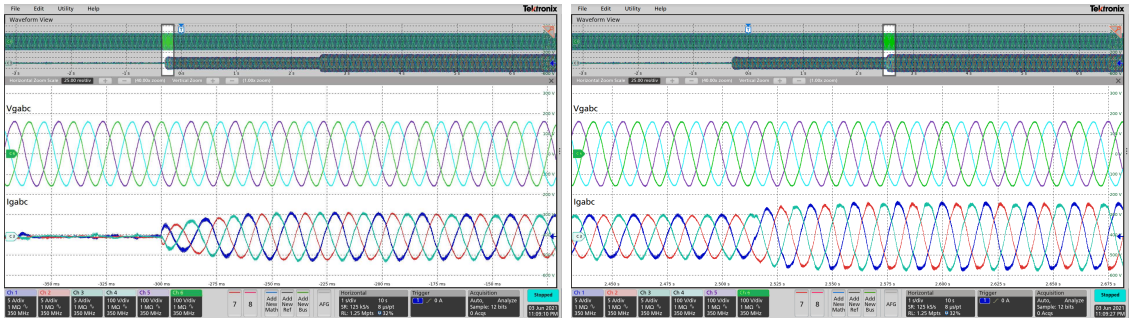


Figure 4.17: Three phase grid voltage ($V_{g_{abc}}$) (top trace, unit x-axis: 25 ms/div; y-axis: 100 volts/div) and grid injected current ($I_{g_{abc}}$) (bottom trace, unit x-axis: 25 ms/div;y-axis:5 Amps/div) with step change in i_{dref} from 0 to 0.4PU (left trace) and 0.4 PU to 0.6 PU (right trace) with K_p=0.0957 and K_i=259

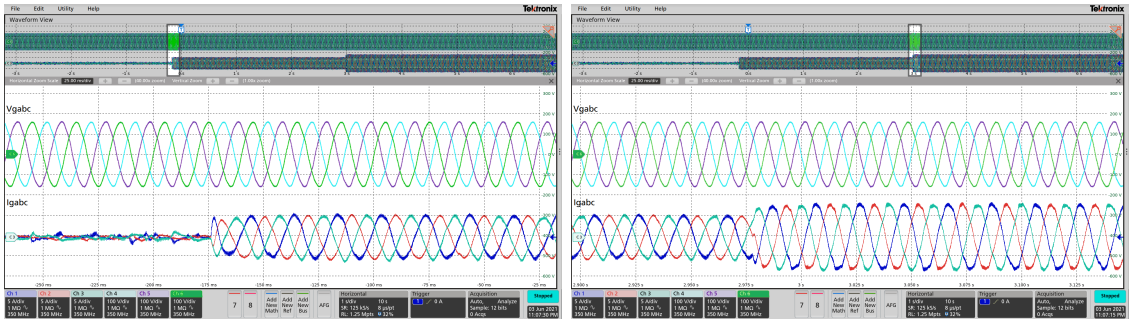


Figure 4.18: Three phase grid voltage ($V_{g_{abc}}$) (top trace, unit x-axis: 25 ms/div; y-axis: 100 volts/div) and grid injected current ($I_{g_{abc}}$) (bottom trace, unit x-axis: 25 ms/div; y-axis:5 Amps/div) with step change in i_{dref} from 0 to 0.4PU (left trace) and 0.4PU to 0.6 PU (right trace) with K_p =0.4 and K_i = 1034

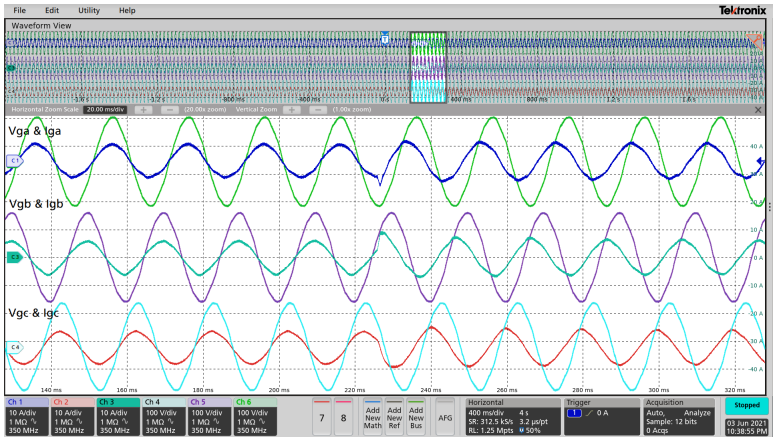
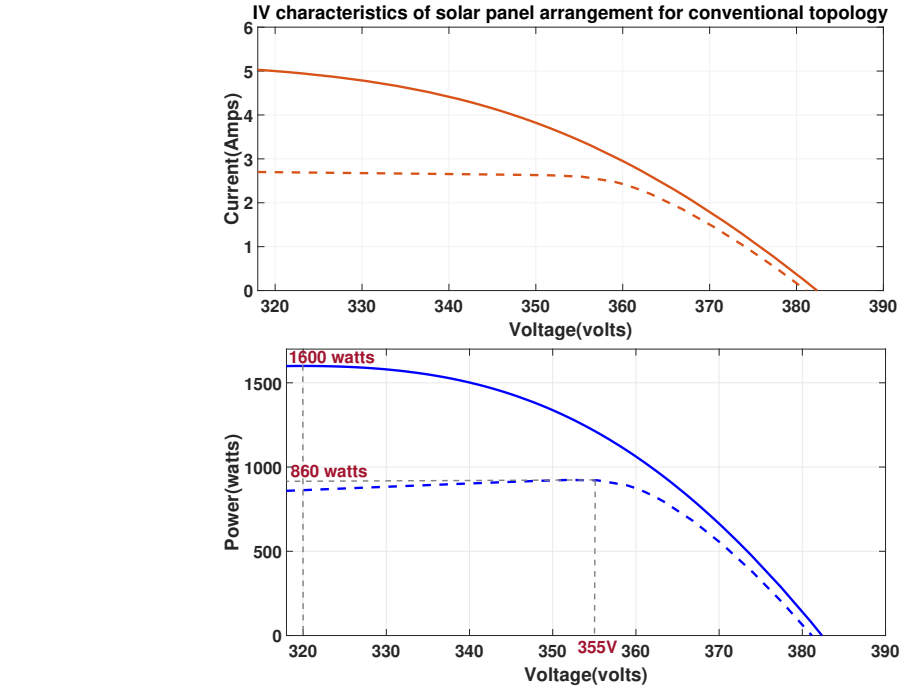


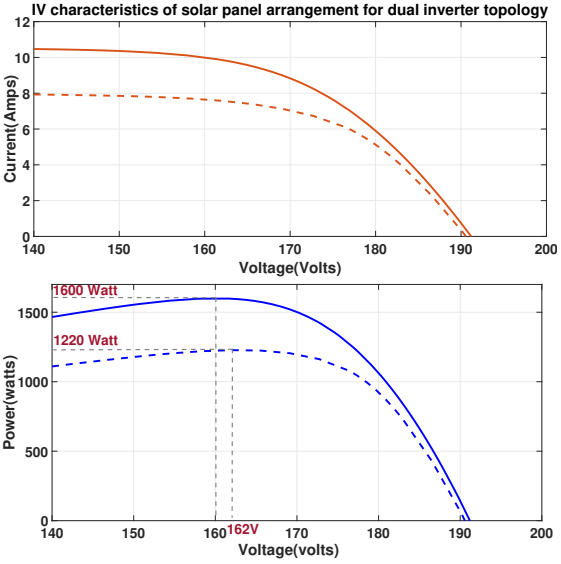
Figure 4.19: Three Phase grid voltage ($V_{g_{abc}}$, unit x-axis: 20 ms/div; y-axis: 100 V/div) superimposed on three phase grid injected current($I_{g_{abc}}$;unit x-axis: 20 ms/div; y-axis: 10 Amps/div) with step change in reactive power reference from 0 to 0.2 PU at t=225 ms

From the active and reactive power dynamics, it is evident that the designed controller for proposed configuration is robust in achieving stable operation with desired dynamic response. Finally, the features associated with the reduced DC bus voltage to generate 440V (l-l RMS) AC grid voltage along with common-mode voltage behavior are compared as shown in Table-4.5 to show the efficacy of the proposed configuration over existing topologies. As shown in Table-4.5, with the proposed configuration and devised PWM in this work, the maximum gain can be accomplished four times compared to conventional inverter topology. It indicates that only seven solar panels with a voltage rating of 24V are sufficient to generate the 440V(L-L) AC bus voltage, whereas, in conventional topology with SPWM, twenty-seven number of such solar panels are required. The reduced DC potential eases the PID effect that improves solar panels' life connected in series as per [44]-[45]. Apart from the accomplished gain, the proposed CMV elimination switching scheme offers the flexibility to operate the proposed topology with the common DC source / multiple DC and gives provision to ground DC bus as compared in Table-4.5. In addition to these features, the reduced DC bus requirement indicates connecting solar panels in parallel instead of series for the same power rating that improves the energy extraction efficiency of the solar panels during partial shading conditions. The energy extraction performance during partial shading conditions with other topologies at the same power rating are compared in Feature-6 of Table-4.5. The proposed variants are advantageous during partial irradiation condition in terms of energy yield, the energy extraction metrics comparing parallel, dual and proposed configurations is provided in Table-4.6. In all conditions the solar panels are arranged to yield the power of 1600 watt at full irradiation (1000 W/m^2). Based on the configuration, the required number of solar panels connected in series and corresponding parallel strings are depicted in Table-4.6. In all configurations, the partial irradiation is created by reducing the irradiation of two solar panels from 1000 W/m^2 to 500 W/m^2 in one string that derived the IV and PV characteristics as shown in Fig.4.20. From Fig.4.20 and Table-4.6, it is clearly evident that, during partial irradiance condition, the maximum energy yield with the proposed configuration is 1410 Watt that is 88% of maximum power. Whereas conventional parallel inverter and dual inverter configuration can extract 860 Watt (53% of maximum power) and 1220 Watt (76% of maximum power) respectively. From the discussion it is clearly evident that the proposed configuration exhibit superior performance during partial irradiance compare to other configurations mentioned in Table-4.6 due to reduced DC potential.

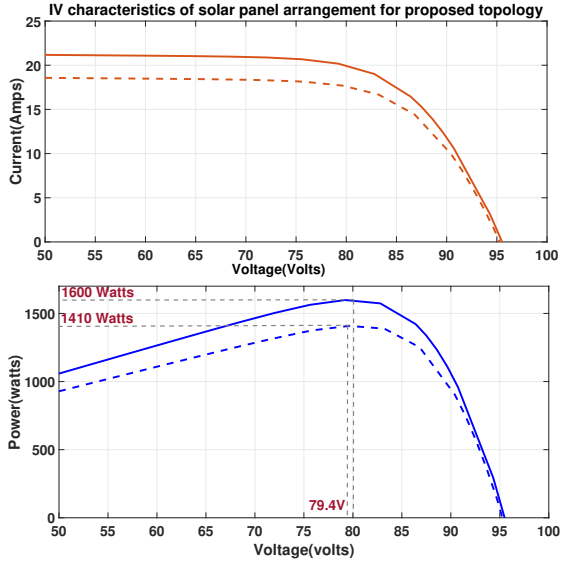
The reduced operating potential of the circuit leverages the switching devices blocking voltage capability. The reduced DC blocking capability would enhance the switching frequency of the switching devices by reducing the reverse recovery time, as shown in Fig.4.21. In Fig.4.21, IRF family switches with the same power rating at different voltage blocking capabilities are compared and observed that the higher voltage blocking capability (IRF840 Vs. IRF5210) indicates wider drift region yield longer reverse recovery time (460ns vs. 170ns). Thus, the exhibited switching frequency is relatively lower as the reverse recovery time increases with higher blocking voltage (500V vs. 100V). This clearly



(a) Parallel conventional inverter



(b) Dual inverter



(c) Proposed configuration

Figure 4.20: IV (left) and PV (right) characteristics of solar panel arrangement during full (solid line) and partial (dotted line) irradiance conditions

indicates the proposed configuration is superior in terms of operating with higher switching frequencies than conventional topologies wherein the DC bus potential requirement is higher at the same power.

Table 4.5: The performance comparison matrix between proposed topology and other conventional topologies

1. F_1(Feature-1): Required DC bus Voltage to generate 440V(L-L) AC.
2. F_2(Feature-2): Converter Voltage Gain.
3. F_3(Feature-3): Total number of series connected solar panel module (24V) to meet the desired DC bus voltage requirement.
4. F_4(Feature-4): Ability to operate with single DC source.
5. F_5(Feature-5): Existence of CMV between the inverter modules.
6. F_6(Feature-6): Maximum power extraction during partial shading (irradiation) conditions.

Topology	PWM Techniques	AC Voltage	F_1	F_2	F_3	F_4	F_5	F_6
Single stage parallel inverter[58]	SPWM	440V	650V	1(ref)	27	No	Yes	Very poor
	SVPWM	440V	560V	1.16	24	No	Yes	Poor
Dual Inverter[54]-[57]	SVPWM	440V	280V	2.32	12	No	Yes	moderate
	ZSV Elimination	440V	325V	2	14	Yes	No	moderately high
Proposed Configuration	Variant-1	440V	325V	2	14	Yes	No	moderately high
	Variant-2	440V	185V	3.53	8	Yes	No	High
	Variant-3	440V	162V	4.01	7	Yes	No	High

Table 4.6: The energy yield performance comparison table during partial irradiance condition

S.No.	Topology	No of series connected solar panel modules	No of such series connected parallel strings	DC bus voltage at		Power Extraction during		Efficiency during partial irradiation condition
				1000 w/m^2	500 w/m^2	Full irradiation $1000w/m^2$	partial irradiation $500w/m^2$	
1	Conventional Parallel Inverter	8 (8*40V=320V)	1	320V	355V	1600 Watt	860 Watt	53.75%
2	Dual Inverter	4 (4*40V=160V)	2	160V	162V	1600 Watt	1220 Watt	76.25%
3	Proposed Configuration	2 (2*40V=80V)	4	80V	79.4V	1600 Watt	1410 Watt	88.12%

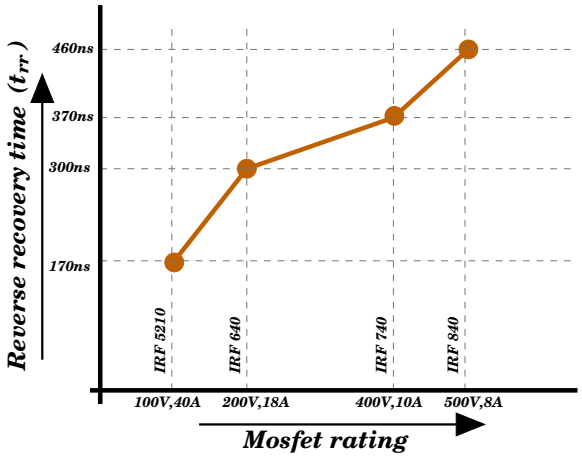


Figure 4.21: Variation of reverse recovery time (t_{rr}) of IRF family switching devices reference to voltage blocking capability

4.5 conclusion

The presented work describes the elicitation of grid voltage with reduced DC bus voltages for improved reliability of inverter and solar panels. The voltage boost phenomena is demonstrated with a series connected inverter topology consist of three inverter modules. With the proposed configuration, the voltage boost variations with reference to the grid interface transformer connections and switching algorithm is demonstrated by deriving three variant. With the elicited variants, it is observed that, the DC bus requirement is only 58% (variant-1), 33% (variant-2) and 29% (variant-3) compare to conventional grid interface inverters. The exclusive impedance balancing switching algorithms for all three variants are employed to ensure the inverter modules operate with the common DC bus. With the employed common DC bus, the efficacy of closed loop controller design is verified by perceiving the grid injected power dynamics.

Chapter 5

Conclusion

5.1 Summary

Significant contribution of the presented research work are as follows:

1. The work reported in this paper, built around deriving the positive damping for the PCC oscillations through a thorough assessment of system natural response in weak grid scenario. The natural response of the system is influenced by control parameters, impedance of system and their interactions. In stiff grid scenario, the system impedance are compensated to model the controller gains for desired injected power characteristic. Whereas in weak grid scenario, the influence of network impedance need to be assessed in the presence of system impedance to model the controller gains. The interaction between the system impedance (filter inductance and grid injected power resistance), network impedance (grid inductance) and controller gains requires multi dimensional assessment forced past researcher to derive the simplified models. Since the derived existing models are not exactly mimicking the weak grid scenario, it is required to use a secondary controls (PLL shaping, feed-forward damping, additional hardware etc) along with the current controller gain compensation for grid injected current quality shaping. But with appropriate modeling of weak grid scenario, the current controller gain compensation is sufficient to bring the positive damping to power oscillations at PCC. Considering this fact, the presented work attempted to derive the equivalent system impedance model by observing the natural interactions between the system and network impedance in synchronous reference frame. With the obtained natural response through the axis transformation principle, the current controller gain characterization is proposed to accomplish the positive damping for power oscillations at PCC by assessing the controller sampling time effect. The accomplished positive damping steers the system towards the stable region. The presented work also briefed about accomplishing the grid injected power quality as per IEEE-1547(IEEE-519) standards by tuning of the positive damping towards the natural frequency of identified equivalent system impedance model. In this work, the derived model along with the controller gain compensation is validated through hardware experimentation and MATLAB simulations on IEEE-13 bus system by creating weak grid and very weak grid scenarios in lab.

2. The proposed work described a series-solar interface inverter operating with two switching algorithms to validate DC bus minimization and CMV elimination

efficacy. With the proposed solar inverter configuration, the CMV responsible for the circulating current can be eliminated simply by choosing the two inverters' appropriate switching combinations. With the CMV elimination, the DC negative bus/DC capacitor midpoint can be connected to the ground, eases the PID effect on solar panels. Apart from the CMV complete elimination, the inherent reduced demanded DC bus voltage compared to conventional parallel inverters to synthesize the required AC bus voltage improves the inverter's overall reliability.

3. A novel high gain voltage solar interface inverter topology is also proposed aiming to reduce the DC bus voltage requirement further compare to dual inverter series topology to realize the grid voltage. The grid voltage realization and the corresponding DC bus requirement is demonstrated through three variants of proposed topology. For all three variants, the independent switching schemes are devised to accomplish the instantaneous per-phase impedance balance while synthesizing the grid voltage. With the devised switching schemes, all proposed variants are tested on hardware by employing common DC bus. Further the closed loop controller modeling is demonstrated for proposed configuration through state space analysis for stable operation at desired dynamic response.

5.2 Scope of Future Research

1. An adaptive current Controller can be implemented for weak grid coupled solar inverter using the derived plant transfer model.

2. DC bus utilization can be further reduced by extending the proposed configuration and employed in such a system where there is a restriction in DC bus potential like electric vehicles etc.

3. Different PWM techniques can be analyzed for the proposed series configuration to reduce the magnitude of leakage current in case of achieving the maximum DC gain with an isolated DC bus.

4. Different MPPT techniques can also be realized to extract the maximum power in case of partial shading conditions for the novel proposed configuration.

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