Device-to-Circuit Co-optimization of Two-Dimensional Material-based Field-Effect Transistors for Future Technology Node

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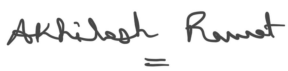
Dedicated to My Loving Family

Declaration of Originality

I hereby declare that the work which is being presented in the thesis entitled **Device-to-Circuit Co-optimization of Two-Dimensional Material-based Field-Effect Transistors for Future Technology Node** has been solely authored by me. It presents the result of my own independent investigation/research conducted during the time period from July, 2018 to October, 2023 under the supervision of Dr. Brajesh Rawat, Assistant Professor, Department of Electrical Engineering. To the best of my knowledge, it is an original work, both in terms of research content and narrative, and has not been submitted or accepted elsewhere, in part or in full, for the award of any degree, diploma, fellowship, associateship, or similar title of any university or institution. Further, due credit has been attributed to the relevant state-of-the-art and collaborations (if any) with appropriate citations and acknowledgments, in line with established ethical norms and practices. I also declare that any idea/data/fact/source stated in my thesis has not been fabricated/ falsified/ misrepresented. All the principles of academic honesty and integrity have been followed. I fully understand that if the thesis is found to be unoriginal, fabricated, or plagiarized, the Institute reserves the right to withdraw the thesis from its archive and revoke the associated Degree conferred. Additionally, the Institute also reserves the right to appraise all concerned sections of society of the matter for their information and necessary action (if any). If accepted, I hereby consent for my thesis to be available online in the Institute's Open Access repository, inter-library loan, and the title & abstract to be made available to outside organizations.



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Akhilesh Rawat

Certificate

This is to certify that the thesis entitled **Device-to-Circuit Co-optimization of Two-Dimensional Material-based Field-Effect Transistors for Future Technology Node**, submitted by **Akhilesh Rawat (2018EEZ0011)** for the award of the degree of **Doctor of Philosophy** of Indian Institute of Technology Ropar, is a record of bonafide research work carried out under my (our) guidance and supervision. To the best of my knowledge and belief, the work presented in this thesis is original and has not been submitted, either in part or full, for the award of any other degree, diploma, fellowship, associateship or similar title of any university or institution.

In my opinion, the thesis has reached the standard fulfilling the requirements of the regulations relating to the Degree.

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Lay Summary

In the realm of cutting-edge technology, the search for new materials that can enhance electronic devices is being conducted by researchers. A promising group of materials known as two-dimensional materials (2DMs), such as MoS_2 and WS_2, has been discovered. These materials could potentially enable the creation of significantly improved, smaller electronic devices. The excitement surrounding these materials arises from their similarity to silicon, which has been a staple in the production of electronic gadgets for a long time. However, a challenge exists: understanding how to fully utilize these materials is still being worked on.

This research is centered around three main questions: (i) Which 2DM is more promising for short-channel devices? (ii) What occurs when these materials encounter non-idealites in fabrication process? and (iii) how do 2-D materials compare to the existing silicon technology? To answer these questions, computer simulations are used to investigate the performance of 2DMs in tiny transistors, which serve as the building blocks of electronic devices. It is discovered from the results that certain 2DM-based transistors could excel at creating the logical components of the devices, such as smartphones and computers.

Investigations are also conducted to understand the impact of minor issues in these materials and how they perform in extremely small transistors. Surprisingly, some 2DM-based transistors outperformed their silicon counterparts in these minuscule transistors. Finally, an assessment is made of how these materials function in circuits, similar to those found in electronic gadgets and it is observed that the chips made from 2DMs have the potential to surpass those made from silicon.

So, in simple terms, this research assists in understanding how to utilize these new materials to create electronic devices that are faster and more efficient. It is akin to the process of learning how to create superior tools for the future.

Abstract

The quest for new materials capable of scaling beyond the limits of silicon has led to the emergence of two-dimensional materials (2DMs) in the device landscape. Notably, 2DMs, such as MoS_2, WS_2, BP, InSe, and others, have shown remarkable performance and emerged as prominent contenders for ultra-scaled CMOS devices due to their carrier mobility comparable to silicon, ease of large-scale fabrication using CMOS-compatible processing techniques, and feasibility of three-dimensional integration. Despite significant progress in the development of 2DM-based field-effect transistors (FETs), the processing technology is still in its early stages. As recent experimental progress unfolds, several pertinent questions arise before the development of integrated circuits: (i) How do we select the specific 2DM from a family of over 1800 options?; (ii) What role do non-idealities, such as interface traps, high contact resistance, and phonon scattering, play in device-to-circuit level performance?; and (iii) How do they compare to existing Si CMOS technology?. This thesis aims to address these questions through a comprehensive modeling approach that encompasses device-to-circuit level analysis.

The main objective of this research is to undertake device-to-circuit level co-optimization of 2DM-FETs. To achieve this, a dissipative quantum transport simulation framework is developed to accurately estimate the performance of 2DM double-gate (DG)-FETs. The quantum simulation is conducted by self-consistently solving the 2-D Poisson's equation with diffusive non-equilibrium Green's function formalism (NEGF) under the self-consistent Born approximation method. Using this developed framework, a study is conducted on various 2DM-FETs to evaluate their suitability for digital applications at both the device and circuit levels. It is found that materials with moderate transport effective mass and moderately high transverse mass are better suited for digital logic applications. Subsequently, the quantum transport modeling framework is extended to describe the interface trap states in MoS_2-FETs by introducing 0-D states with a bandgap. The analysis reveals that the trap-induced inelastic tunneling current strongly affects the OFF-state current, threshold voltage, and subthreshold slope for gate lengths below 18 nm, while charge trapping marginally reduces the ON-state current of MoS_2-FETs. Furthermore, a well-calibrated 3-D TCAD tool is employed to thoroughly analyze and optimize the performance of 2DM stacked gate-all-around nanosheet (NS)-FETs. The study indicates that single-layer (SL) and bilayer (BL) MoS_2 NS-FETs exhibit more favorable switching characteristics compared to Si NS-FETs for sub-5 nm nodes. Finally, CMOS inverters based on 2DM DG-FETs are explored

and benchmarked against conventional Si-based devices. The study finds that the heterogeneous WSe_2-MoS_2 CMOS inverter shows more suitability for logic applications with larger noise margins, nanowatt power dissipation, and comparative delay to Si-based inverter.

By addressing these research objectives, this work contributes to the understanding and optimization of 2DM-FETs at the device and circuit levels, paving the way for their potential integration into future electronic systems.

Keywords: Two-Dimensional Materials (2DMs); Non-Equilibrium Green's Function Formalism (NEGF); MoS_2-FET; Interface trap state, Gate-all-around FET; CMOS Inverter

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Chapter 1

Introduction

1.1 Historical Evolution of Semiconductor Devices

With the introduction of the transistor in late 1947, a significant turning point marked the culmination of the vacuum tube era, signaling its impending replacement by emerging semiconductor electronics. During this period, the scientific community had limited familiarity with semiconductor technology. It was at this juncture that the Bell Labs team, under the leadership of W. Shockley and S. Morgan, made a pivotal decision to focus their research on two of the most basic semiconductors: silicon and germanium. This decision proved to be astute, as just two years later, they successfully achieved the milestone of creating the first functional transistor. However, at the time, the underlying theory governing this remarkable device remained shrouded in mystery. Clarity arrived when W. Shockley articulated the long-sought-after theory, elucidating the principles behind the transistor's operation. During the 1950s, a surge of enthusiasm swept through the scientific and engineering communities as they were drawn to the immense potential and the prospect of controlling powerful semiconductor materials. The momentum behind semiconductor research received a significant boost in 1956 following the awarding of the Nobel Prize in Physics to W. Shockley, W. Brattain, and J. Bardeen, recognizing their pioneering work on semiconductors and their pivotal discovery of the transistor effect. In 1952, I. Ross and G. Dacey achieved a significant milestone by successfully bringing to life the first unipolar transistor, a concept initially patented by Lilienfeld in 1926 [1]. Following this achievement, another groundbreaking development took place in 1960, when Bell Labs, led by the group of M. M. Atalla, reached a pivotal moment in the field by inventing the first MOSFET [2].

Subsequently, the next significant leap occurred at Fairchild Semiconductors when J. Hoerni introduced the planar process for transistors, marking a major breakthrough. This innovation was leveraged by R. Noyce, who successfully employed it to construct an integrated circuit (IC) in 1959 [3]. From the year 1960 until the early 2000s, in accordance with Dennard's scaling guidelines, the semiconductor industry successfully reduced the size of MOSFET devices at an exponential rate as foreseen by Moore's prediction in 1965 [4, 5]. However, it is worth noting that an intriguing transition occurred when the

industry reached the 130 nm node, signifying the conclusion of the traditional Dennard scaling. This marked the commencement of a new era known as “More Moore.” In this era, the fundamental complementary metal-oxide semiconductor (CMOS) principles remained unchanged, but novel technological advancements were introduced to enable further miniaturization of transistors.

1.2 Challenges in Silicon (Si) MOSFETs and Emergence of 2-D Materials

Aggressive scaling of CMOS technology enables remarkable enhancements in the performance, density, capabilities, and cost of microprocessors. However, in the current technological landscape, as the nanometer realm is ventured, it increasingly challenges the ability to further reduce device sizes while maintaining the advantages in performance. Major problems with the current silicon (Si) MOSFETs are parameter fluctuation of nominal identical transistors, adverse short channel effects (SCEs), and the deteriorating effect of parasitics [6].

In the last decade, significant efforts have been undertaken to prolong the lifespan of Si-MOSFETs. This has been achieved through the introduction of new manufacturing processes or improvements in existing technology, including strain engineering, reducing clock frequencies, and the advancement of stacked gate-all-around (GAA) nanosheet field-effect transistors (NS-FETs) [7, 8, 9]. These architectural solutions are currently beneficial, but the pursuit of physical dimensions approaching the ”deeper nanoscale” realm, specifically beyond 12 nm (at the 1 nm technology node), poses a formidable challenge within the confines of existing technologies. The Chip manufacturers have transitioned from the 7-nm to the 5-nm scale. However, the ongoing quest for enhanced performance encounters progressively diminishing returns [6] due to: (i) the mounting challenge in reducing the supply voltage further is primarily attributed to the inherent limitation imposed by the subthreshold swing (SS), (ii) increasing leakage current resulting from adverse SCEs, (iii) density improvement that approximates 1.6× rather than the anticipated 2×, and (iv) the necessity for additional circuitry to monitor and adapt to variations in performance. Thus, to maintain Moore’s law and to ensure the evolution of semiconductor technologies, the major device communities are looking toward novel materials and entirely distinct transistor architectures that can ensure performance improvement with reduced transistor sizes.

The quest for a new material, which allows the device to scale beyond the end of the road map for Si has led to the emergence of two-dimensional (2-D) Materials

(2DMs) in the device landscape. The emergence of graphene in 2004 has ignited the research works in 2DM-based electronics [10]. However, the absence of band gap in graphene limits its applications as a channel material for digital logic applications [10], but it inspired the discovery of other 2DMs, including monolayer MoS_2 in 2011 [11]. Since then, other transition metal dichalcogenides (TMD), such as WS_2, WSe_2, $MoSe_2$, etc. have emerged with single or few-layer channels. Especially, molybdenum disulfide (MoS_2) has emerged as a leading candidate for ultra-scaled CMOS devices in the realm of post-silicon electronics. This is primarily attributed to its carrier mobility, which is on par with silicon, its ease of large-scale fabrication with CMOS compatible processing techniques, and three-dimensional (3-D) integration feasibility [12]. These outstanding electronic properties make 2-D MoS_2 a potential material for scaling down the device dimension to a few nanometers range without encountering adverse SCEs.

Particularly, in the early stages of 2DMs fabrication technology development, modeling proves to be a highly valuable tool for assessing various technology choices and device configurations. A grasp of the fundamental physics facilitates optimization at both material and architectural levels, potentially reducing development costs by streamlining the time and effort required to transition from design to functional prototype fabrication. Consequently, this thesis employs quantum transport modeling to address several pivotal concerns related to variability and parasitics, as well as to assess diverse strategies for enhancing the performance of 2DM-based FETs. Further, well-calibrated rigorous 3-D TCAD simulation has been utilized to assess and predict the performance potential of stacked GAA NS-FET with 2DMs. Lastly, a comprehensive circuit-level performance benchmarking of 2DM-based CMOS inverter configurations is performed to assess their suitability and performance for ICs. This evaluation serves as a guiding reference for experiments and aims to stimulate additional research initiatives.

1.3 Transistor Performance Metrics and Trade-offs

Semiconductor devices find significant applications in two primary domains: digital ICs and radio-frequency (RF) ICs. Digital ICs are constructed using logic gates, such as NOR and NAND gates, which employ both p-type and n-type transistors in combination to execute specific logical operations. The control of these gates allows transistors to function as switches, conducting high currents in the “on” state and very low currents in the “off” state. Given the diverse range of expectations and requirements, it becomes valuable to establish Figure of Merits (FOMs) which encompass critical facets of transistor

performance, spanning from the device level to the circuit level. Additionally, these FOMs outline the essential criteria and obstacles that need to be addressed to successfully integrate 2DMs into semiconductor devices.

■ The application of gate voltage to the channel is essential for utilizing FETs as switches, and this necessitates a high current value in the ON-state and a low value of in the OFF-state. A substantial ON-state current facilitates the rapid charging of capacitive loads, typically comprising the gates of one or more following transistors. Conversely, a low OFF current minimizes leakage current, which predominantly governs static power dissipation. The ON/OFF current ratio stands as a critical FOM for digital switches, with greater values signifying superior performance. According to the 2021 requirements outlined by the International Roadmap for Devices and Systems (IRDS), 1nm technology node multigate MOSFETs are expected to possess an ON-state current of 1750 $\mu A/\mu m$ and an ON/OFF current ratio within the range of $10^5 - 10^7$ for high-performance logic applications [13]. Achieving such an ON/OFF ratio is dependent on the semiconductor nature of the transistor channel and featuring a sufficiently wide energy gap.

■ Another significant FOM used to evaluate switching characteristics is the subthreshold swing (SS). It quantifies the the rate at which the current increases below the threshold voltage (i.e., when $V_{GS} < V_{TH}$ for n-FETs).

$$SS = \frac{dV_G}{d(\log_{10}(I_{DS}))} \tag{1.1}$$

where, SS is typically measured in millivolts per decade of current (mV/dec), V_G is the gate voltage and I_{DS} represents the drain to source current. A steeper subthreshold slope indicates a quicker transition between the OFF-state and ON-state. Ideally, SS should be as small as possible, and for conventional Si MOSFETs, its lower limit is typically 60 mV/dec.

■ The drain-induced barrier lowering (DIBL) is assessed by computing the change in the threshold voltage (V_{TH}) between the drain voltages $V_{DS} = 0.05$ V and $V_{DS} = 0.5$ V and normalizing it by ΔV_{DS}.

■ The intrinsic device delay ($\tau = C_g V_{dd}/I_{ON}$) serves as another critical metric for evaluating the switching behavior of the device. Here, C_g, V_{dd}, and I_{ON} represent the gate capacitance, supply voltage, and ON-state current, respectively. It highlights the inherent constraints on the switching speed of the device and its ability to operate for AC applications.

■ The power delay product (PDP) represents a vital metric for evaluating the switching performance of a device. It quantifies the energy expenditure needed for the

transition from the ON- to OFF-state. Additionally, it serves as an indicator of the dynamic power dissipation (P_{dyn}), with the relationship $P_{dyn} = \alpha \text{PDP} f$, where f denotes the operating frequency, and α represents the activity factor.

■ One of the crucial static performance metrics for the basic CMOS digital block includes maximum DC gain. In the context of multistage logic circuits, an inverter with a maximum DC gain exceeding 1 is highly desirable due to its ability to enhance circuit robustness against errors and promote regenerative behavior.

This thesis primarily focuses on exploring the potential utility of 2DMs in the context of logic transistors, consequently restricting the discussion to parameters pertaining to both device and circuit levels.

1.4 State-of-Art of Two-Dimensional Material MOSFETs

Single atomic thick 2DMs have emerged as highly attractive candidates for beyond-silicon electronics, owing to their exceptional mechanical and electronic properties, including high electrical and thermal conductivities, their ultra-thin surfaces devoid of dangling bonds [12], [14]. Additionally, their relatively high carrier effective mass effectively suppresses direct source-to-drain tunneling current, which minimises the OFF-state leakage. Further, weak inter-plane van der Waals (vdW) bonds facilitate the easy detachment of individual layers without damage, allowing transfer to various substrates effortlessly [15].

In recent years, substantial advancements have been made in the experimental fabrication of 2DM-FETs [12], [14]. Studies focusing on materials such as MoS_2, WS_2, and WSe_2 have exhibited impressive switching capabilities with ON/OFF current ratios ranging from 10^4 to 10^6 for sub-10 nm channel lengths [16, 17, 18]. Particularly noteworthy is the recent achievement of an exceptional ON/OFF ratio of 10^6 in MoS_2-FETs, even at a physical gate length of 1 nm [19]. These findings underscore the promising potential of 2DMs in realizing high-performance FETs for post-silicon electronics. Theoretical investigations further support this notion, showing competitive speed and lower switching energy compared to III-V compound and traditional Si MOSFETs, especially for sub-5 nm technology node [20], [21].

Despite the promising performance of MoS_2-FETs, there are several significant challenges in realizing high-performance 2DM-FETs for future technology node. These include:

- Recent research has uncovered a diverse range of 2DMs beyond graphene,

with metallic, semiconducting, and insulating properties. These materials can be classified into various categories, including X-enes, X-anes, Fluoro-X-enes, TMDs, Semiconductor-Metal Chalcogenides (SMCs), MX-enes, Group-IV Monochalcogenides, Janus 2DMs, and III-V Compounds [22]. Finding the most promising 2DM: With a vast family of over 1800 materials, identifying the most suitable and promising 2DM for specific applications remains a challenge. Further research is needed to explore and evaluate the performance characteristics and suitability of different 2DMs.

- Early works on MoS_2-FETs predominantly focused on single-gate structures, with limited attention given to stacked multigate architectures [23]. Recent experimental efforts have showcased the performance potential of MoS_2 in 2-layer and 3-layer stacked single MoS_2-based NS-FETs, with gate lengths around 370 nm [24] and 540 nm, respectively [25]. TSMC recently accomplished the integration of MoS_2 in a GAA nanosheet nFET with a gate length of 40nm, demonstrating an impressive ON-state current of 410 μA/μm at 1 V drain voltage [26]. These advancements open up new possibilities for incorporating MoS_2 into 3-D multigate FET structures, presenting exciting prospects for further improving device performance and integration capabilities.

- Fabricated MoS_2-FETs, regardless of the type of gate oxide employed (HfO_2, Al_2O_3, SiO_2), have reported interface trap densities (D_{IT}) in the range of 10^{11}-10^{13} cm^{-2} eV^{-1} [27, 28, 29, 30]. These trap charges introduce undesirable obstacles to MoS_2-FET performance, including mobility degradation, diminished electrostatic control, trap-assisted tunneling, and temperature instability. The presence of sulfur vacancies at the oxide-MoS_2 interface has been found to mainly contribute to distributed shallow trap states within the bandgap energy range of MoS_2 [31], [32]. However, many simulation models have disregarded the impact of interface charge, resulting in an overestimation of MoS_2-FET performance [33], [34]. It is crucial to undertake meticulous analysis of interface trap states and modeling to minimize their adverse effects and optimize device performance.

- The integration of 2DMs in CMOS inverters has witnessed rapid progress. Initially demonstrated with monolayer graphene, CMOS inverters faced limitations due to high leakage current resulting from the zero energy gap of graphene [35]. However, subsequent developments utilizing single 2DM sheets, such as MoS_2, WSe_2, and BP,

through chemical, electrostatic, and doping of contact metal work function, have shown remarkable switching dynamics and improved electrostatic characteristics [15, 36, 37, 38]. Furthermore, there has been active exploration of heterogeneous CMOS inverter configurations that incorporate diverse layered materials for the channel. Examples include nMOS with MoS_2 and pMOS with α-$MoTe_2$, BP, WSe_2, and Si nanowires. These efforts aim to attain improved noise margin, higher gain, and enhanced speed in semiconductor devices [15], [39]. Notably, there has been substantial interest in p-type WSe_2- and n-type MoS_2-based CMOS inverters, especially for their applications requiring high gain and low power (LP). This interest is fueled by their exceptional electron and hole mobilities at room temperature, which surpass those of other 2DM-FETs [40], [41].

Addressing these challenges will be instrumental in unlocking the full commercial potential of 2DM transistors and advancing their integration into various electronic devices and systems. In conclusion, the exceptional properties of 2DMs have positioned them as highly promising candidates for post-silicon electronics. Extensive experimental studies have showcased their excellent switching performance, while ongoing research addresses challenges related to interface trap charges and explores their integration into multigate FET structures. Additionally, the development of CMOS inverters based on these materials shows a significant performance potential for achieving high-performance and low-power ICs.

1.5 Problem Definition

2DMs have shown significant potential for next-generation electronic devices [42]; yet, numerous technological challenges remain unresolved. Due to their atomic-scale thickness, 2DMs possess intrinsic physical properties that are highly susceptible to the effects of device fabrication, material integration, and processing procedures. Numerous significant challenges must be addressed before the successful integration of 2DMs into commercial devices can be achieved. These include the mitigation of defects and impurities, the reduction of contact resistance between 2DMs and metals, and the minimization of parasitic effects [12]. Nevertheless, the swift advancements in device fabrication technology and material synthesis in recent years presents optimistic possibilities for a future where nearly ideal devices with minimal non-idealities can be achieved [43], [44]. The present focus of this research is driven by extensive performance benchmarking and rigorous optimization of materials and device design parameters in

2DM-FET under the presence of non-idealities, such as contact resistance, electron-phonon scattering, and interface trap charges at the device and circuit level.

The objective of this thesis is to tackle the specific aspects of 2DM-based transistors using numerical modeling, with a focus on their relevance to future integrated circuit applications. These specific aspects include:

■ Development of atomistic and multiphysics diffusive quantum transport model for 2DM-FETs.

■ Finding the suitable 2DM from a family of more than 1800 exfoliable 2DMs.

■ Investigation of the impact of interface trap in the performance of monolayer MoS_2-FET.

■ Investigation of 2DM-based 3-D multichannel MOSFET performance and comparison with existing Si-based MOSFET.

■ Investigation of 2DM-based devices performance in CMOS inverter configurations and comparison with existing Si-based CMOS inverter.

1.6 Thesis Framework Overview

The thesis is structured into seven chapters, each of which serves the following purposes:

Chapter 1 provides a concise overview of the thesis, encompassing its rationale, problem statement, and a comprehensive summary of the content.

Chapter 2 presents a concise overview of the developed dissipative quantum transport model for 2DM-FETs. To capture all intricate atomic level phenomena, initially a DFT-based atomistic model is established for 2DMs. This model is employed to ascertain critical parameters such as band effective mass, dielectric constant, lattice constant, and energy gap. After obtaining material attributes, the dissipative quantum transport simulation is built upon the self-consistent solution of 2-D Poisson's and non-equilibrium Green's function (NEGF) formalism all within the self-consistent Born approximation (SCBA) method for incorporating scattering mechanism. To begin, the NEGF approach for quantum transport in MoS_2 is introduced by employing a 1-D tight-binding Hamiltonian matrix. Following that, the modeling framework developed to model the electron-phonon scattering mechanism is discussed. Lastly, the developed transport model undergoes verification by comparing it to the results of previous simulations.

Chapter 3 delves into the investigation of device-to-circuit level performance for a

range of 40 emerging 2DMs and conventional TMDs, including MoS_2, WS_2, and WSe_2. The performance analysis is conducted employing a multi-scale modeling methodology based on the NEGF approach, which seamlessly connects and integrates three design levels: material, device, and circuit. Further, the chapter investigates the performance of 2DMs in three key digital circuits, CMOS inverter, 6-T static random-access memory (SRAM) cell, and 32-bit arithmetic logic unit (ALU). The primary objective is to explore the performance limitations and advantages offered by these novel 2DMs in digital applications, with a particular focus on their superiority over silicon counterparts.

Chapter 4 begins by introducing a quantum-mechanical framework for modeling interface trap states in MoS_2-FETs. The framework incorporates 0-D states within the self-consistent solutions of dissipative NEGF and Poisson's equations, allowing for a comprehensive description of both single and multiple interface trap states. The position, energy level, and area of the trap states are specified within this unified framework. The chapter explores the impact of trap energy and position on the transfer characteristics (I_{DS} - V_{GS}) of MoS_2-FETs. It then proceeds to investigate the effect of a single interface trap site on the key short-channel performance metrics and its temperature dependency. Furthermore, the chapter explores the degradation of MoS_2-FET performance in the presence of multiple interface traps. Finally, the chapter determines the threshold voltage (V_{TH}) and low field electron mobility (μ_n) for various interface trap densities (D_{IT}), and verifies the obtained μ_n by comparing it to reported experimental results for different trap densities.

Chapter 5 focuses on the analysis and design of 3-D integration of single-layer (SL) and bilayer (BL) MoS_2 in stacked GAA NS-FETs. The chapter primarily centers around the comparative analysis of multichannel stacked SL-MoS_2 and BL-MoS_2 NS-FETs with Si NS-FETs of various widths, highlighting their potential performance benefits. Initially, the chapter introduces a 3-D TCAD simulation methodology that accurately describes electronic transport in both MoS_2 and Si NS-FETs, achieving high computational efficiency and adaptability while maintaining accuracy. Subsequently, it explores the advantages of SL-MoS_2 and BL-MoS_2 NS-FETs over Si NS-FETs for logic applications, comparing important metrics such as I_{ON}, SS, intrinsic speed, and switching energy. This chapter also discusses the scaling trends of these logic switching advantages with respect to the technology node.

In Chapter 6, a detailed investigation is done to analyse the performance of CMOS inverters that employ 2DMs, specifically MoS_2, WS_2, WSe_2, black phosphorus (BP),

and WSe_2-MoS_2. Additionally, their performance is also benchmarked with that of SI-based counterparts for channel lengths below 10 nm. This chapter begins by examining the transfer characteristics and short-channel performance metrics of pMOS-FET and nMOS-FET based on 2DMs and Si. It then proceeds to analyze the static performance metrics, such as gain and noise margin, as well as dynamic performance metrics, including delay, power, and power-delay product (PDP) for both 2DM-based and Si-based inverters. Finally, this chapter explores the inverter performance dependence on supply voltage (V_{DD}), contact resistance, interconnect resistance and capacitance, parasitic capacitances, and device scaling.

Chapter 7 primarily concludes the research and provides a framework for potential avenues of future work, with a particular focus on modeling perspectives.

1.7 Novel Findings in this Thesis

Given that devices relying on 2DMs are still in the developmental phase, the work in this thesis contributes in numerous ways to the field of modeling, physics, and application for 2DM-based transistors. The primary contributions and corresponding novel findings are outlined as follows.

■ The initial phase of this work centers around the development of a dissipative quantum transport model for 2DM-FETs with a focus on the reduction in the computational burden.

- The main step involved in accurately modeling the electronic properties through NEGF is the identification of a suitable tight binding Hamiltonian model as it describes the bandstructure of device and also decides the computational cost associated with iteratively solving NEGF equations. Thereby, a 1-D elementary cell is identified along the width direction. This simplification largely reduces the computational cost and provides similar results with full real-space calculation for 2DM-FET, when the potential along the width direction is uniform.

- The other advantage of 1-D unit cell assumption is that it enables a computationally efficient transport model, which facilitates extensive investigations across a wide range of 2DMs.

- Further, the various 2DM-FETs can be expressed by the same Hamiltonian, by simply replacing the material attributes such as dielectric constant, bandgap, lattice constant, electron or hole effective mass.

- The modeling of the electron-phonon scattering mechanism using the SCBA loop is performed by utilizing the convergence criteria of the electron correlation function (G_n) and retarded Green's function (G) for both inelastic and elastic scattering. The convergence criterion is set to a value of ($\Delta < 0.001$) to ensure current conservation in the device.

- To ensure the accuracy of the convergence process in the SCBA loop current is monitored throughout the device, as the current between two adjacent grid points along the channel should remain constant in a self-consistently converged SCBA loop.

■ Motivated by the demand for high speed and low power consumption with high integration density in the electronic system, device-to-circuit level performance of emerging 40 2DMs is investigated using a multi-scale modeling methodology based on the NEGF approach.

- The selection of the most suitable two-dimensional material for digital applications necessitates a meticulous assessment and rigorous optimization process, considering key material attributes like effective masses in both the transverse and transport directions, as well as the bandgap. These attributes exhibit a closely interconnected influence on various critical factors, including the velocity of charge carriers, tunneling probability across the channel potential barrier, density of states (DOS), and quantum capacitance (C_q).

- The findings indicate that 2DMs with moderately low effective mass in the transport direction and high transverse effective mass could be better suited as a channel material to achieve higher ON-state current.

- The results reveal that five 2DMs, such as GeTe, PbS, Sn_2S_2, $Ti_2N_2Cl_2$, and $Ti_2Br_2N_2$, have promised excellent switching performance with higher ON-state current, lower device delay, and lower power delay product.

- The results suggest that certain 2DMs, such as Tl_2S, MoSeTe, Ag_2I_2, SnS_2, Ti_2N_2, and $Ti_2Br_2N_2$, GeTe, give symmetric ON-state current for both NFET and PFET, which makes them a favorable choice for CMOS technology as they could provide an innate solution to the NFET and PFET size matching issue.

■ With the increasing demand to understand the factors affecting the transfer characteristics of short-channel MoS_2-FET for overcoming the variability issue, a modeling

framework is introduced that describes the interface trap state in MoS_2-FET. This framework incorporates the description of interface trap states into the self-consistent solutions of 2-D Poisson's equation and dissipative NEGF by modifying the on-site potential energy in the atomic-level description of the channel.

- Using the proposed model, a systematic investigation of the impact of interface traps on the I–V characteristics of MoS_2-FET is performed by considering various trap energy levels and positions along the channel.
- It is found that interface trap states with energy toward the mid-gap energy level from the conduction band significantly increase the OFF-state current due to phonon-assisted source-drain tunneling current with trap states, while the charge trapping in the interface states reduces the ON-state current.
- It is found that the interface trap states close to the mid-gap severely affect the key device performance metrics, such as OFF-state current (I_{OFF}), SS, and V_{TH}, for the sub-18 nm gate length.
- The simulation results suggest that minimizing the interface trap states with energy close to mid-gap energy level and trap position around the middle of the channel can considerably reduce the leakage current and improve the short-channel MoS_2-FET performance.

■ To develop a CMOS-compatible device architecture, this research presents the 3-D integration of single-layer (SL) and bilayer (BL) MoS_2 in stacked NS-FETs using fully calibrated TCAD simulation for the future technology node.

- The findings indicate that integrating atomically thin MoS_2 in stacked NS-FET presents a promising opportunity to achieve a high ON-state current and a substantial ON-OFF current ratio, while maintaining a near-ideal SS.
- Even at an aggressively scaled 0.5 nm technology node, the SL- and BL-MoS_2 NS-FETs demonstrate strong immunity against SCEs.
- The short channel behavior of MoS_2 NS-FET can be further enhanced by increasing the number of layers and selecting a smaller equivalent oxide thickness (EOT).

■ To determine the feasibility and performance of 2DMs for ICs, a comprehensive performance analysis of CMOS inverter configurations is performed which is based on

2DMs, such as BP, MoS_2 WSe_2, WS_2, WTe_2, WeS_2-MoS_2. Their performance is also benchmarked with that of Si-based counterparts for channel lengths below 10 nm.

- Among the range of 2DM-based inverters, the configuration utilizing heterogeneous WSe_2 and MoS_2 demonstrates exceptional switching characteristics for channel lengths of 5.6 nm and beyond. It exhibits a larger static noise margin, power dissipation in the nanowatt range, and comparable speed when compared to Si-based inverters.
- The findings indicate that the CMOS inverters based on higher electron and hole effective mass 2DMs can be more favorable to scaling down the channel length below 3 nm.
- The analysis of performance and benchmarking results indicate favorable prospects and potential in the utilization of 2DM-based devices for forthcoming logic applications. Nevertheless, the critical factors for enhancing the performance of CMOS inverter lie in the optimization of parasitic capacitances, contact resistance, and channel length as pivotal device design parameters.

Chapter 2

Quantum Transport Model For 2-D Material-based FETs

2.1 Introduction

Over the past four decades years, the study of electron transport in semiconductors has been given considerable attention, particularly due to the operational principles of semiconductor devices hinging on the precise control of electron and hole movements. Several approaches have been implemented to accurately describe the intricate transport mechanisms within semiconductor devices. In the classical framework, the transport properties in a semiconductor device are described through the drift-diffusion (DD) equation, which is derived from the first moment of the distribution function in Boltzmann Transport Equation (BTE) [45]. However, when the device dimension is reduced to less than 1 μm, the electric field in the device becomes significantly high, which leads to the hot-carrier effect, such as velocity overshoot [45]. This results in the loss of predictive capability of the DD equation. It becomes imperative to employ the hydrodynamic model at such dimensions, which is a higher moment of the BTE. In this model, the current expression is modified to exhibit a direct proportionality to the gradient of carrier temperature, which results in kinetic energy-dependent mobility rather than field-dependent mobility. [46], [47].

As the dimension of the device scales below 100 nm, the accuracy of moment-based solutions derived from the BTE begins to deteriorate [48], [49]. This phenomenon becomes notably ineffective as the strength of the electric field intensifies, potentially resulting in the emergence of abnormal velocity peaks attributed to the truncation of moments. Therefore, in such scenarios, employing microscopic transport models becomes necessary. In the context of semi-classical methodologies, these models may involve the application of particle-based Monte Carlo techniques or the direct solution of the full BTE [50], [51].

In the case of devices with dimensions even smaller, typically in the sub-20 nm range, where the dimensions approach the scale of a few atomic lengths, modeling approaches derived from BTE fail to provide viable solutions. This failure arises due to the emergence of several quantum mechanical phenomena in this regime, including quantum tunneling, carrier confinement, and quantum interference [47], [52]. The NEGF approach

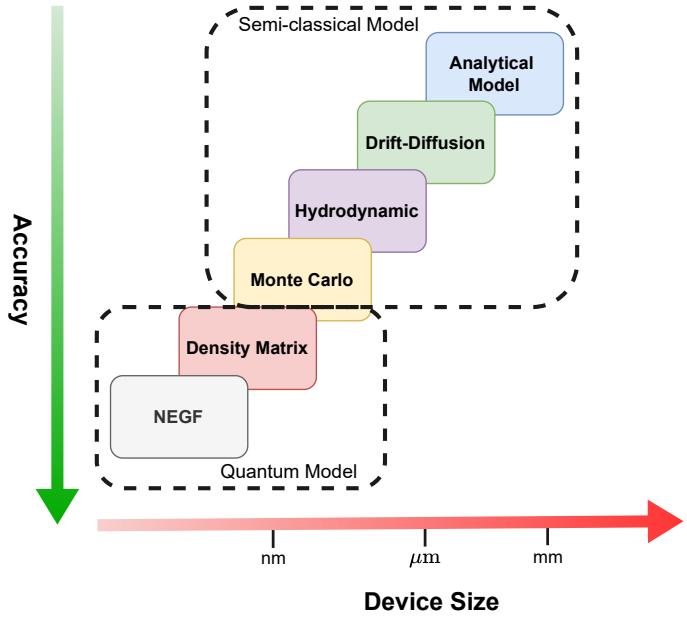

Figure 2.1: Hierarchy of carrier transport models incorporating dissipative interactions.

emerges as a promising theoretical framework for studying quantum-mechanical systems that operate significantly distant from equilibrium conditions [53]. NEGF has attracted significant attention in the last 20 years for providing a critical understanding of carrier transport mechanisms at these microscopic dimensions. The NEGF-based approach has demonstrated its effectiveness in modeling and offering deeper insights into the underlying physics of a wide range of nanoscale devices, encompassing Si nanowires [54] and FinFETs [55], III-V MOS-FETs [56], carbon nanotubes (CNT) [57], 2DM-based FETs [34], etc.

2.2 Overview of Quantum Transport Framework

As device dimensions continue to shrink, quantum mechanical simulations have become crucial for precise performance predictions of nanoscale devices. While a comprehensive quantum simulation can be established through the self-consistent resolution of Schrödinger and Poisson's equations, this approach is either computationally inefficient or applicable solely to simplified and very small structures with fewer atoms [52]. An expedient and straightforward approach to model quantum transport is solving the Schrödinger equation within the NEGF formalism [58]. This method offers a compelling trade-off between computational efficiency and the accurate incorporation of quantum effects [55]. The NEGF formalism also offers a solid conceptual foundation upon which additional physical phenomena, such as scattering, can be incorporated [48]. Even though ballistic transport is anticipated to have a pivotal role in nanoscale devices, it is well-established that numerous other factors, such as random impurities, remote coulomb

scattering, surface roughness, and phonon scattering, will exert a substantial influence on the electrical characteristics [52].

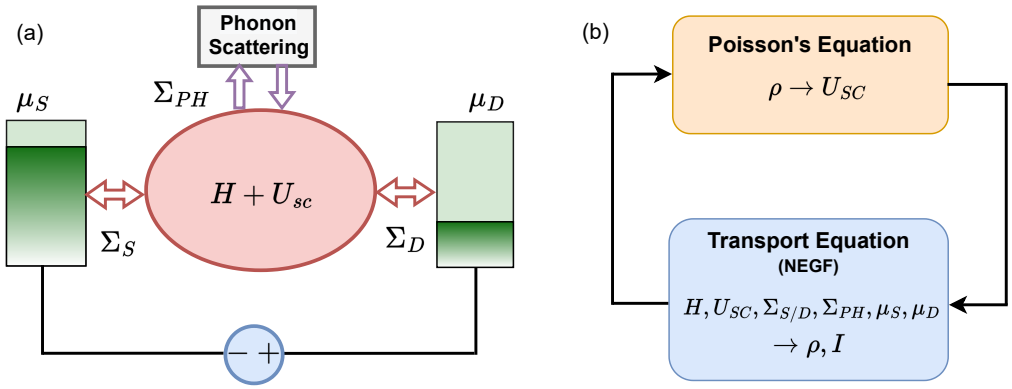

Figure 2.2: Schematic of the device system coupled to source and drain contact and a phonon scattering bath, and (b) self-consistent procedure in the dissipative NEGF model. Here, H represents the Hamiltonian of the device, U_{SC} stands for the self-consistent potential within the device, $\Sigma_{S/D}$ represents the self-energy matrix associated with the source and drain regions, I signifies the current, and $n(r)$ corresponds to electron density. Additionally, μ_S and μ_D represent the Fermi levels of the source and drain contacts, respectively.

Fig. 2.2(a) illustrates the schematic of the device using the dissipative NEGF model. The description of the central channel region is achieved through the Hamiltonian matrix (H). The on-site electrostatic potential energy, which is obtained by self-consistently solving Poisson's equation, is included with the Hamiltonian. The interaction of the source and drain regions with the channel is defined using self-energies ($\Sigma_{S/D}$). The incoherent scattering processes inside the device, such as electron-phonon and phonon-phonon scatterings, are modeled using self-energy matrices (Σ_{PH}). The self-energy associated with scattering is calculated using the SCBA.Further, the charge density is calculated within the device by solving the retarded Green's function and employing the Fermi-Dirac distribution. As Fig. 2.2(b) illustrates, the charge density and Poisson's equation are solved iteratively until a specific convergence criterion is met. Once the desired convergence criteria is met, the dissipative NEGF formalism within the SCBA scheme yields a precise and well-defined relationship that can be employed to determine the charge density and current. Based on the above discussion, the step-by-step procedure for treating the dissipative quantum transport in nanoscale device, as shown in Fig. 2.3, is elucidated as follows [47], [53].

(i) **Choice of Representation and Discretization Method** - In the first step, based on the type of device and its contacts, an appropriate choice is made for (a) the representation or basis in which the discretization of the operators is done, and (b)

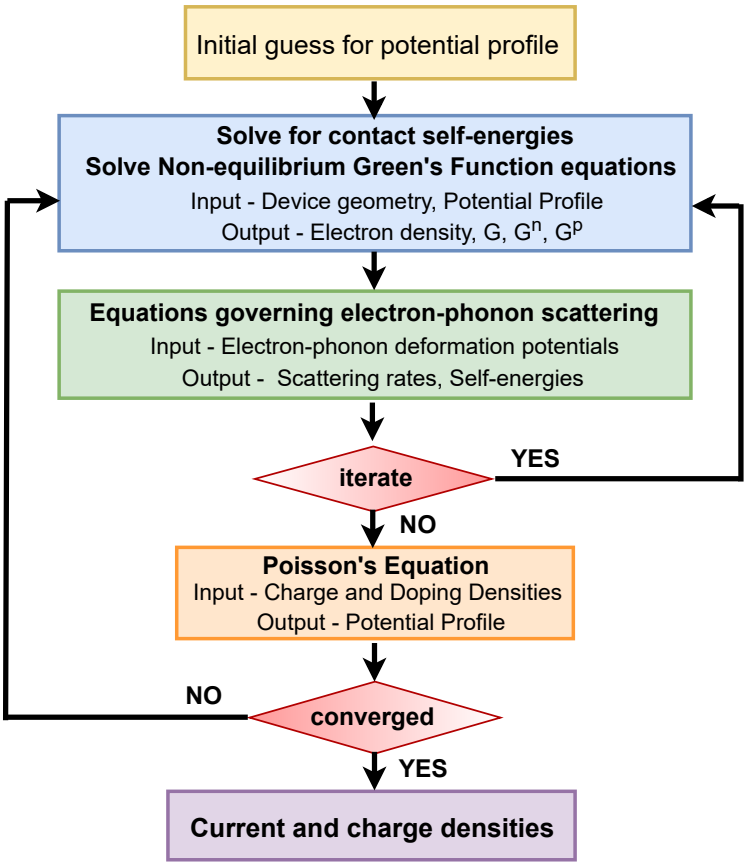

Figure 2.3: Flowchart depicting the integration of 2-D Poisson's equation and NEGF equation within the framework of the self-consistent Born approximation (SCBA) to obtain solutions for modeling dissipative quantum transport.

the method for the discretization of the operators. This study adopts the real-space basis for expressing the matrices, and the finite difference method is employed to discretize the respective operators.

(ii) **Modeling of Hamiltonian** - A critical step in accurately modeling electronic transport through the NEGF formalism is identifying and constructing a suitable tight-binding Hamiltonian matrix, which adequately describes the material properties. This Hamiltonian matrix plays a pivotal role, as it essentially characterizes the electronic band structure of the isolated device. Moreover, the computational cost of NEGF is influenced by the size of the Hamiltonian matrix. To obtain a precise description of the material, one can adopt first-principles DFT simulations and experimental studies for acquiring material parameters.

(iii) **Contact Definition** - After defining an accurate atomistic description, the subsequent phase involves the integration of the influence of source and drain contacts. The influence of drain and source contacts is incorporated by introducing

self-energy matrices into the Hamiltonian matrix, which describes the open boundary conditions essential for solving the Schrödinger equation. The self-energy matrices for the source (Σ_S) and drain (Σ_D) are calculated using the surface Green's function. The computation cost required for solving the surface Green's function is reduced using the Sancho-Rubio Algorithm [59].

(iv) **Initial Guess for Device Potential** - To initiate the self-consistent procedure, an initial approximation of the self-consistent potential across the device is required. This initial guess of the device potential can be obtained from the semi-classical carrier statistics.

(v) **Ballistic NEGF** - Having gathered all the information from the previous steps, the ballistic NEGF equation is solved to yield the Gr, which presents the response of the system to an impulse excitation within the device. The retarded Green's function is used to calculate the electron and hole correlation functions (G^n and G^p), and charge density ($n(r)$) within the device.

(vi) **Treatment of Phonon Scattering in NEGF** - The next step is to incorporate the electron-phonon scattering effect, which is achieved by including the scattering self-energy in the device Hamiltonian matrix. The calculation of electron-phonon scattering self-energy requires in and out scattering functions ($\Sigma_{in/out}$), which are calculated within the SCBA scheme using the ballistic G^n and G^p. In the SCBA scheme, the retarded Green's function ($Gr(E)$) and the scattering self-energy (Σ_{PH}) are determined self-consistently based on certain convergence criteria that ensure current continuity in the device. Similar to the ballistic case, this $Gr(E)$ is used to calculate the G^n and G^p, and $n(r)$ within the device.

(vii) **Self-consistent solution** - Using the charge density, the 2-D Poisson's equation is solved to obtain the self-consistent potential (U_{SC}) in the device. The 2-D Poisson equation provides an accurate description of the device electrostatics, as it considers the distribution of charge in both dimensions. This is in contrast to the 1-D transport assumption, which assumes charge to be constant along the width of the device.

(viii) **Calculation of Current** - Upon achieving convergence, the current passing through the device is computed using Gr in conjunction with $\Sigma_{in/out}$.

2.3 Dissipative Transport in 2-D Material-based Field-Effect Transistors

Introducing 2DMs in industrial process integration for technology development could be very expensive and time-consuming. Further, selecting 2DM with optimized geometry and interface is a challenging task from the family of more than 1800 exfoliable materials [22]. Therefore, there is a pressing need for a modeling framework that allows the estimation of integrated device performance based on the crystallographic properties of the constituent transistor materials. Such a framework would serve as a valuable tool to guide experimental endeavors and stimulate focused research efforts in the right direction. In order to conduct the assessment prior to the availability of the wafer, these models must adhere to first principles. Despite considerable dedication to synthesis and manufacturing, the community focused on 2DMs still needs a computationally efficient modeling framework, which can precisely forecast device performance based solely on material data.

One of the significant driving forces behind the interest in monolayer 2DMs is their potential to serve as a substitute for traditional Si as the channel material in ultra-scaled MOSFETs. Experimental measurements have shown that the electron mobility in 2DMs at room temperature is considerably lower than that of bulk Si. The decrease in mobility is primarily ascribed to electron-phonon scattering, which is an intrinsic mechanism that is challenging to mitigate at room temperature. Monolayer 2-D semiconductors generally exhibit higher electron-phonon scattering rates compared to their 3-D counterparts, mainly due to the denser electronic and phononic states near the band extrema [60]. Furthermore, both experimental observations and theoretical calculations, such as those based on density functional theory and the BTE, have confirmed the limitations imposed by electron-phonon scattering on the mobility of monolayer 2DMs. Given these factors, it becomes imperative to incorporate electron-phonon interactions into the modeling framework of 2DM-based devices. A careful understanding of the impact of electron-phonon scattering is essential for optimizing the performance of monolayer 2DM-based devices and advancing their practical applications in the field of nanoelectronics. Therefore, it becomes important to develop a proper diffusive quantum-transport model for the 2DM-FET that can accurately incorporate the effect of electron-phonon interaction. [61].

MoS_2 is selected as the representative material for providing the description of the NEGF modeling approach. However, the approach in this work can be easily extended to model a broad range of devices by adjusting the material attributes as needed.

2.3.1 Modeling of Hamiltonian

To comprehend electron transport in nanoscale devices, the time-independent Schrödinger equation governing the behavior of an electron within the device system can be solved. The Schrödinger equation can be given as

$$\frac{\hbar^2}{2m}\nabla^2\psi + V\psi = E\psi \tag{2.1}$$

Where, ψ denotes the wave-function of the electron in the device, V represents the potential energy, and E corresponds to the total energy possessed by the electron.

The matrix form of this equation represents the eigen value problem for the closed system.

$$H\psi = E\psi \tag{2.2}$$

where H signifies the Hamiltonian matrix associated with the device. The eigen values of H correspond to the allowed energy levels within the channel, which describe the electronic band structure of the isolated device.

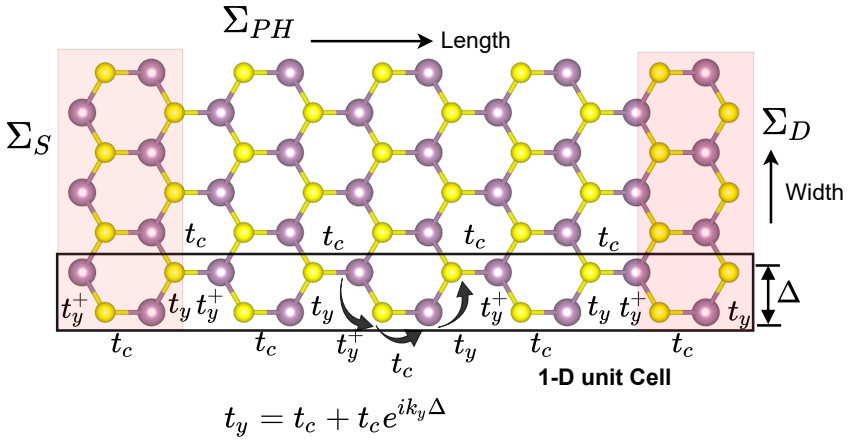

Figure 2.4: Schematic of the device depicting the atomic structure of 2H-MoS_2 sheet with 1-D unit cell and corresponding binding energy, and contact ($\Sigma_{S/D}$) and scattering self-energies (Σ_{PH}).

To reduce the computational burden, a tight-binding Hamiltonian is constructed by identifying a 1-D elementary cell along the width [62], as shown in Fig. 2.4. In the

nearest-neighbor approximation, the Hamiltonian for 1-D elementary cell can be given as

$$H\left(k_y\right)=\begin{bmatrix} \alpha & \beta_1 & & & & \\ \beta_1^{\dagger} & \alpha & \beta_2 & & & \\ & \beta_2^{\dagger} & \alpha & \beta_1 & & \\ & & \beta_1^{\dagger} & \alpha & \beta_2 & \\ & & & \beta_2^{\dagger} & \cdots & \cdots \\ & & & & \cdots & \cdots \end{bmatrix}_{N_x\times N_x} \tag{2.3}$$

Where, α represents the on-site coupling matrix, and β_1, and β_2 denote the coupling matrices responsible for interactions between adjacent atoms. N_x corresponds to the total number of atoms contained within the unit cell of the device. The coupling matrices are calculated as

$$\alpha=\begin{bmatrix} E_{cm} & t_c \\ t_c & E_{vm} \end{bmatrix},\quad \beta_1=\begin{bmatrix} 0 & 0 \\ t_y^{\dagger} & 0 \end{bmatrix},\quad \beta_2=\begin{bmatrix} 0 & 0 \\ t_y & 0 \end{bmatrix}$$

Where, E_{vm} is represented as the top of the valence band, and E_{cm} is represented as the bottom of conduction band. The t_c represents the nearest-neighbor electron hopping between atoms situated within the same plane, while t_y characterizes the nearest-neighbor electron hopping between atoms in distinct planes. t_y is calculated as

$$t_y=t_c+t_c e^{ik_y\Delta}$$

Where, t_c can be calculated as

$$t_c=\frac{2\hbar^2 E_G}{3a_c^2 m_x^*}$$

Where, Δ is the lattice parameter. When dealing with a large-area 2DM, it becomes possible to apply Bloch periodic boundary conditions along the width. Consequently, the quantization of transverse wave vector (k_y) is achieved by enforcing Bloch periodic boundary conditions with a period denoted by Δ as

$$k_y=\frac{2\pi v}{\Delta},\quad \text{and}\quad v=\pm1,\pm2,\pm3...\pm n. \tag{2.4}$$

Where, $\Delta=\frac{\sqrt{3}}{2}a_c$, which is calculated by assuming armchair orientation of 2DM along transport direction.

A Substantial computational cost savings can be realized by restricting the definition of k_y to a limited region within the Brillouin zone. It has been observed that k_y values near the high-symmetry point, where the bandgap is defined, are adequate for accurately reproducing the band structure of 2DMs in the vicinity of the conduction band minima

and valence band maxima. By employing this approach, the full real-space lattice of 2DMs is effectively transformed into several distinct 1-D real-space lattices.

2.3.2 Contact Modeling

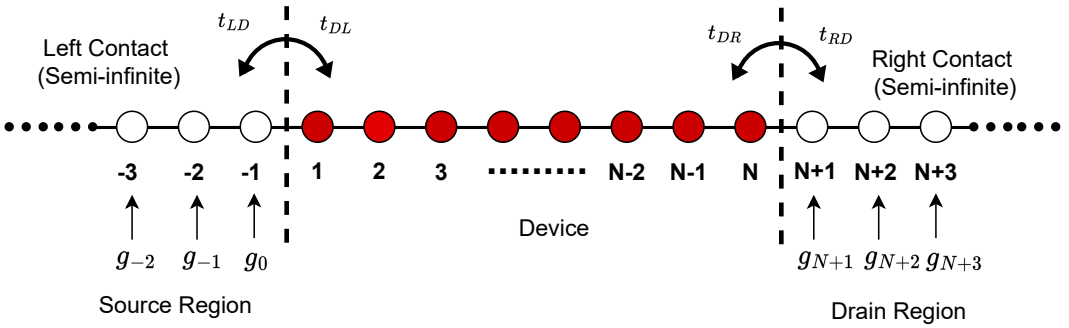

Figure 2.5: Dividing the simulation domain into three parts: the device region, as well as the left and right contact region.

The closed device system establishes connections with the external world through contacts, which facilitates the inflow and outflow of electrons. To achieve this, the self-energy matrices of the source and drain contacts (Σ_S and Σ_D) are added to the device Hamiltonian. Σ_S and Σ_D are calculated by using surface Green's function.

Fig. 2.5 illustrates the 1-D elementary cell of the entire device, segmented into three distinct regions: the left contact region (comprising unit cells 0, -1, -2, ...), the device region (comprising unit cells 1, 2, ..., N-1, N), and the right contact region (comprising unit cells N+1, N+2, ...). The matrix A is defined as $A = EI - H$ and $G = A^{-1}$, where G is the retarded Green's function of the system, and I is the identity matrix.

Now, by the definition of A,

$$AG = I \tag{2.5}$$

The matrices A and G can also be divided into corresponding block matrices based on the region of the entire device. Eq. 2.5 can, therefore, be expressed as

$$\begin{bmatrix} A_{LL} & A_{LD} & O \\ A_{DL} & A_{DD} & A_{DR} \\ O & A_{RD} & A_{RR} \end{bmatrix} \begin{bmatrix} G_{LL} & G_{LD} & G_{LR} \\ G_{DL} & G_{DD} & G_{DR} \\ G_{RL} & G_{RD} & G_{RR} \end{bmatrix} = \begin{bmatrix} I & O & O \\ O & I & O \\ O & O & I \end{bmatrix}. \tag{2.6}$$

Where, O represents the zero matrix.

The matrices A_{RR}, A_{LL}, and A_{DD} are associated with the right semi-infinite contact, left semi-infinite contact, and the device region, respectively. $A_{LD} = A_{DL}^{+}$ and $A_{DR} = A_{RD}^{+}$ correspond to the coupling between left contact and the device region and right contact

and the device region, respectively, and are given by,

$$A_{LD} = \begin{bmatrix} 0 & \dots & 0 \\ \vdots & \ddots & \vdots \\ -t_{LD} & \dots & 0 \end{bmatrix}, \quad A_{RD} = \begin{bmatrix} 0 & \dots & -t_{RD} \\ \vdots & \ddots & \vdots \\ 0 & \dots & 0 \end{bmatrix} \tag{2.7}$$

From the Eq. 2.6,

$$A_{LL}G_{LD} + A_{LD}G_{DD} = 0 \tag{2.8}$$

$$A_{DL}G_{LD} + A_{DD}G_{DD} + A_{DR}G_{RD} = I \tag{2.9}$$

$$A_{RD}G_{DD} + A_{RR}G_{RD} = 0 \tag{2.10}$$

The Eq. 2.8-2.10 can be rearranged as

$$G_{LD} = -A_{LL}^{-1}A_{LD}G_{DD} \tag{2.11}$$

$$G_{RD} = -A_{RR}^{-1}A_{RD}G_{DD} \tag{2.12}$$

On putting Eq. 2.11 and Eq. 2.12 in Eq. 2.9 and rearranging the terms gives

$$[A_{DD} + A_{DL}A_{LL}^{-1}A_{LD} + A_{DR}A_{RR}^{-1}A_{RD}] = I \tag{2.13}$$

Using Eq. 2.13, the infinite Green's function can be converted to a finite device Green's function (G_{DD}) by defining $\Sigma_S = A_{DL}A_{LL}^{-1}A_{LD}$ and $\Sigma_D = A_{DR}A_{RR}^{-1}A_{RD}$ as coupling to the right and left contacts. The Σ_S and Σ_D matrices are called the self-energy matrices.

The Green's function for the source (left) and drain (right) contact is defined as

$$g^L = A_{LL}^{-1} \tag{2.14}$$

$$g^R = A_{RR}^{-1} \tag{2.15}$$

The atoms located on the initial and final atomic sites in the device (1 and N site in Fig 2.5) are connected to the contacts. Consequently, the non-zero blocks in the $\Sigma_{S/D}$ correspond to the first and the last 2×2 entries, which can be computed as

$$\Sigma_S = \beta_2^+ g_0^L \beta_2 \tag{2.16}$$

$$\Sigma_D = \beta_2^+ g_{N+1}^R \beta_2 \tag{2.17}$$

Where, g_0^L and g_{N+1}^R signifies the surface Green's function of the source contact (left contact), and drain contacts (right contact).

To reduce the computational burden associated with calculating the surface Green's function, an efficient and faster iterative Sacho-Rubio algorithm is employed. By

performing the block matrix multiplication of A_{LL} and the final column of g^L, Eq. 2.14 can be rewritten as

$$\begin{bmatrix} \bullet & \bullet & & & & & \\ \bullet & \bullet & \bullet & & & & \\ & \bullet & \bullet & \bullet & & & \\ & & A_{-2,-3} & A_{-2,-2} & A_{-2,1} & & \\ & & & A_{-1,-2} & A_{-1,-1} & A_{-1,0} & \\ & & & & A_{0,-1} & A_{0,0} \end{bmatrix} \begin{bmatrix} \bullet \\ \bullet \\ \bullet \\ g_{-2,0} \\ g^L_{-1,0} \\ g^L_{0,0} \end{bmatrix} = \begin{bmatrix} \bullet \\ \bullet \\ \bullet \\ 0 \\ 0 \\ I \end{bmatrix} \tag{2.18}$$

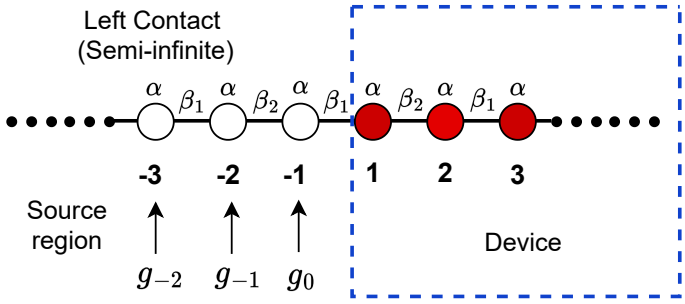

Figure 2.6: Schematic of quasi 1-D elementary cell with left contact and device region.

For the case of 2DM with Hamiltonian as defined by Eq. 2.3, the Eq. 2.19 gets modifies as

$$\begin{bmatrix} \bullet & \bullet & & & & & \\ \bullet & \bullet & \bullet & & & & \\ & \bullet & \bullet & \bullet & & & \\ & & \beta_1^+ & EI-\alpha & \beta_2 & & \\ & & & \beta_2^+ & EI-\alpha & \beta_1 & \\ & & & & \beta_1^+ & EI-\alpha \end{bmatrix} \begin{bmatrix} \bullet \\ \bullet \\ \bullet \\ g_{-2,0} \\ g^L_{-1,0} \\ g^L_{0,0} \end{bmatrix} = \begin{bmatrix} \bullet \\ \bullet \\ \bullet \\ 0 \\ 0 \\ I \end{bmatrix} \tag{2.19}$$

$$(EI-\alpha)g^L_{0,0} = I - \beta_1^+ g^L_{-1,0} \tag{2.20}$$

$$(EI-\alpha)g^L_{-1,0} = -\beta_2^+ g^L_{-2,0} - \beta_1 g^L_{0,0} \tag{2.21}$$

$$(EI-\alpha)g^L_{-2,0} = -\beta_1^+ g^L_{-3,0} - \beta_2 g^L_{-1,0} \tag{2.22}$$

On taking $u_1 = -(EI-\alpha)^{-1}\beta_1$, $u_2 = -(EI-\alpha)^{-1}\beta_2$, $v_1 = -(EI-\alpha)^{-1}\beta_1^+$, and

$v_2 = -(EI - \alpha)^{-1}\beta_2^+$, and substituting Green's function, Eq. 2.22 becomes

$$g^L_{-2,0} = vg^L_{-4,0} + ug^L_{0,0} \tag{2.23}$$

$$g^L_{-4,0} = vg^L_{-6,0} + ug^L_{-2,0} \tag{2.24}$$

$$g^L_{-6,0} = vg^L_{-8,0} + ug^L_{-4,0} \tag{2.25}$$

Where, $v = (I - u_1v_1 - u_2v_2)^{-1}v_1v_2$, and $u = (I - u_1v_1 - u_2v_2)^{-1}u_1u_2$. The Eq. 2.25 can be generalized as

$$g^L_{-2n,0} = vg^L_{-2n-2,0} + ug^L_{-2n+2,0} \tag{2.26}$$

The process of substitution of surface Green's function can be continued until the magnitude from the higher order surface Green's function terms becomes zero.

$$g^L_{-1,0} = (u_1 + v_2u + v_2u^2v...)g^L_{-0,0} + (v_2v + v_2uv^2)^{-1}g^L_{-4,0} + v_2v^2g^L_{-6,0} \tag{2.27}$$

Where, $\theta = u_1 + v_2u + v_2u^2v...$, and $\eta = v_2v^2$. The substitution process is continued until $\eta < \delta$, where δ is an arbitrarily small value of the convergence criteria. Equation 2.27 can then be expressed as

$$g^L_{-1,0} = \theta g^L_{0,0} \tag{2.28}$$

Therefore, on substituting the Eq. 2.28 in Eq. 2.22, an approximation for the surface Green's function is given by

$$g^L_{0,0} = (EI - \alpha - \beta_2^+\theta)^{-1} \tag{2.29}$$

A comparable approach can be employed to derive the surface Green's function for the drain (right) contact.

2.3.3 Ballistic NEGF Framework

After constructing a suitable Hamiltonian and defining the self-energies, the retarded Green's function of the system, under the conditions of ballistic transport, can be computed as,

$$Gr(E, k_y) = [EI - H(k_y) - \Sigma_S - \Sigma_D]^{-1} \tag{2.30}$$

Where I represents the identity matrix, k_y represents the transverse momentum wave vector, and E corresponds to the energy. The electron-electron interaction is incorporated into H by a self-consistent potential (U_{SC}), which is obtained from the solutions of the coupled Poisson's equation. The inversion of full Green's function can be a computationally demanding step. Thus, a significant reduction in computational cost can be attained by employing the Gauss elimination (GE) method to solve a limited number of columns in

the retarded Green's function. The source (S) and drain (D) contacts, described by Σ_S and Σ_D, are considered to be in an equilibrium state and are defined by their respective Fermi energy levels μ_S and μ_D.

The discrete energy levels of the isolated device undergo broadening when it is connected to the external S and D contacts. This broadening function due to S and D contacts is given by

$$\Gamma_{S/D}(E) = -i(\Sigma_{S/D}(E) + \Sigma^{+}_{S/D}(E)) \tag{2.31}$$

The electron and hole correlation functions G^n and G^p are given by

$$G^n = Gr\Sigma^{in}Gr \tag{2.32}$$

$$G^p = Gr\Sigma^{out}Gr \tag{2.33}$$

where, Σ^{in} and Σ^{out} are the total in and out scattering functions. For the case of ballistic transport, these are calculated as

$$\Sigma^{in}(E) = \Sigma^{in}_S(E) + \Sigma^{in}_D(E) \tag{2.34}$$

$$\Sigma^{out}(E) = \Sigma^{out}_S(E) + \Sigma^{out}_D(E) \tag{2.35}$$

where, $\Sigma^{in}_{S/D}$ and $\Sigma^{out}_{S/D}$ are the in and out-scattering functions for S/D contact, and are given by

$$\Sigma^{in}_{S/D}(E) = \Gamma_{S/D}(E) f_{S/D}(E) \tag{2.36}$$

$$\Sigma^{out}_{S/D}(E) = \Gamma_{S/D}(E)(1 - f_{S/D}(E)) \tag{2.37}$$

where, $f_{S/D}$(E) is the S/D Fermi-Dirac distribution function expressed as $f_{S/D}(E) = 1/(1+\exp((E-\mu_{S/D})/k_BT))$. The charge density from the retarded Green's function can be computed as

$$\begin{aligned} n(x) = (-q)\int_{-\infty}^{+\infty} dE \times \sum_{k_y} [A_S(E,x,k_y) \times f_S(E) + \\ A_D(E,x,k_y) \times f_D(E)] \end{aligned} \tag{2.38}$$

where q represents the electron charge, T represents the absolute temperature, k_B represents the Boltzmann constant, and $\mu_{S/D}$ is the S/D Fermi levels. The quantities A_S and A_D represent the local density of states (LDOS) originating from the source (S) and drain (D) contacts, respectively, and these can be determined as follows

$$\begin{aligned} A_S &= G^r(E,k_y)\,\Gamma_S G^r(E,k_y)^+ \\ A_D &= G^r(E,k_y)\,\Gamma_D G^r(E,k_y)^+ \end{aligned} \tag{2.39}$$

This charge density ($n(x)$) is used to self-consistently solve the 2-D Poisson's equation for a desired convergence criteria. Once the convergence is met, the source-to-drain current density is computed by the Landauer formula.

$$I_{DS} = \frac{2q}{hW} \times \int_{BZ} dk_y \int dE T(E, k_y)[f_S(E) - f_D(E)] \tag{2.40}$$

where h represents the Planck's constant, W represents the width of the device, and $T(E, k_y)$ is the transmission coefficient that can be computed as $T(E, k_y) = \Gamma_S(E, k_y)A_D(E, k_y)$.

2.3.4 Modeling of Electron-Phonon Scattering

In the previous section, NEGF formalism for modeling the ballistic transport in a device is discussed. However, practical devices typically operate under conditions where scattering processes significantly influence their transport properties. The NEGF formalism for the ballistic transport case can be extended to incorporate the influence of phonon scattering effects. This modification involves adjusting scattering probes using the self-energy matrices, which was originally used to represent the coupling between the active device region and S/D contacts for modeling the perturbing factor acting upon the device Hamiltonian.

The retarded Green's function of the device under the influence of electron-phonon scattering is given as

$$Gr(E, k_y) = [EI - H(k_y) - \Sigma_S - \Sigma_D - \Sigma_{PH}]^{-1} \tag{2.41}$$

The self-energy (Σ_{PH}) for electron-phonon scattering is calculated through Hilbert transformation as

$$\Sigma_{PH}(E) = \frac{1}{2\pi} \int \frac{\Gamma_{PH}(E')}{E' - E} dE' - i\frac{\Gamma_{PH}(E)}{2} \tag{2.42}$$

Where Γ_{PH}, representing the level broadening due to scattering, is given as

$$\Gamma_{PH}(E) = \Sigma_{PH}^{in}(E) + \Sigma_{PH}^{out}(E) \tag{2.43}$$

The calculation of Σ_{PH} is simplified by neglecting the real component of Σ_{PH}, as its influence is considered to be negligible [57]. Therefore, the simplified Σ_{PH} is presented by

$$\Sigma_{PH}(E) = -i\frac{\Gamma_{PH}(E)}{2} = \frac{-i}{2}(\Sigma_{PH}^{in}(E) + \Sigma_{PH}^{in}(E)) \tag{2.44}$$

The in-scattering function, Σ_{PH}^{in}, and out-scattering function, Σ_{PH}^{out}, associated with electron-phonon scattering include contributions from both elastic and inelastic phonon

scattering processes. The calculation of these in-scattering and out-scattering functions is performed using the SCBA method. The SCBA method is used within the field of quantum mechanics to account for the effects of scattering present in quantum systems.

In case of elastic scattering, the energy associated with the phonon can be safely neglected. The acoustic phonon mode is contributed to the elastic scattering mechanism. Therefore, the in and out scattering functions for elastic phonon scattering (Σ_{el}^{in} & Σ_{el}^{out}) are calculated as

$$\Sigma_{el}^{in}(i,i,E) = D_{ac}G^{n}(i,i,E) \tag{2.45}$$

$$\Sigma_{el}^{out}(i,i,E) = D_{ac}G^{p}(i,i,E) \tag{2.46}$$

The in- and out-scattering functions (Σ_{op}^{in} and Σ_{op}^{in}) for inelastic scattering are calculated as

$$\Sigma_{inel}^{in}(i,i,E) = D_{op}[(n_\omega+1)G^{n}(i,i,E+\hbar\omega) + n_\omega G^{n}(i,i,E-\hbar\omega)] \tag{2.47}$$

$$\Sigma_{inel}^{out}(i,i,E) = D_{op}[(n_\omega+1)G^{p}(i,i,E-\hbar\omega) + n_\omega G^{p}(i,i,E+\hbar\omega)] \tag{2.48}$$

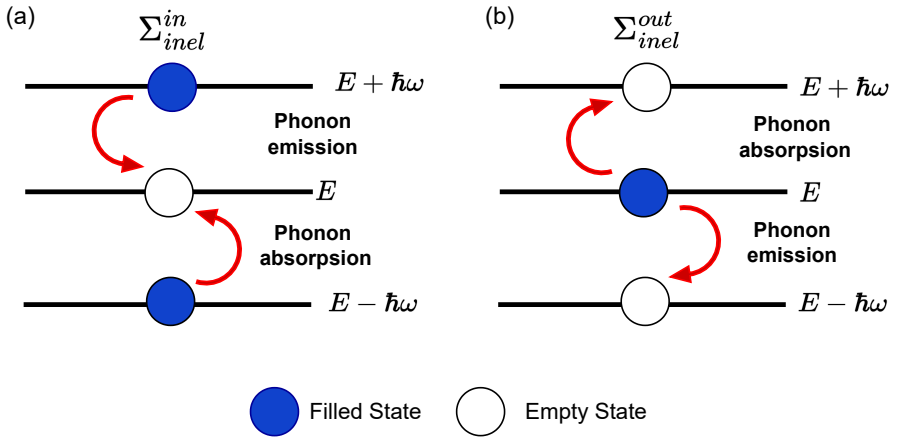

Figure 2.7: Inelastic scattering mechanism: Pictorial illustration of (a) electrons scattering into an unoccupied state at energy E, and (b) electrons scattering out of an occupied state at energy E, as a result of interaction with a single phonon carrying energy $\hbar\omega$.

where, n_ω denotes the phonon occupation factor, which is determined by Bose-Einstein statistics, ω is the frequency of the optical phonon. Σ_{inel}^{in} have two contributions based on phonon absorption and phonon emission mechanism. The optical phonon scattering is contributed inelastic scattering mechanism. It can be inferred from Fig. 2.7(a) that an electron can scatter to an unoccupied state at energy E by phonon emission from the occupied state at energy $E+\hbar\omega$ or phonon absorption from the occupied state at energy $E-\hbar\omega$. Similarly, for the Σ_{inel}^{out}, an electron can scatter out from a occupied

state at energy E by phonon absorption to an unoccupied state at energy $E+\hbar\omega$ or phonon emission to an unoccupied state at energy $E-\hbar\omega$, as illustrated in Fig. 2.7(b). D_{ac} and D_{op} are the electron-phonon coupling strength for acoustic and optical phonon scattering, respectively, which are given by the following expression [61]:

$$D_{ac} = \frac{K_{ac}^2 K_B T}{\rho_{2D} v_s^2} \tag{2.49}$$

$$D_{op} = \frac{\hbar K_{op}^2}{2\rho_{2D}\omega_0} \tag{2.50}$$

where K_{ac} and K_{op} correspond to the deformation potential for acoustic and optical phonons, respectively, ρ_{2D} is the 2-D mass density of the 2DM, and v_s stands for the sound velocity in the material. The K_{ac} and K_{op} can be obtained from the first principle DFT simulation and the previously reported experimental studies.

The expressions for the electron (G^n) and hole (G^p) correlation functions are given as

$$G^n = Gr\Sigma^{in}Gr \tag{2.51}$$

$$G^p = Gr\Sigma^{out}Gr \tag{2.52}$$

where Σ^{in} and Σ^{out} are the total in scattering and out scattering functions, which are defined as

$$\Sigma^{in}(E) = \Sigma^{in}_{PH}(E) + \Sigma^{in}_{S}(E) + \Sigma^{in}_{D}(E) \tag{2.53}$$

$$\Sigma^{out}(E) = \Sigma^{out}_{PH}(E) + \Sigma^{out}_{S}(E) + \Sigma^{out}_{D}(E) \tag{2.54}$$

The calculation of current flowing from position x_j to x_{j+1} along the x (transport) direction is carried out as

$$I_{j\to j+1} = \sum_{k_y} \frac{iq}{\hbar} \int_{-\infty}^{+\infty} \frac{dE}{2\pi} \left[H_{j,j+1}(k_y) G^n_{j+1,j}(E,k_y) \; - H_{j+1,j}(k_y) G^n_{j,j+1}(E,k_y) \right] \tag{2.55}$$

where, j denotes the grid point along the transport direction. The Eq. Since the local interaction assumption between electron (hole) and phonon is assumed, only diagonal elements of the Σ_{PH} are non-zero. The Eq. 2.41-2.52 are solved iteratively for certain convergence criteria which ensure the current continuity across the device. In a self-consistently converged SCBA loop, the current is calculated using Eq. 2.55 between two adjacent grid points along the channel, which should remain constant.

The calculation of the charge density within the device is performed by self-consistently solving the retarded Green's function in conjunction with the 2-D

Poisson's equation, aiming for the specified convergence criteria. The electron and hole density at a particular site along the channel can be calculated as

$$n_i = \sum_{k_y} \frac{1}{a_x a_z} \int_{-\infty}^{+\infty} \frac{G^n(i,i,k_y,E)}{2\pi} dE, \quad p_i = \sum_{k_y} \frac{1}{a_x a_z} \int_{-\infty}^{+\infty} \frac{G^p(i,i,k_y,E)}{2\pi} dE \tag{2.56}$$

The current through the device is calculated as,

$$I_{DS} = \frac{2q}{h} \int_{BZ} dk_y \int dE[trace\left(\Sigma_s^{in} G^p - \Sigma_s^{out} G^n\right)] \tag{2.57}$$

where h is Planck's constant, and E is the energy of the charge carrier.

2.4 2-D Electrostatics

For an accurate description of the potential within the device, an appropriate modeling of electrostatics is necessary, as it governs the current characteristics of the device. The electrostatics in the device are determined by solving the 2-D Poisson's equation, which relates the electrostatic potential $U_{SC}(x,z)$ and the charge density ($\rho(x)$) within the device. Since 1-D transport is considered in the modeling framework, the 2-D Poisson's equation is adequate to define the electrostatics of the device, as the potential along the width remains constant. The 2-D Poisson's equation for the device geometry can be expressed as

$$\nabla.(\varepsilon \nabla U_{SC}(x,z)) = q\rho(x) \tag{2.58}$$

Where q denotes the electronic, ϵ represents the electrical permittivity, and $\rho(x)$ signifies the charge density in the device, which is calculated as $\rho(x) = p - n + N_D^+ - N_A^-$. Here, p (n) represents the electron (hole) concentration, and N_D^+ (N_A^-) stands for the ionized acceptor (donor) concentration. The Poisson's equation, as described in Equation 2.58, is discretized using the finite-difference method. Dirichlet boundary conditions are applied at the gate voltage, while Neumann boundary conditions are imposed at the remaining nodes. To enhance the convergence of the self-consistent Poisson-NEGF loop, a non-linear inner loop is introduced within the framework of the 2-D Poisson's equation. This non-linearity is introduced due to the semiclassical carrier statistics, which converts the charge density into quasi-Fermi level through a dummy function. The non-linear inner loop acts as a damping mechanism for updating the potential energy, effectively preventing larger fluctuations between consecutive iterations. As a result, the coupled equations converge effectively and stably. To solve the non-linear Poisson's equation, the Newton-Raphson method is employed.

2.5 Validation of the Quantum Transport Modeling Framework

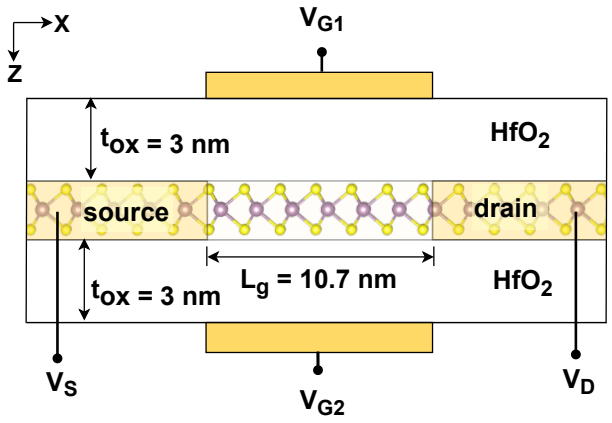

Figure 2.8: Schematic of the simulated double gate single layer MoS_2 field-effect transistor (FET). The geometrical parameters and device dimensions adopted from [63].

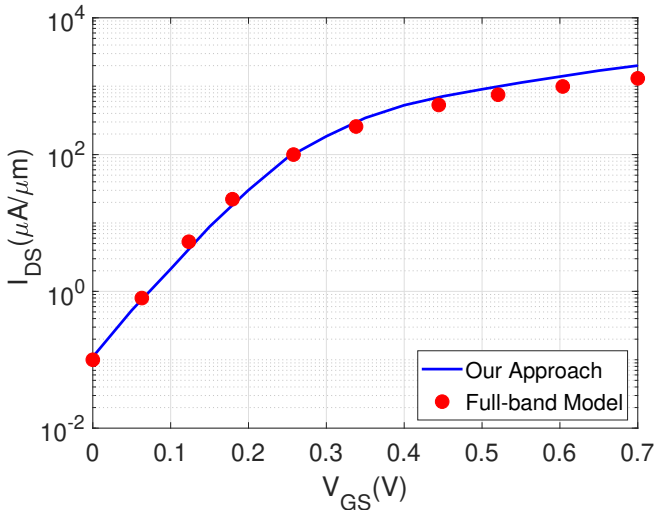

Figure 2.9: Transfer characteristics (I_{DS}–V_{GS}) of MoS_2-FET by the developed model in this work and full-band quantum transport model by Szabo et al. [63].

The accuracy of the tight-binding Hamiltonian model can be verified by calibrating results with a more sophisticated first-principle tool based on DFT simulation [63], [64]. Fig. 2.9 shows that the I-V characteristics of MoS_2-FET using 1-D real-space NEGF simulation are in good agreement with a more sophisticated first-principle tool based on DFT simulation [63]. However, verification with experiments is only qualitative as experimental techniques for 2DM-FETs are not sufficiently mature and are not allowed to produce reliable MOSFET-like devices. Most of the fabricated 2DM-FETs are either based on Schottky contacts or long-channel devices [16, 65, 66]. Further, the experimental devices suffer from larger defects in the crystal, higher interface trap density, larger contact

resistance, and scattering from substrate and impurities interactions.

To verify the accuracy of the modeling approach in incorporating the inelastic scattering, Fig. 2.10(a) and (b) show the conduction band profile and the energy-position-resolved current spectrum for ballistic and dissipative transport, respectively, for $V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V. It is observed that phonon scattering causes thermal relaxation of the electrons by phonon emission, as they move across the conduction band potential barrier. This results in the broadening of the current spectra compared to the ballistic case. Therefore, it can be inferred that the developed dissipative transport model accurately captures the electron-phonon scattering. Nevertheless, utilizing a quantum transport model that encompasses the entire band structure allows for a more comprehensive investigation of materials where the impact of higher energy bands and non-parabolicity on semiconductor device behavior is significant. However, it introduces additional complexity and a computationally intensive requirement when modeling quantum transport in MOSFETs.

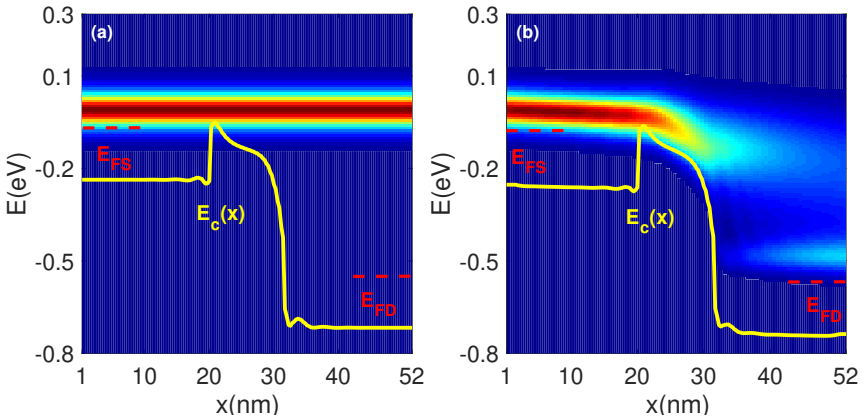

Figure 2.10: Conduction band profile (E_c) and energy-position-resolved current spectrum for (a) ballistic and (b) dissipative transport for $V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V.

2.6 Summary

A dissipative quantum transport modeling framework for the 2DM-FET has been developed. This framework relies on the self-consistent solutions of the 2-D Poisson's equation and dissipative NEGF formalism, utilizing a tight-binding Hamiltonian based on nearest-neighbor interactions. To reduce the computational cost associated with a full real-space description, a large-area 2DM sheet is modeled by identifying the 1-D elementary cell along the transverse direction. The electrostatics in the device is described using the 2-D Poisson's equation, which is discretized using the finite-difference method. The developed modeling approach has shown an excellent agreement when compared to

a more sophisticated full-band quantum transport tool, which demonstrates the accuracy of the developed framework in describing the dissipative quantum transport phenomena in 2DM-FETs. As 2DM-based devices are still in their initial phases of development, the developed modeling framework could be a promising tool for early performance evaluation across different technology choices and device configurations.

Chapter 3

Performance Analysis of Novel 2-D Materials

3.1 Introduction

The pursuit of high-speed and low power consumption in electronic systems has emerged as the primary driving force behind the search for alternative materials in post-silicon electronics. This need has grown even more pressing at sub-3 nm nodes as Si-based multigate MOSFET suffers from increased surface roughness and quantum effects [25], [27]. The discovery of graphene in 2004 ignited the exploration of 2DMs to replace silicon. However, the absence of a bandgap in graphene limits its suitability as a channel material for digital logic applications [14]. Nonetheless, it acted as a catalyst, prompting the investigation of other 2DMs, particularly transition metal dichalcogenides (TMDs) like WS_2, WSe_2, and $MoSe_2$, which have shown promise with single or few-layer channel configurations [14]. Especially, molybdenum disulfide (MoS_2) has been emerged as a prominent contender for ultra-scaled CMOS devices for post-silicon electronics due to their carrier mobility comparable to silicon, easy and large-scale fabrication with CMOS compatible processing techniques, and three-dimensional integration feasibility [12]. Interestingly, recent experimental studies on MoS_2-FET have demonstrated excellent switching performance with an ON-OFF current ratio of around 10^6, and SS of around 65 mV/dec for gate length down to 1 nm [16], [19].

In recent years, intensive research efforts have unveiled numerous new exfoliable 2DMs, expanding beyond graphene and TMDs [22]. These materials exhibit a range of properties, including metallic, semiconducting, and insulating characteristics, and encompass various categories, such as X-enes, X-anes, novel TMDs, MX-enes, Group-IV Monochalcogenides, Janus 2DMs, etc [22], [67]. With an extensive pool of more than 1800 exfoliable materials, selecting 2DM with optimized geometry and interface is challenging. Thus, a modeling framework that enables material-to-circuit level performance estimation from the crystallographic information of constituent transistor materials is in great demand to guide the experiments and trigger more efforts in the right direction.

This chapter employs a multi-scale modeling methodology to elucidate the performance constraints and advantages presented by these novel 2DMs in digital

applications. The logic performance of selected 40 2DMs in PFET and NFET configuration is assessed by implementing three key digital circuits, including, the CMOS inverter, 6-Transistor Static Random-Access Memory (6T SRAM), and 32-bit Arithmetic Logic Unit (ALU). The objective is to narrow down the design space for 2DMs and identify the five most promising options, including GeTe, PbS, Sn_2S_2, $Ti_2N_2Cl_2$, and $Ti_2Br_2N_2$, which could potentially surpass the excellent switching performance projected by IRDS 2021 [13].

3.2 2-D Material Family

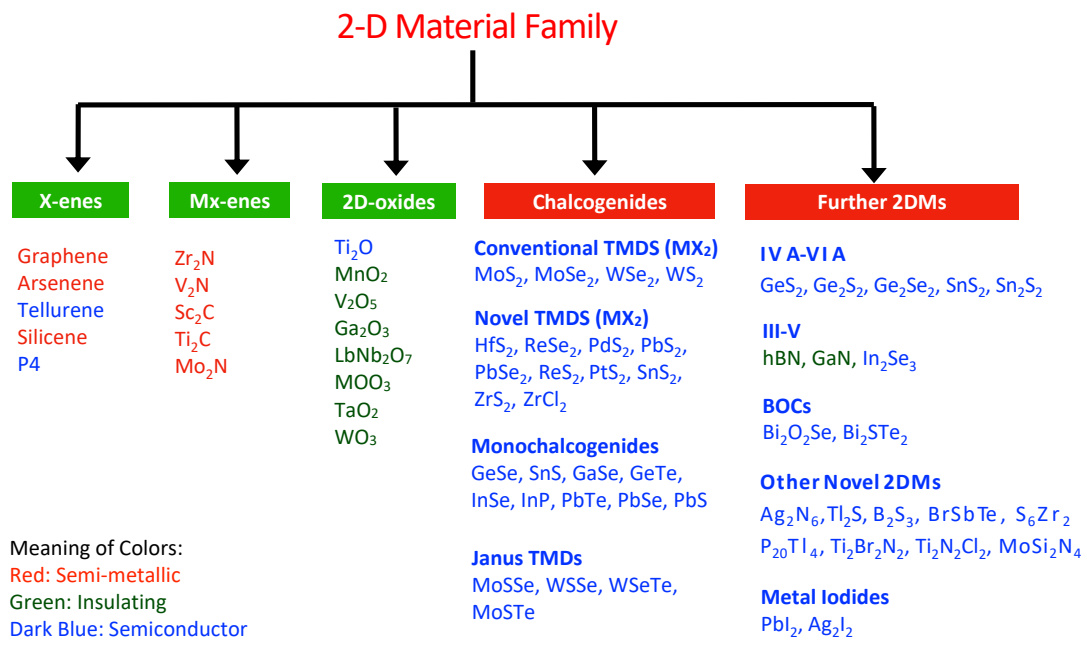

Figure 3.1: Classification of the two-dimensional materials (2DMs).

Recent DFT studies have revealed the existence of a diverse range of 2DMs with metallic, semiconducting, and insulating properties [22], [68]. Fig. 3.1 classifies the 2DMs into different categories, which are described below.

- **X-enes** - The first discovered 2-D material graphene belongs to this category. X-enes class includes the hexagonal lattices with a single element, including graphene, silicene, germanene, phosphorene, and stanene. These materials are gapless and known as Dirac materials, while phosphorene is a semiconductor with a significant energy gap [69]. X-anes are closely related to X-enes, but they have additional out-of-plane bonding with hydrogen atoms. Graphane nanoribbon, silicane, and germanane are examples of X-anes, which possess substantial energy gap by introducing quantum confinement in the X-enes class [67].

- **MX-enes** - MX-enes class consists of the transition metals (M) and carbides and nitrides of (X), which are synthesized through the selective etching of strongly bonded layered solids [70]. Most MX-enes family materials exhibit semimetallic properties [71]. The structured MX-ene sheets have found diverse applications, serving as catalysts, lubricants, and components in hybrid supercapacitors

- **2D-oxides**- 2DM oxides encompass MO, MO_x, and M_xO_y configurations, where M represents metals, and x and y denote potential oxidation states, as well as perovskite-type oxides. Their ultra-thin nature ensures a significant exposure of atoms at the surfaces, leading to novel properties and applications not typically observed in traditional bulk oxides [72]. The crystal structures of these 2DM oxides exhibit a wide spectrum, ranging from cubic to triclinic symmetry, contributing to their diverse range of properties and potential applications.

- **Chalcogenides** - Chalcogenides consist of a transition metal (M) and a chalcogen (X or Y), which can be S (Sulfur), Se (Selenium), or Te (Tellurium), forming hexagonal-lattice structures of MX, MX_2, and MXY layers. This classification encompasses widely studied conventional TMDs (MX_2), including MoS_2, WSe_2, and WS_2, which have garnered tremendous research attention as channel materials [67]. On the other hand, the list expands to include recently discovered novel TMDs (MX_2), such as ReS_2, HfS_2, ZrS_2, PdS_2, etc. Due to their unique combinations of transition metals and chalcogens, novel TMDs represent a new frontier in semiconductor research. Notably, semiconducting group 4 TMDCs, including ZrS_2, $ZrSe_2$, HfS_2, and $HfSe_2$, have recently emerged as promising candidates for various semiconductor applications and have shown promise in advancing electronic and optoelectronic technologies [22]. Group-IV monochalcogenides (MX) is a family of layered van der Waals materials that includes GeS, GeSe, SnS, SnSe, among others. Janus 2DMs (MXY), such as MoSSe, WSSe, MoSTe, WSeTe, are recently synthesized TMDs where the top chalcogenide layer is entirely replaced with a different chalcogenide, resulting in an asymmetrical out-of-plane structure [73].

- **Further 2DMs** - Further theoretical investigations suggest the stability and potential energy gaps ranging from 1 to 3 eV in various classes of 2DMs, including IV–IV, and III–V compounds [22], [67]. Several 2-D layered composites in the group V-VI material category are gaining considerable attention due to their potential applications in thermoelectric systems, including compounds like Bi_2Te_3

and Bi_2O_2Se [74]. The list also includes $MoSi_2N_4$, which belongs to a family of emerging 2DMs described by the chemical formula MX_2Y_4 [75], where M represents a transition metal, and X and Y can be the group IV and V elements, respectively. The metal iodide group exhibits a layered structure in which metal atoms create a central layer nestled between two layers of iodine atoms. The prevailing configuration among these materials is the stable 2H polytype.

As the synthesis of these materials is still in its early stages of development, there is a growing need to identify the most suitable material from this diverse class for FETs.

3.3 Device Geometry

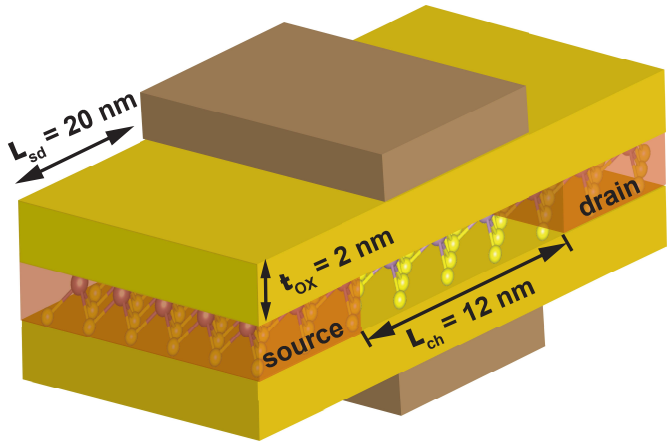

Figure 3.2: Schematic of the double gate 2DM-FET (NFET and PFET) considered for the simulation, where the device parameters are taken from the IRDS 2021 projection [13].

Fig. 3.2 illustrates the considered double gate geometry of n-MOSFET, with device design parameters sourced from the IRDS 2021 projection for the 1 nm technology node [13]. The channel material consists of an intrinsic monolayer sheet of 2DM with a length of $L_g = 12$ nm. The source (S) and drain (D) regions are both considered to be n-type doped regions, with a doping concentration of approximately $N_{S/D} = 5{\times}10^{13}$ cm^{-2} and a length of around $L_{S/D} = 20$ nm. For the gate-oxide material, Al_2O_3 is employed as both the top and bottom gate-oxide, with a thickness of approximately 2 nm and a dielectric constant of 10. This thickness represents the equivalent oxide thickness (EOT) of approximately 0.78 nm. In this simulation, the p-MOSFET (PFET) has nearly identical device geometry to the n-MOSFET (NFET), except that the source and drain regions are doped as p-type dopants.

3.4 Selection of 2-D Materials

The Atlas of 2DMs lists more than 1800 materials [22, 68], but this work focuses on selecting 40 2DMs which could provide excellent switching performance metrics for ultra-scale technology nodes. The following criteria have been adopted for shortlisting promising 2DMs for MOSFETs: (i) 2DMs should be structurally stable, which is verified by investigating the non-negative branches in the phonon band structure using DFT simulations; (ii) 2DMs should possess an energy gap larger than 1 eV, as the switching ratio is approximately related to $\exp(-E_g/kT)$ [76]; (iii) anisotropic materials with low transport and a high density of states effective mass should be given more preference, as they can allow for higher thermionic current components; and (iv) the thickness of the material should be less than 1.5 nm to achieve excellent gate electrostatic control. Fig. 3.1 shows the shortlisted novel 2DMs, which are qualified for considered selection criteria.

3.5 Multi-scale modeling of 2-D material-based FETs

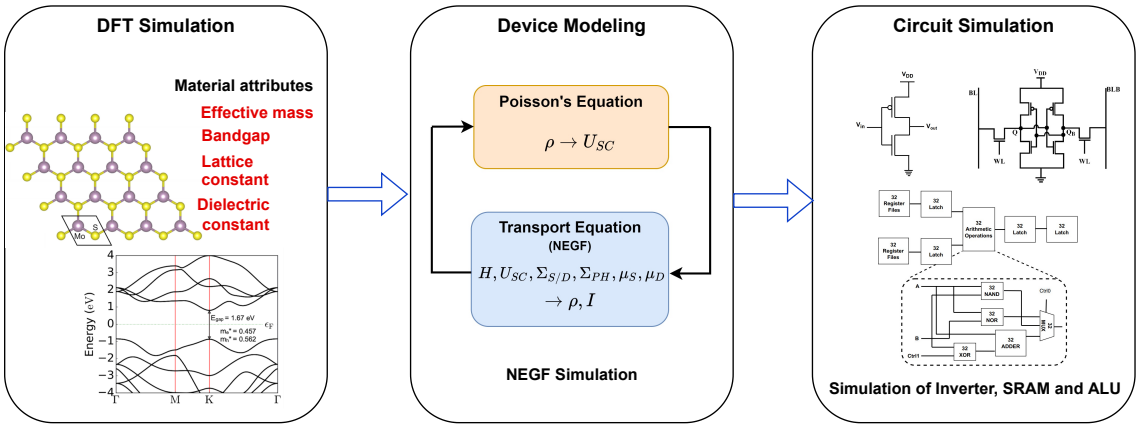

Figure 3.3: Multi-scale modeling of 2DM-based FETs from material-to-device-to-circuit.

Fig. 3.3 summarizes the developed multi-scale modeling approach for examining the device-to-circuit level performance of novel 2DMs. The initial step in the multi-scale modeling methodology is to acquire the material attributes from DFT simulations. These material attributes are then used in a quantum transport simulation to accurately predict short-channel performance. Further, the netlist level simulation is implemented to estimate the circuit performance. The proposed multi-scale modeling approach translates the material attributes into the circuit-level design, addressing the challenges of developing a design technology co-optimization tool for novel 2DMs.

3.5.1 DFT Simulation of Selected 2-D Materials

DFT simulation of the novel 2DMs is performed to determine material attributes, including effective mass, energy gap, and lattice constant. The DFT simulations involve identifying a unit cell of the 2DM and implementing a 20 Å vacuum space to eliminate fictitious interactions between a 2DM layer and its periodic images. The K-point sampling of the Brillouin zone is set to be equal to the density of K-points along the unconstrained direction in Γ-centered Monkhorst-Pack grids, with a density mesh cutoff approximately 1.5 times the default value. The PulayMixer algorithm is employed with a maximum of 150 iteration steps for enhancing the convergence of self-consistent field iterations. The fast Fourier transform (FFT) is utilized to solve the Poisson equation. The electronic structures are calculated using Generalized Gradient Approximation (GGA) exchange-correlation and the Perdew-Burke-Ernzerhof (PBE) functional, along with the OpenMX (Open Source package for Material eXplorer) norm-conserving pseudopotential. For geometry optimization of the 2DM unit cell, the LBFGS (Limited-memory Broyden-Fletcher-Goldfarb-Shanno) algorithm is employed with a maximum force tolerance of 0.01 eV/Å and stress tolerance value of 0.001 eV/Å^3.

To calculate the phonon dispersion and density of states in QuantumATK, the ForceField calculator based on the frozen phonon method is used. For this purpose, a supercell of the 2DM is selected with a reduced force tolerance of 0.001 eV/Å and stress tolerance of 0.001 eV/Å^3 for geometry optimization. The first derivative of the forces in the frozen phonon method is calculated using a finite difference scheme by applying small displacements of 0.01 Å to the supercell along the unconfined directions. The dynamical matrix is further used to compute the phonon properties of 2DMs.

3.5.2 Quantum Transport Simulation

The evaluation of device performance is conducted by developing a dissipative quantum-transport model, as elaborated in Chapter 2.

3.5.3 Circuit Simulation

To assess the logic performance of 2DM-FETs, three essential digital circuits are designed: the CMOS inverter, 6T SRAM, and 32-bit ALU. The performance of these logic circuits is computed using the BCB methodology [77], [78]. In this methodology, device-level geometrical parameters, current, and capacitance of the intrinsic device, as well as process technology parameters such as metal half-pitch, contact resistance, capacitance, and resistance of interconnect, are utilized to predict the performance of

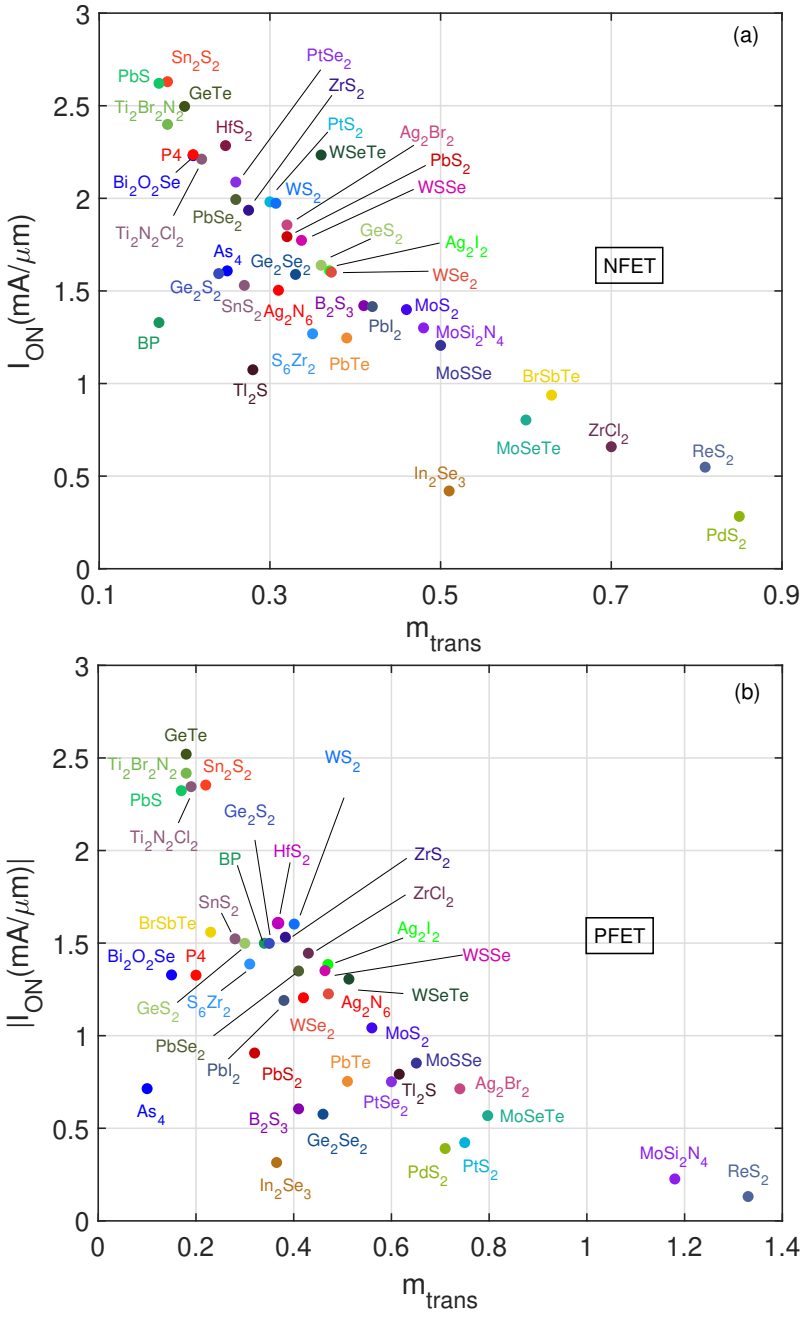

Figure 3.4: ON-state current (I_{ON}) of 40 novel 2DM-in (a) NFET and (b) PFET configuration at $V_{DS} = 0.6$ V.

logic circuits in terms of delay, energy consumption, and throughput.

3.6 Results

Fig. 3.4(a) and (b) shows the ON-state current [$I_{ON} = I_{DS}\,(V_{GS} = V_{DS} = 0.6V)$] of 40 2DM-based NFETs and PFETs, respectively, as a function of the transport effective mass (m_x) at $V_{DS} = 0.6$ V. The I_{ON} of both devices is calculated at the fixed OFF-state current [$I_{OFF} = I_{DS}\,(V_{GS} = 0, V_{DS} = 0.6V)$] of around 10 nA/$\mu$m, which is based on IRDS 2021 requirements for the 1 nm node

The ON-state current of 2DM-based NFETs and PFETs is determined by device parameters, including the tunneling probability across the source-to-channel potential barrier (T_{BTBT}), the velocity of charge carriers (v), the density of states (DOS), and quantum capacitance (C_q). These factors in terms of material attributes can be described using the following expressions:

$$T_{BTBT} \propto exp(-c\sqrt{m_x}) \quad [79] \tag{3.1}$$

$$v = \frac{1}{\hbar}\frac{dE}{dk} = \frac{\hbar k}{m_x} \quad [79] \tag{3.2}$$

$$\text{DOS} = \frac{g_s g_v \sqrt{m_x m_y}}{2\pi\hbar^2} \quad [53] \tag{3.3}$$

$$C_q \propto DOS \quad [53] \tag{3.4}$$

where, c is a parameter that relies on both the height and width of the potential barrier, m_x and m_y are the effective mass along transport and transverse directions, respectively, E is the energy, and k is the momentum vector. The complex interplay among these four factors collectively determines the ON characteristics of 2DM-FETs.

- From Eq. 3.1, it can be inferred that lower values of m_x result in considerable source-to-drain tunneling current in the OFF-state. This necessitates a much larger negative gate bias to achieve the fixed OFF-state current, considerably reducing the I_{ON} at a fixed value of V_{DD} window.
- As demonstrated in Eq. 3.2, a larger value of m_x can reduce the carrier velocity, which leads to lower thermionic current components and, consequently, a lower I_{ON}.
- If both m_x and m_y are higher, significantly lower values of velocity (v) and quantum capacitance (C_q) result in smaller I_{ON} among 2DMs.
- 2DMs with anisotropic effective mass, featuring a moderately lower m_x and a moderately larger value of m_y, allow for a considerably large value of I_{ON}. This is because m_x in this range ensures sufficiently high velocity (v), while maintaining higher DOS, as inferred from Eq. 3.2 and Eq. 3.3.
- 2DMs with higher m_x could exhibit considerably higher Cq, exceeding the quantum capacitance limit. This leads to poor gate electrostatic control, which limits the ON-state current of the device.

Among the 2DMs, $MoSi_2N_4$ and ReS_2 with $m_x > 1.1$ exhibit a considerably low value of $I_{ON} < 0.25$ mA/μm in PFET configuration owing to the significantly lower v.

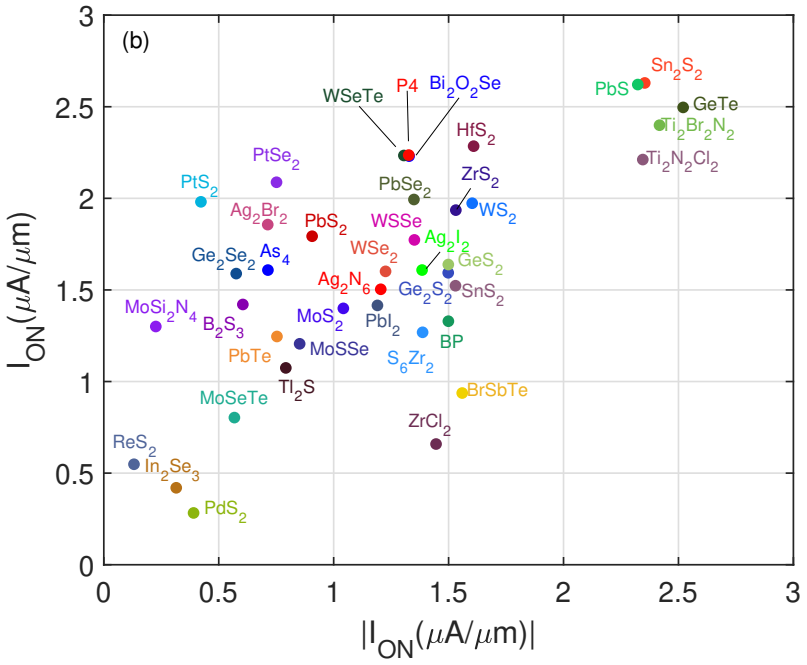

Figure 3.5: NFET I_{ON} vs. PFET I_{ON} of the considered novel 2DM-based FETs at V_{DS} = 0.6 V.

Additionally, ReS_2 with $m_x > 0.8$ has lower I_{ON} among 2DMs in NFET due to increased quantum capacitance. Specially, 2DMs with m_x in between 0.2-0.45 promise moderate I_{ON} current in the range of 1–1.5 mA/μm, for both NFET and PFET. This is because m_x in this range ensures sufficiently high v, while source-drain tunneling current affects the OFF-state characteristics. It is also observed that 2DMs with m_x = 0.35-0.4, such as PbI_2, B_2S_3, exhibit the I_{ON} of around 1.45 mA/μm in NFET, as that of MoS_2. In contrast, Ag_2I_2, GeS_2, $GeSe_2$, and As_4 with m_x = 0.25-0.35 offer moderately higher I_{ON} of around 1.65 mA/μm in NFET, nearly similar to that of WSe_2. The IRDS 2021 projects an I_{ON} of around 1.75 mA/μm for 1 nm technology node without contact resistance, which is easily achieved by five materials in both PFET and NFET, namely, GeTe, PbS_2, Sn_2S_2, $Ti_2Br_2N_2$, and TiN_2Cl_2. Therefore, the 2DMs with moderately lower m_x and higher m_y could be better suited as a channel material to achieve higher I_{ON}.

Fig. 3.5 displays the I_{ON} of NFET vs I_{ON} of PFET for the 40 2DMs. It is found that certain 2DMs, such as Tl_2S, MoSeTe, Ag_2I_2, SnS_2, $Ti_2N_2Cl_2$, $Ti_2Br_2N_2$, and GeTe, give symmetric and higher I_{ON} among the 2DMs, for both NFET and PFET. This makes them a favorable choice for CMOS technology as they can provide an identical low-to-high and high-to-low delay with same size device for the PFET and NFET.

Fig. 3.6 (a) and (b) illustrate the SS versus the I_{ON} of the 2DM-based NFETs and PFETs, respectively, for the fixed I_{OFF} of 10 nA/μm at V_{DS} = 0.6 V. It is observed that GeTe, TiN_2Cl_2, PbS_2, Sn_2S_2, and $Ti_2Br_2N_2$ based NFET and PFET promises lower

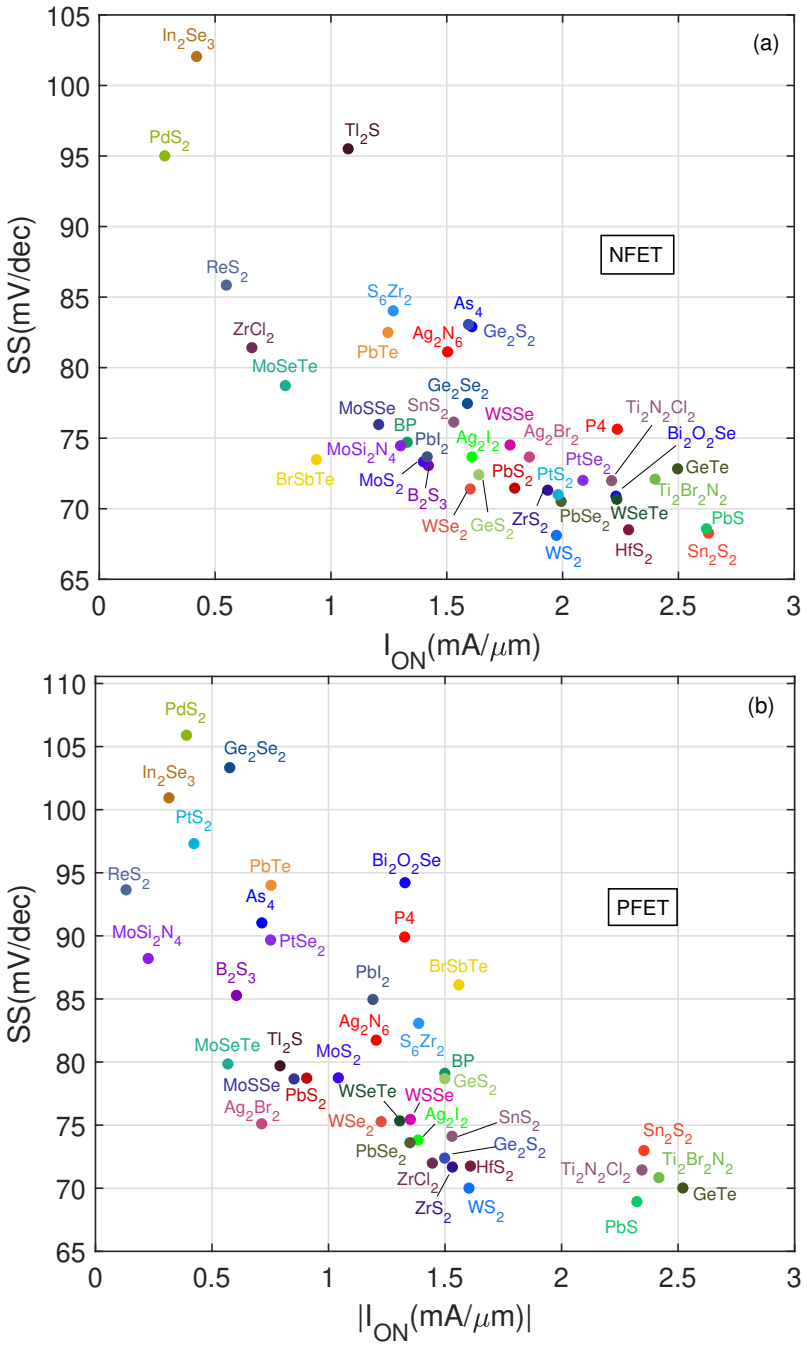

Figure 3.6: Subthreshold swing (SS) of the considered novel 2DM-based (a) NFETs and (b) PFETs as a function of $|I_{ON}|$ at $|V_{DS}| = 0.6$ V.

SS because of lower source-to-drain tunneling. Additionally, certain 2DMs, such as PbS, Sn_2S_2, and $PbSe_2$, which are characterized by lower m_x values, exhibit improved SS owing to their reduced C_q values. Most of the 2DMs with I_{ON} in the range of around 1.3–2 mA/μm, such as B_2S_3, $MoSi_2N_4$, Ag_2I_2, GeS_2, PbS_2, WSSe, Ag_2Br_2, PtS_2, $PbSe_2$, ZrS_2 in NFET, and Ag_2I_2, Ge_2S_2, HfS_2, $PbSe_2$, ZrS_2, $ZrCl_2$, WSSe in PFET, demonstrate SS of around 70 mV/dec to 75 mV/dec. Fig. 3.7(a) and (b) show the C_g versus m_x of the 2DM-based NFET and PFET, respectively at $V_{DS} = 0.6$ V. Here, C_g is a series

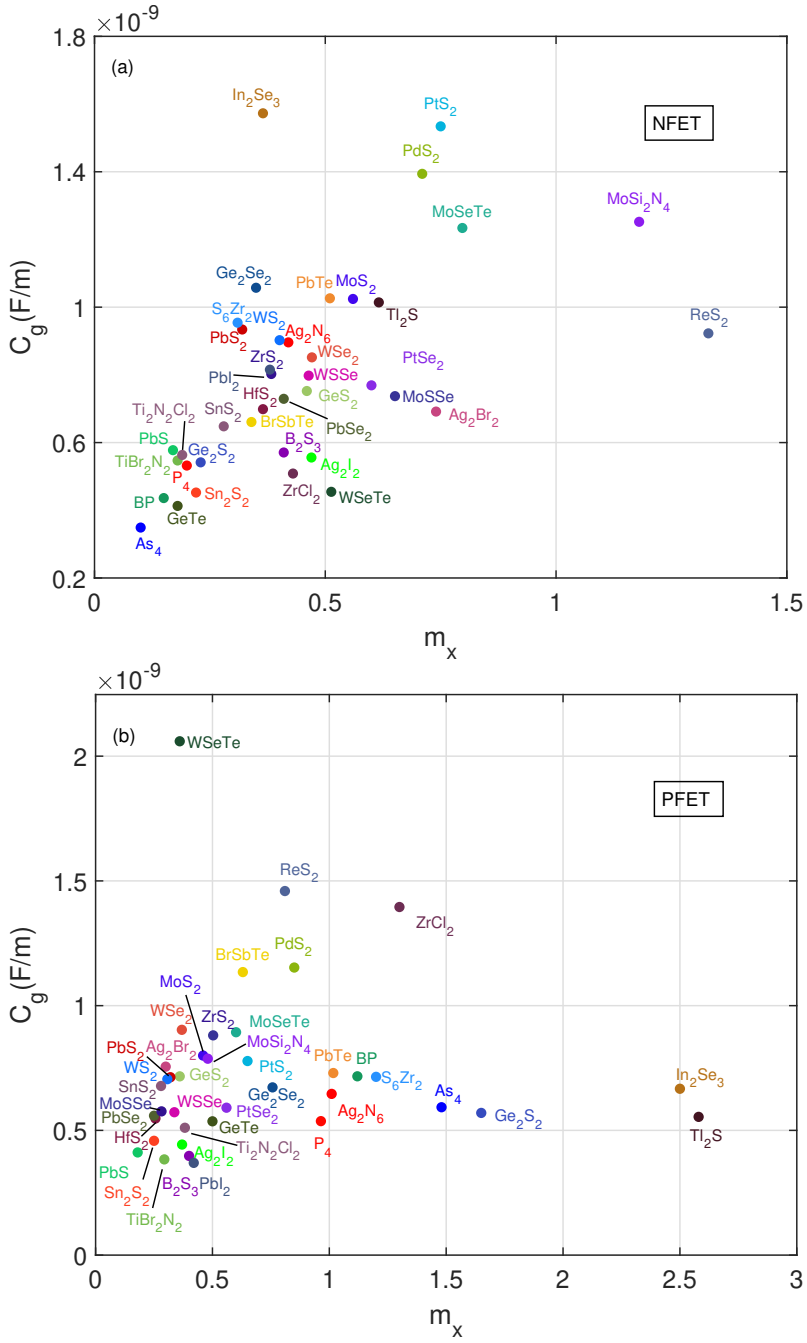

Figure 3.7: Gate capacitance (C_g) of the considered novel 2DM-based (a) NFETs and (b) PFETs as a function of m_x at $|V_{DS}| = 0.6$ V.

combination of oxide capacitance (C_{ox}) and quantum capacitance (C_q), given by $C_g = C_{ox}C_q/(C_{ox} + Cq)$. It is observed that 2DMs with lower m_x and m_y values exhibit a reduced C_g compared to those with higher m_x and m_y. This trend arises because higher values of m_x and m_y result in a larger quantum capacitance C_q. Especially, 2DMs with m_x in the range of 0.25-0.35, such as GeTe, Sn_2S_2, BP, and As_4 in NFET, and Sn_2S_2, PbS, $Ti_2Br_2N_2$ in PFET, show $C_g < 0.5$ fF/μm.

Fig. 3.8(a) and (b) show the intrinsic device delay versus the power-delay product

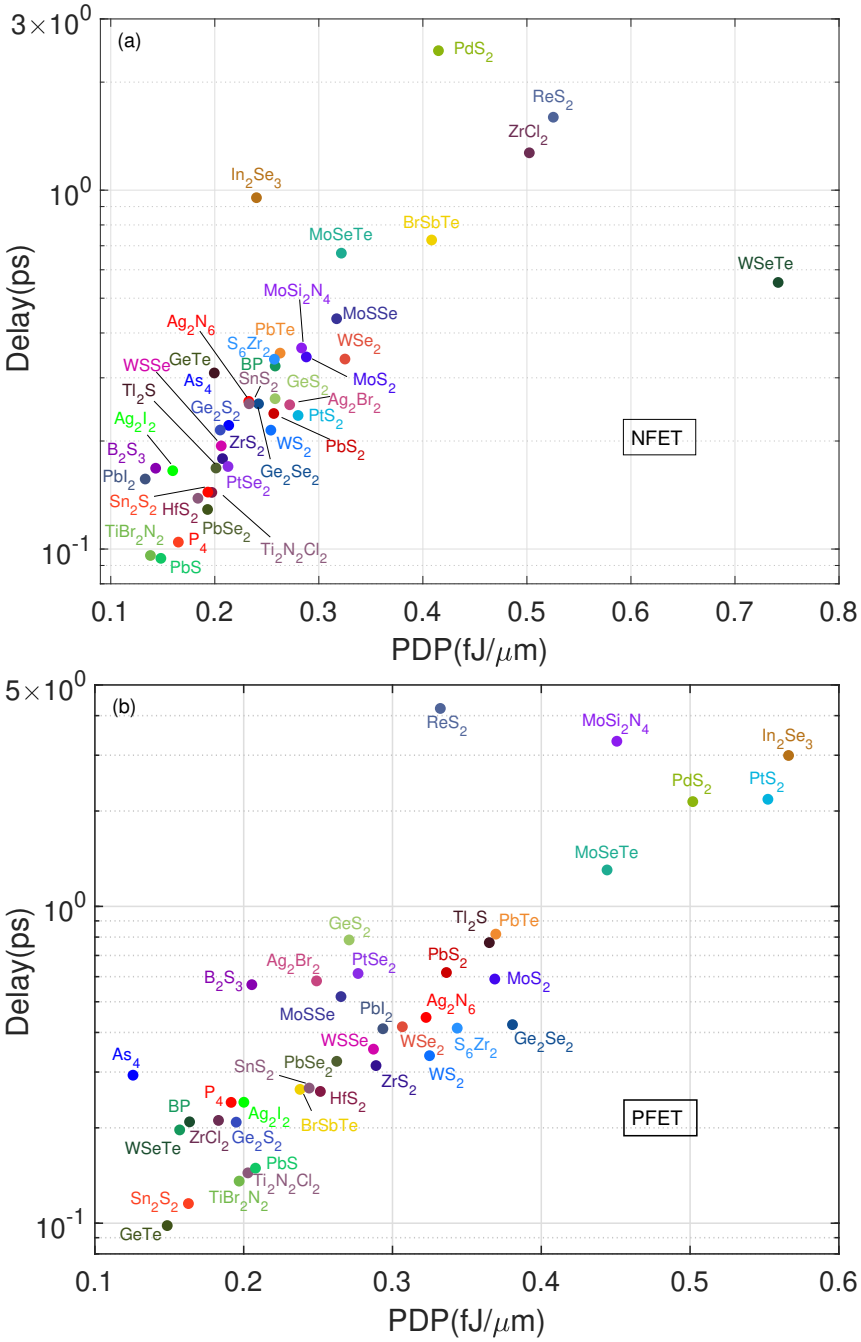

Figure 3.8: Intrinsic delay versus PDP for the 2DM-based (a) NFETs and (b) PFETs at $V_{DS} = 0.6$ V.

(PDP) of the 2DM-based NFETs and PFETs, respectively, for the fixed I_{OFF} of 10 nA/μm. The delay of the devices is calculated as $\tau = C_g V_{DD}/I_{ON}$, where C_g is the gate capacitance, V_{DD} is the supply voltage. It is observed that 2DMs, such as Sn_2S_2, PbS, and $Ti_2Br_2N_2$ with smaller m_x, demonstrate significantly lower value of intrinsic device delay. This is because a lower value of m_x leads to higher I_{ON}, allow considerably faster charging and discharging of the load capacitance. Among the selected 2DMs, PbS and GeTe show the lowest intrinsic delay of around 0.95 ps and 0.98 ps in PFET and NFET, respectively,

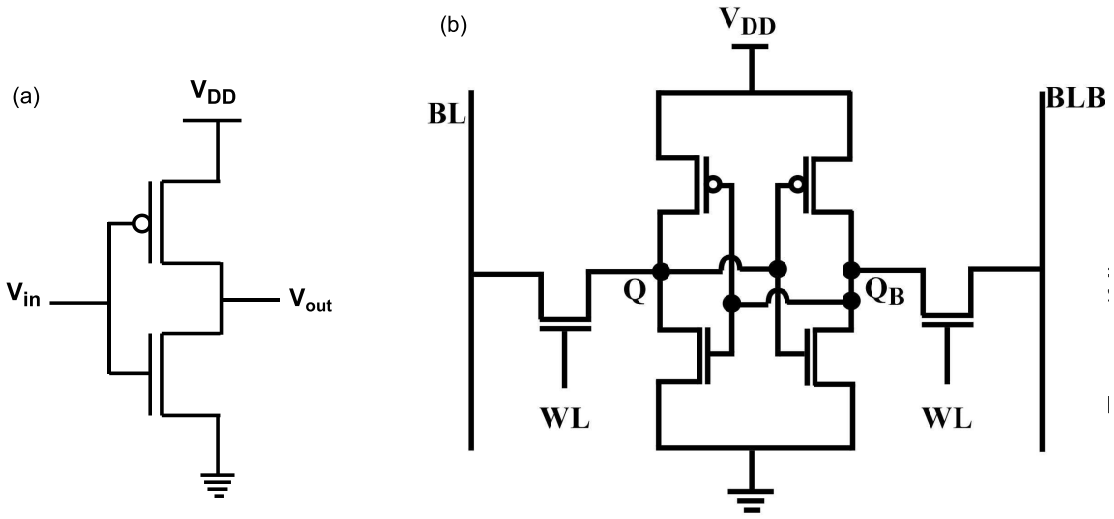

Figure 3.9: Schematics of the (a) CMOS inverter and (b) 6-T SRAM with the selected 2DMs.

which is around 0.31× and 0.21× lower than the delay of MoS_2 in PFET and NFET, respectively. Further, the PDP for most of the 2DMs in both PFET and NFET lies in the range of 0.4 fJ/μm. 2DMs, such as In_2Se_3, PdS_2, and ReS_2 show considerably higher values of the delay and PDP in both PFET and NFET due to lower I_{ON} and higher C_g.

3.6.1 CMOS inverters based on novel 2DMs

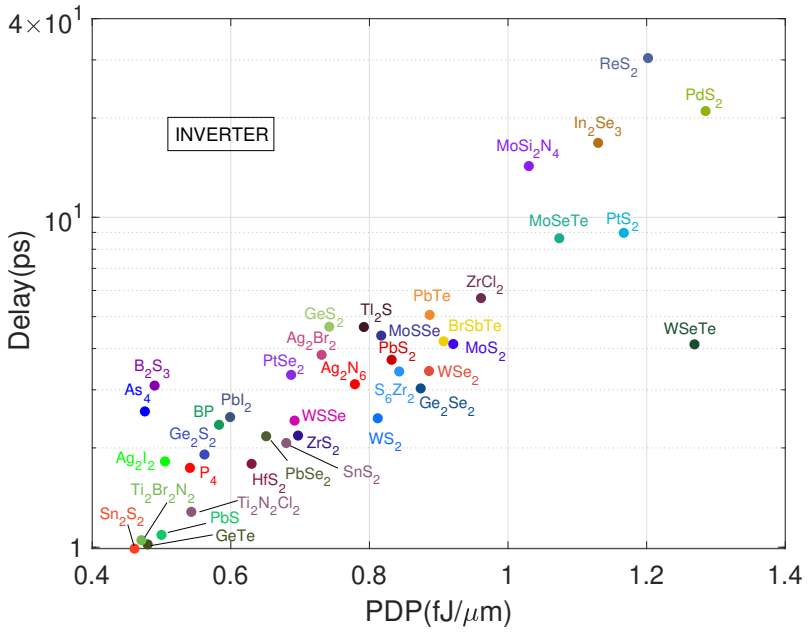

Figure 3.10: Switching delay as a function of the power-delay product (PDP) of CMOS inverter with the selected 2DMs.

In this section, the CMOS inverter and 6T SRAM cell are designed with selected 40 2DMs to derive their performance for more complex digital circuits. Fig. 3.9 (a) shows the

schematic of the CMOS inverter design, which comprises pull-up p-MOS and pull-down n-MOS. Fig. 3.10(a) shows the delay as a function of PDP for the CMOS inverters based on the selected 2DM. The delay of the inverter is calculated as the difference between the times of the 50% transition in the output and input pulses. It is observed that among the selected 2DMs, GeTe, PbS, Sn_2S_2, $Ti_2Br_2N_2$, and $Ti_2N_2Cl_2$ demonstrate the lower delay and PDP in CMOS inverter configuration. Compared to the most popular TMD material MoS_2, these materials show nearly 0.24-0.31× lower delay and nearly 0.50-0.59× lower PDP, respectively. Therefore, GeTe, PbS, Sn_2S_2, TiN_2Cl_2, and $Ti_2Br_2N_2$, are more favorable candidates among 2DMs for high-speed and low-power applications.

3.6.2 6T SRAM cell with novel 2DMs

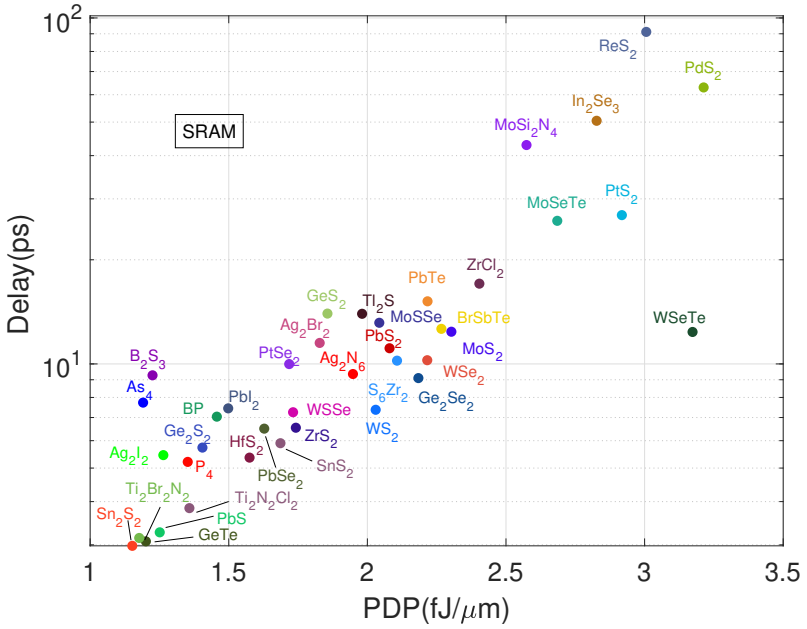

Figure 3.11: Switching delay as a function of the power-delay product (PDP) of 6-T SRAM with the selected 2DMs.

Fig. 3.11 shows the delay as a function of PDP for the 6T-SRAM cell [see Fig. 3.9 (b)] based on the selected 40 2DMs. The delay is determined by considering the average of the read and write delay of the SRAM cell. It is observed that 2DMs, namely, GeTe, Sn_2S_2, and $Ti_2Br_2N_2$, maintain their switching benefits of inverter level to SRAM cell with lower delay and PDP. As observed in CMOS inverter, these 2DMs offer considerably higher switching speed with nearly 0.26-0.33× lower delay and nearly 0.54-0.61× lower PDP, compared to MoS_2. The enhanced switching speed and reduced power dissipation observed in these 2DMs suggest their potential as strong candidates for next-generation digital logic applications.

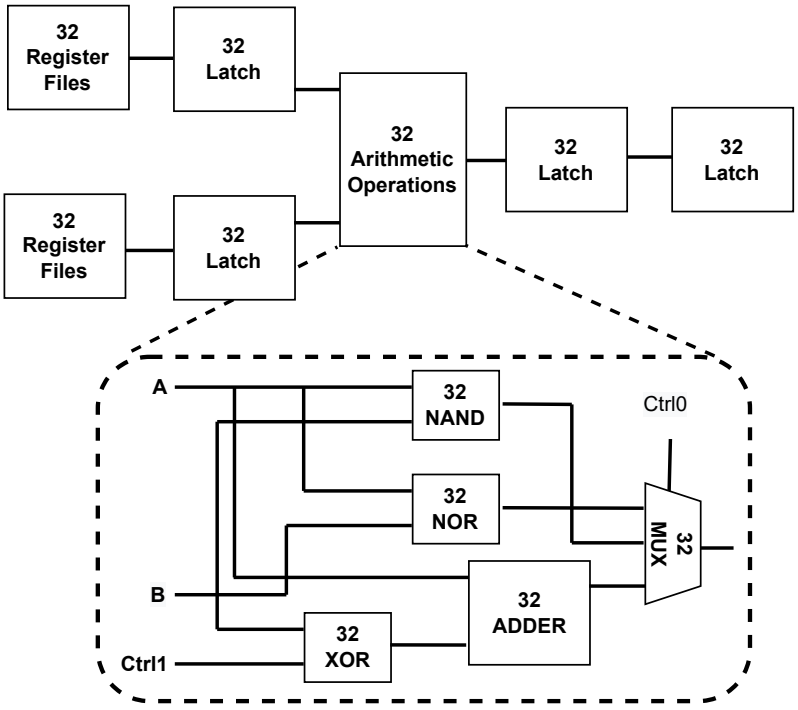

Figure 3.12: Block level schematic of 32-bit ALU with the selected 2DMs.

3.6.3 Performance of 2DMs in 32-bit ALU

To evaluate the system-level performance potential of the selected 2DMs, a comprehensive performance analysis of the 32-bit ALU is conducted. This investigation considers not only the intrinsic capacitances but also accounted parasitic elements for a more accurate assessment. Fig. 3.12 shows the block level schematic of the 32-bit ALU, where the main Arithmetic Operation (AO) block containing full adder, multiplexer, multi-input NAND, NOR, and XOR gates are implemented using various 2DM-based FETs. In addition to the AO block, the ALU comprises two other vital components, i.e., the register files (RFs) and a latch.

Fig 3.13(a) shows the energy versus delay of the 32-bit ALU based on the selected 2DMs. It is observed that 2DMs such as GeTe, Sn_2S_2, $Ti_2Br_2N_2$, and PbS have exhibited switching energy of around 2.14-25.35 fJ and lower switching delay of around 0.9-1.09 ns. Compared to MoS_2, these 2DMs exhibit around 3.7-3.8× higher speed while consuming around 0.52-0.58× lower energy. Therefore, 2DMs with low to moderate effective mass in the transport direction and higher transverse effective mass could provide superior prospects for low-power and high-speed ALU unit.

In numerous computing applications, power density stands as a critical constraint, imposing an upper limit on the maximum operating speed of digital IC. Thus, it is important to explore throughput as a function of power density. Fig 3.13(b) illustrates

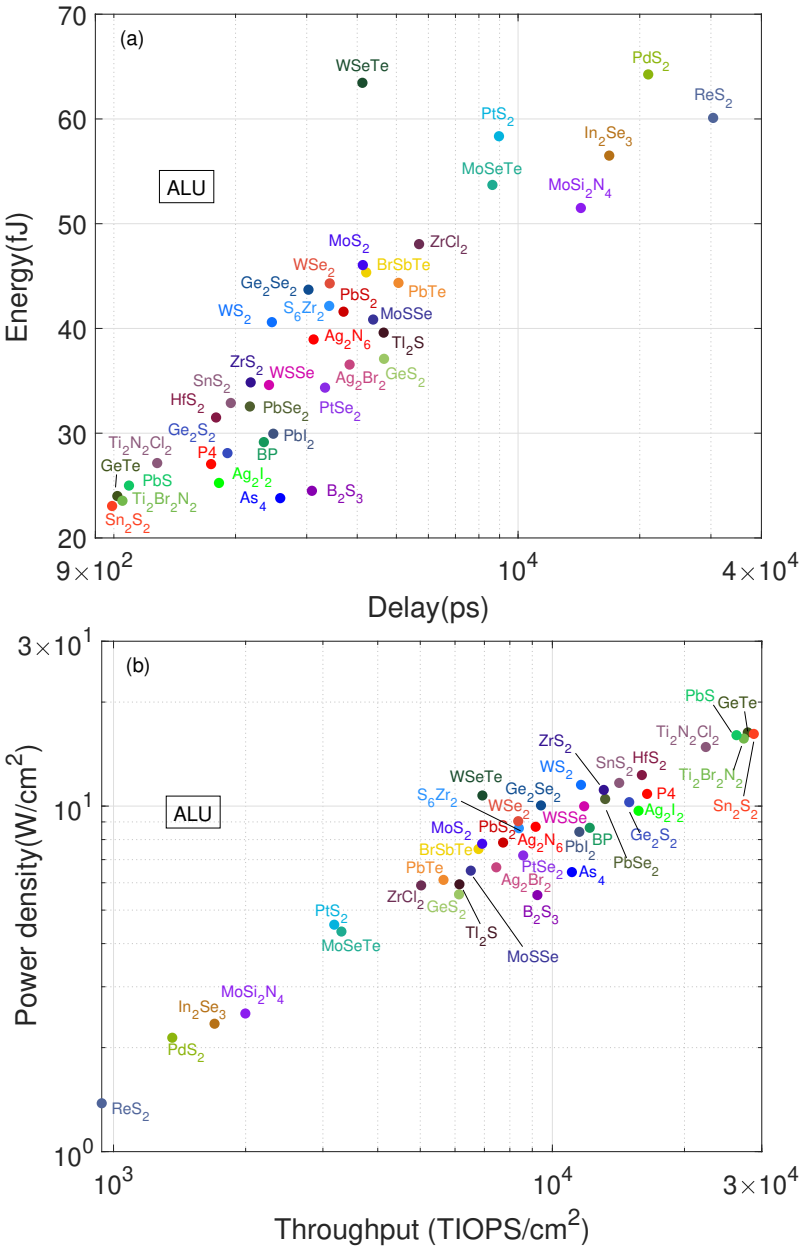

Figure 3.13: Performance projection of 32-bit ALU: (a) Switching energy versus delay and (b) Dissipated power versus computational throughput in tera-integer operations per sec (TIOPS) per cm^2 for the considered 2DM-based 32-bit ALU.

the power density versus computational throughput in tera-integer operations per second (TIOPS) per square centimeter of the 32-bit ALU based on the selected 2DMs. The computational throughput is determined as the inverse of the circuit delay time divided by the circuit area. It is observed that despite GeTe, Sn_2S_2, $Ti_2Br_2N_2$, TiN_2Cl_2, and PbS show higher throughput, they consume higher power compared to other 2DMs. Interestingly, these five 2DMs maintain their inverter level performance benefits in ALU with around 3.25-4.17× higher throughput over conventional TMD such as MoS_2. Further, 2DMs, namely ReS_2, In_2Se_3, PdS_2 show considerably lower throughput compared to other

2DMs, while exhibiting lower power density to perform ALU operations.

3.7 Summary

Using a multi-scale modeling methodology, this chapter has investigated the device-to-circuit level performance analysis of a diverse set of 40 emerging 2DMs. The results reveal that five 2DMs, namely, GeTe, PbS, Sn_2S_2, $Ti_2N_2Cl_2$, and $Ti_2Br_2N_2$, and have promised excellent switching performance with higher I_{ON}, lower device delay and lower power delay product among 40 set of emerging 2DMs. Further, it has found that these five 2DMs maintain their superior performance at the circuit level in the CMOS inverter configuration and 6-T SRAM cell with faster speed and lower power dissipation. These five 2DMs have exhibited notably superior throughput in ALU compared to other 2DMs, but at the expense of higher power consumption. This comprehensive analysis serves as a valuable guide for optimizing 2DM-based FETs, with the prospect of replacing Si in future technology nodes.

Chapter 4

Analysis and Modeling of Interface Trap States in MoS_2-FET

4.1 Introduction

2-D molybdenum disulfide (MoS_2) has emerged as a prominent contender for the future ultra-scaled CMOS devices due to its carrier mobility comparable to silicon, easy and large-scale synthesis techniques, and three-dimensional integration feasibility [12], [14]. The MoS_2-FET has shown impressive switching performance with an ON-OFF current ratio of approximately 10^6 and a subthreshold slope (SS) of approximately 65 mV/dec even at ultimate scaling limit of 1 nm gate length [19]. Despite the promising aspects, the majority of fabricated MoS_2-FETs have reported the interface trap density (D_{IT}) of 10^{11}-10^{13} cm^{-2} eV^{-1}, regardless of the type of gate oxide used, including HfO_2, Al_2O_3, SiO_2 [27, 28, 29, 30]. The presence of high-density interface trap charges can introduce undesirable impediments to the MoS_2-FET performance, including loss of electrostatic control, mobility degradation, trap-assisted tunneling, and temperature instability. Therefore, a critical analysis of the interface trap states effect on short-channel MoS_2-FET is indispensable to develop more reliable and stable integrated circuits (ICs).

It has been found that the sulfur vacancy at the oxide-MoS_2 interface mainly provides distributed shallow trap states within the MoS_2 bandgap energy range [31], [32]. Although experimental efforts have confirmed the presence of interface trap charges, most simulation models have neglected the interface charge effect, which are leading to overestimation of MoS_2-FET performance [34], [80]. Some recent works have modeled the interface trap charge using the classical SRH model [81], [82], which fails to account for the quasi-localized nature of interface traps at ultra-scaled channel lengths. However, the interface trap states provide localized states within the bandgap that could affect both carrier transport and electrostatics [83]. The classical SRH model describes the interaction between carriers and traps at the interface using an average value of the interface trap density. However, this approach does not fully capture the complex interplay between various physical mechanisms, such as electrostatics, impurity scattering, trapping, and tunneling, that can affect the behavior of carriers in the vicinity of interface traps. This limitation is overcome in our quantum transport model for

interface traps, which generate quasi-bound localized interface states and account for a multitude of trap-related phenomena. he electric-field enhancement factors, which play a critical role in incorporating TAT current in the classical SRH, depend not only on the local electric field but also on the local density of states (LDOS) that participate in the tunneling process. The presence of interface trap charges could also increase the temperature sensitivity of device characteristics [83], but no study on MoS_2-FET has been conducted until now. Therefore, careful modeling and analysis of interface trap states on MoS_2-FET performance is urgently needed to minimize and optimize their effect on device performance.

This chapter presents a quantum-mechanical framework for modeling interface trap states in MoS_2-FET by introducing 0-D states within the self-consistent solutions of dissipative non-equilibrium Green's functions (NEGF) and Poisson's equations. The proposed framework provides a unified description of both single and multiple interface trap states by specifying the position, energy level, and area of the trap states. Using the developed model, this chapter attempts to answer the following questions regarding the effect of interface trap on MoS_2-FET performance:

(i) What is the physical mechanism responsible for the degradation of MoS_2-FET performance in the presence of interface trap states?

(ii) What are the energy and spatial range of interface trap states which can result in severe performance degradation?

(iii) How will trap states affect the key short channel performance metrics of MoS_2-FET?

(iv) In what ways will trap states modify the temperature dependency of MoS_2-FET?

(v) What design strategies can be employed to minimize interface trap effects on MoS_2-FET performance?

4.2 Device Geometry

Fig. 4.1 shows the considered double gate (DG) geometry of MoS_2-FET, where the trap site is located at the center of the channel at the top gate oxide-MoS_2 interface. The initial design parameters for MoS_2-FET are selected from the IRDS 2021 projection for the 1-nm technology node [13]. An intrinsic monolayer MoS_2 nanosheet serves as the channel material with a length of around $L_g = 12$ nm. The source (S) and drain (D) regions, which have a length of around 20 nm, are consisted of n-type doped MoS_2 nanosheet with

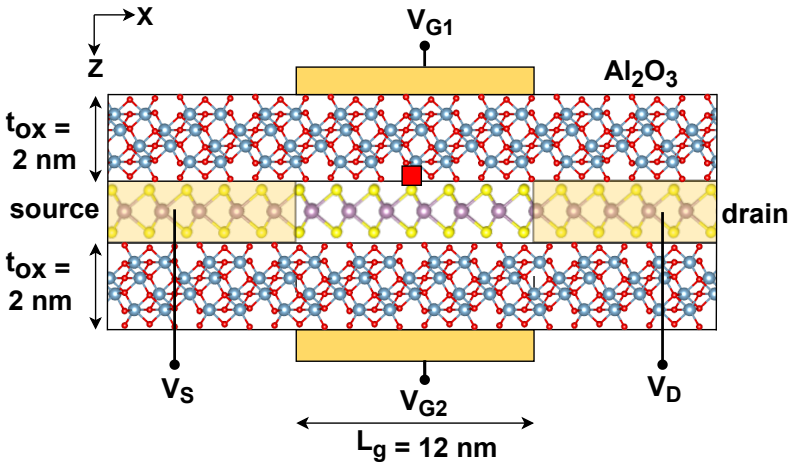

Figure 4.1: Device schematic of double-gate (DG) MoS_2-FET with a trap site (shown in red square) at the center of the channel.

the doping concentration of around $N_{S/D} = 5{\times}10^{13}$ cm^{-2}. The Al_2O_3 with a dielectric constant ($\varepsilon_{Al_2O_3}$) of 10 and a thickness (t_{ox}) of around 2 nm is considered as the top and bottom gate oxides that correspond to an equivalent oxide thickness (EOT) of around 0.78 nm.

4.3 Interface Trap Modeling

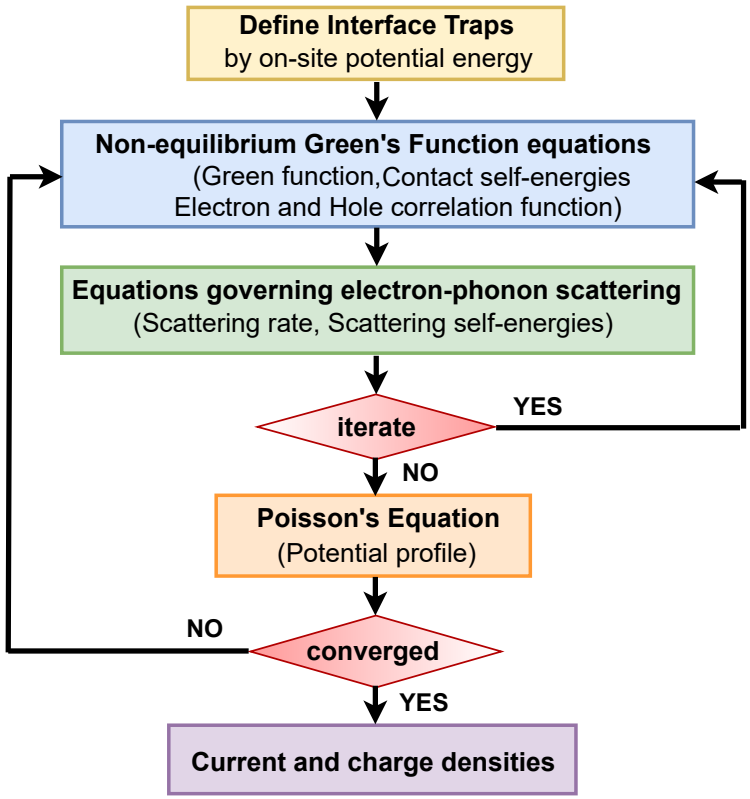

Figure 4.2: Interface trap modeling procedure within the dissipative NEGF-Poisson solver.

Fig. 4.2 summarizes the dissipative quantum-transport modeling framework for describing the interface trap states in MoS_2-FET. The dissipative quantum transport framework, discussed in Chapter 2, is employed here. To introduce the interface trap states at a specific position and energy in the quantum transport model, the on-site potential energy is modified in the Hamiltonian matrix of the device, as shown below:

$$U(r) = E_c(r) + \sum_{i=1}^{N} V_{trap}(r_i),\ r = r_t \tag{4.1}$$

$$U(r) = E_c(r),\ r \neq r_t \tag{4.2}$$

where, $E_c(r)$ is the self-consistent electrostatic potential energy across the device, N is the number of traps, and $r_t = (x_t, z_t)$ is the position of trap site. The position along the z-direction (z_t) is fixed at the oxide-channel interface. The interface trap in Eq. 4.1 enters with a square area potential well on top of the potential energy E_c at the r_t. This generates additional localized states within the energy gap of MoS_2 that correspond to interface states.

The previous studies have shown that acceptor-type interface trap states, which are located close to E_c, mainly impact the I_{DS}–V_{GS} characteristics of n-type MOSFET [62], [84]. In this work, the focus is to understand the effect of acceptor-type interface trap states on n-type MoS_2-FET by varying the value of the on-site potential energy (V_{trap}). However, it should be noted that V_{trap} can be used to introduce both donor- and acceptor-type states.

Fig. 4.3(a)-(d) show the source and drain-injected local density of states (LDOS) with E_c of MoS_2-FET for the four different V_{trap} values under the flat-band condition, when the trap site is located at the center of the channel (x_t = 26 nm from the source). It is observed from the LDOS spectra that varying the V_{trap} can introduce additional localized states within the bandgap. The trap energy level (E_{trap}) for the distributed trap states is defined as the centroid of the trap LDOS. These distributed trap states in MoS_2-FET have also been observed in recent experiments and TCAD simulations [85]. From Fig. 4.3(a)-(d), it is inferred that decreasing the strength of V_{trap} leads to the generation of lower energy trap states from E_c. Additionally, the trap states do not significantly affect the position and broadening of E_c due to the weaker effect of a single trap site.

Fig. 4.4 shows E_{trap} as a function of V_{trap} for two different trap cross-section areas (A_t) of around 0.25 nm^2 and 0.5 nm^2 under the flat band condition. It is observed that the energy level of the trap can be tuned from the conduction band minimum (CBM) at

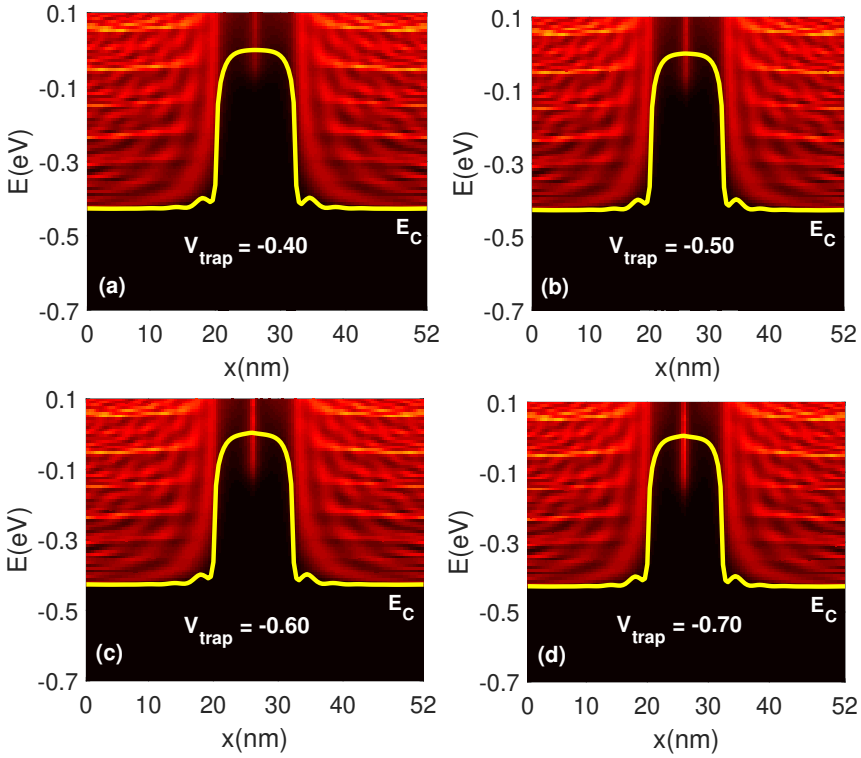

Figure 4.3: Local density of states (LDOS) with E_c of MoS_2-FET along the transport direction under flat-band condition for various values of on-site potential energy (V_{trap}) for the trap at fixed location x_t = 26 nm and A_t of around 0.25 nm^2.

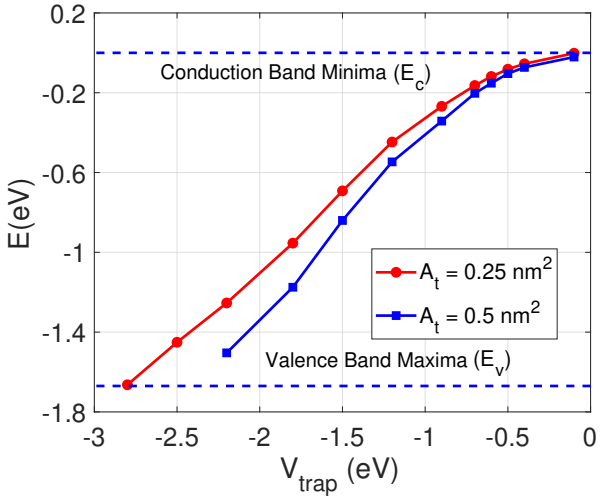

Figure 4.4: Interface trap energy level (E_{trap}) within the MoS_2 bandgap as a function of the on-site potential energy (V_{trap}) for the trap area (A_t) of around 0.25 nm^2 and 0.5 nm^2. The E_{trap} values are determined by taking E_c as the reference level.

0 eV to the valence band maximum (VBM) at −1.67 eV by adjusting V_{trap} within the range of −0.2 eV to −2.8 eV for traps with A_t of around 0.25 nm^2. Similarly, by varying the values of V_{trap} within −0.1 eV to −2.2 eV, the energy level of traps with A_t of around 0.5 nm^2 can be adjusted. Notably, the same value of V_{trap} for two different cross-section areas produces different energy-localized states, as the LDOS spectra are obtained by

self-consistently solving the Poisson's and NEGF equations. Hereafter, trap states are identified based on their E_{trap} values with E_c as the reference level, and the strength of V_{trap} is tuned to achieve the desired E_{trap} value. It is worth mentioning that the proposed Hamiltonian and trap definition can be easily extended to model multilayer MoS_2-FET and other 2DM-based FETs by modifying the material attributes.

4.4 Results

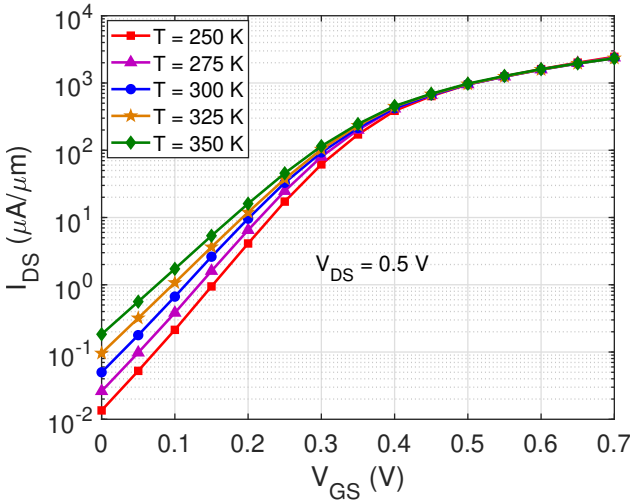

Figure 4.5: Transfer characteristics (I_{DS}–V_{GS}) of DG MoS_2-FET without trap states, obtained using dissipative quantum transport model at V_{DS} = 0.5 V for various device operating temperatures. The metal-semiconductor work function difference, ϕ_{ms}, is selected around -0.084 V at 300 K (room temperature) to achieve a constant OFF-state current.

Fig. 4.5 illustrates the transfer characteristics (I_{DS}–V_{GS}) of DG monolayer MoS_2-FET without interface trap states for the different device operating temperatures (T) at V_{DS} = 0.5 V. The OFF-state current [$I_{DS}(V_{GS} = 0, V_{DS} = 0.5\,\text{V})$] at room temperature (300 K) is set to approximately 50 nA/μm, which is achieved by tuning the work-function difference between the gate metal and semiconductor. It is observed that monolayer MoS_2-FET at 300 K exhibits the ON-state current [$I_{DS}(V_{GS} = V_{DS} = 0.5\,\text{V})$] of around 947.5 μA/μm with subthreshold slope (SS) of 78.35 mV/dec for 1 nm technology node. The improved ON-state current is attributed to two factors: (i) the atomically thin MoS_2 channel enhances the gate electrostatic control over the channel region, and (ii) the moderately high electron effective mass increases the density of states and, therefore, enhances the thermionic current component.

Fig. 4.5 shows that the OFF-state current without interface states slightly increases with increasing operating temperature, but the ON-state current remains largely

independent of temperature. The subthreshold slope (SS) is observed around 74.77 mV/dec, 78.35 mV/dec, and 90.59 mV/dec for temperatures of 250 K, 300 K, and 350 K, respectively. Here, threshold voltage (V_{TH}) is determined using the constant current method by considering the current density of around 1 μA/μm [86]. It is observed that the temperature coefficient dV_{TH}/dT of MoS_2-FET is found to be approximately -1.1 mV/K, which is indicating a weak temperature dependence.

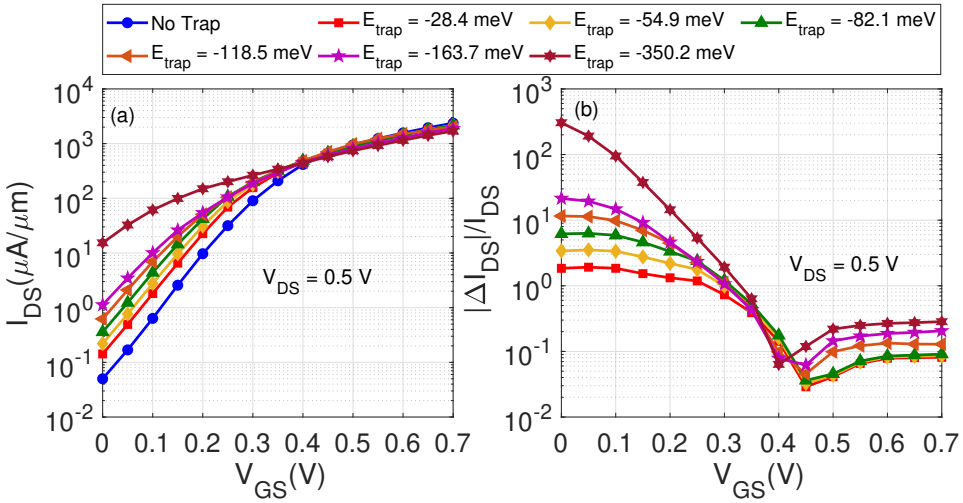

Figure 4.6: I_{DS}–V_{GS} characteristics of monolayer MoS_2-FET at $V_{DS} = 0.5$ V for a single trap located at $x_t = 26$ nm (middle of channel) for different trap energy levels (E_{trap}), and (b) Relative difference between the current in the trap and no trap case $|\Delta I_{DS}/I_{DS}|$ as a function of V_{GS} for different trap energy levels (E_{trap}).

Now focus is on understanding the MoS_2-FET performance degradation in the presence of a single interface trap site. Fig. 4.6(a) shows the I_{DS}–V_{GS} characteristics of MoS_2-FET for a single trap located at $x_t = 26$ nm (i.e., the center of channel region) with the trap energy in the range of 28.4-350.2 meV. The considered trap energies within the bandgap of MoS_2 are very close to experimentally reported values for the Al_2O_3-MoS_2 interface [87]. It is observed from Fig. 4.6(a) that the OFF-state current of MoS_2-FET increases significantly with decreasing the E_{trap} from the conduction band (E_c), while the ON-state current shows marginal decrement. The trap energy states ($E_{trap} = -350.2$ meV) close to $E_g/2$ have shown a significantly stronger influence on both OFF- and ON-state currents. It is observed in Fig. 4.6(b) that the relative difference between trap and no trap case current ($\Delta I_{DS}/I_{DS} = (I_{DS,trap} - I_{DS,no-trap})/I_{DS,no-trap}$) is positive and large for low V_{GS}, whereas $\Delta I_{DS}/I_{DS}$ for high V_{GS} becomes negative. Thus, a single trap site can degrade the OFF-state current, and the trap with E_{trap} beyond -350.2 meV has a considerably higher impact on the I_{DS}–V_{GS} characteristics.

To gain insight into this effect, the E_c profile and current spectra are plotted in Fig.

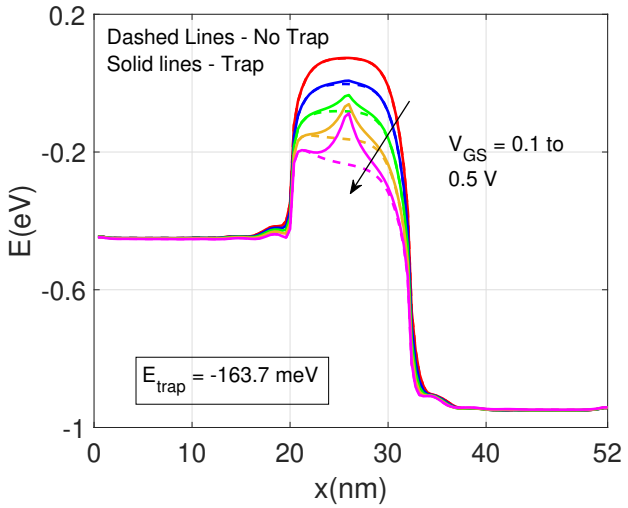

Figure 4.7: Conduction band (E_c) profile of MoS_2-FET at $V_{DS} = 0.5$ V along the transport direction for a single trap at $x_t = 26$ nm with $E_{trap} = -163.7$ meV for V_{GS} varying in the range of 0.1 to 0.5 V with 0.1 V steps.

4.7 and 4.8, respectively. Fig. 4.7 shows the E_c of MoS_2-FET for the no trap case and single trap located at $x_t = 26$ nm with $E_{trap} = -163.7$ meV, when V_{GS} is varied from 0.1 to 0.5 V. It is found that at low V_{GS}, the E_c in the channel region with the interface trap state exhibits negligible fluctuation compared to no trap case. This is because the trap states are not charged for $V_{GS} < 0.2$ V. As V_{GS} increases, the trap states begin to charge and effectively pin the E_c at the trap site. The trap states with $E_{trap} = -163.7$ meV considerably reduce the band profile modulation and cause a shift of around 149.2 meV at the trap site, compared to the no trap case for $V_{GS} = 0.5$ V.

Fig. 4.8(a) shows the E_c profile and the current spectra at the OFF-state for the different E_{trap} values. The current at the OFF-state is predominantly due to source-to-drain tunneling, which increases significantly as E_{trap} decreases toward $E_g/2$. This is because the interface states at the OFF-state offer a more favorable energy window for the band-to-band tunneling current. In practical devices, more interface trap states are expected to be present within the bandgap, which may have a broader energy window. This could worsen the ON-OFF current ratio in the MoS_2-FET [16], [88].

Fig. 4.8(b) illustrates the E_c profile and current spectra at ON-state for different E_{trap} values. It is observed that at the ON-state (for $V_{GS} > 0.4$ V), the current is majorly contributed to the thermionic component for both no trap and trap cases. The trap states do not contribute to tunneling current at high V_{GS} as their energy locations are within the conduction subbands. However, the trap states reduce the gate voltage efficiency by pinning the band profile, which decreases the contribution of the thermionic component. A substantially higher shift in E_c at the trap site is observed for $V_{GS} > 0.4$ V with the

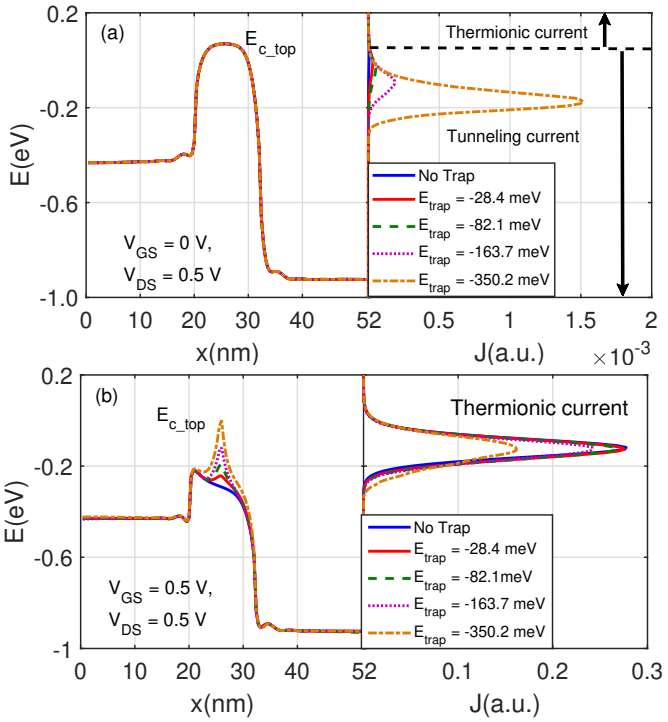

Figure 4.8: Impact of interface trap on the current components of MoS_2-FET for different E_{trap} at $V_{DS} = 0.5$ V: (left) E_c profile along transport direction and (right) the corresponding energy-resolved current spectra (J) at (a) $V_{GS} = 0$ V and (b) $V_{GS} = 0.5$ V.

considered trap cases, compared to the no trap case. In summary, the trap states close to the $E_g/2$ provide more favorable localized trap states for band-to-band tunneling current for low V_{GS} and more effective E_c pinning at the trap site for high V_{GS}. Therefore, trap states with an energy level close to the $E_g/2$ can significantly increase the OFF-state and degrade the ON-state currents of MoS_2-FET.

4.4.1 Impact of Interface Trap Location

To explore how the trap location affects the device performance, Fig. 4.9(a) shows the I_{DS}–V_{GS} characteristics of MoS_2-FET at $V_{DS} = 0.5$ V, when a single trap is placed at three different locations along the channel: the middle of the channel ($L_g/2$), near the source-channel end ($L_g/2 - 4$nm), and near the channel-drain end ($L_g/2 + 4$nm). It is observed that the OFF-state current degrades significantly when the trap is placed at the center of the channel in contrast to near the source and drain ends. This is explained by examining the E_c and current spectra for the different trap positions at the OFF-state, as displayed in Fig. 4.9(b). It is seen that the interface trap states located at the center of the channel result in a considerably higher source-to-drain leakage current compared to source and drain end. The presence of trap states in the middle of the channel provides the shortest tunneling path, which significantly enhances the phonon-assisted tunneling

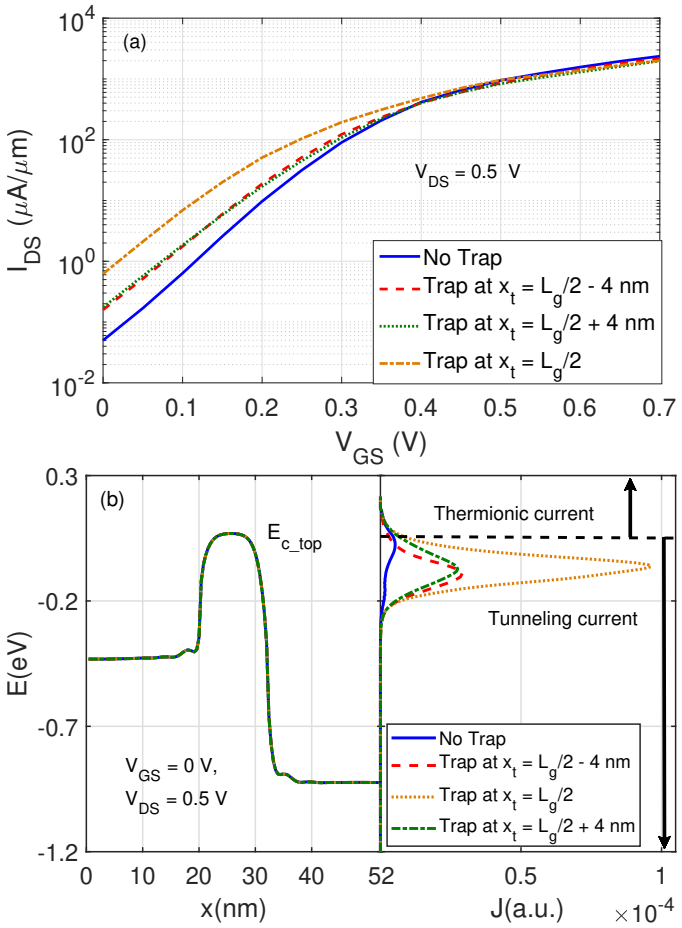

Figure 4.9: MoS_2-FET characteristics with trap site placed through the source end, middle of the channel, and the drain end of the channel: (a) I_{DS}–V_{GS} characteristics at V_{DS} = 0.5 V for a single trap at different x_t along the channel and $E_{trap} = -118.5$ meV, and (b) E_c profile and the corresponding energy-resolved current spectra (J) for the considered traps at $V_{GS} = 0$ V and $V_{DS} = 0.5$ V.

flux of the charge carriers. Thus, the location of the interface trap plays a critical role in inducing variability in device performance, making it imperative for designers to minimize the number of interface trap states present at the middle of the channel.

4.4.2 Effect of Single Interface Trap on Short Channel Performance Metrics

Fig. 4.10 shows the key short channel performance metrics of MoS_2-FET as a function of gate length (L_g) at $V_{DS} = 0.5$ V when a single trap is placed at the middle of the channel with varying E_{trap}. Here L_g is varied while keeping other device parameters, such as $L_{S/D}$, t_{ox}, and $N_{S/D}$, constant. Fig. 4.10(a) shows that the difference between trap and no trap current at the OFF-state significantly increases when the L_g decreases. This is attributed to enhanced trap-assisted source-to-drain tunneling with decreasing the channel potential barrier width. The trap states with $E_{trap} = -163.7$ meV result in around 2.75× increment in the OFF-state current for $L_g = 18$ nm compared to no trap value,

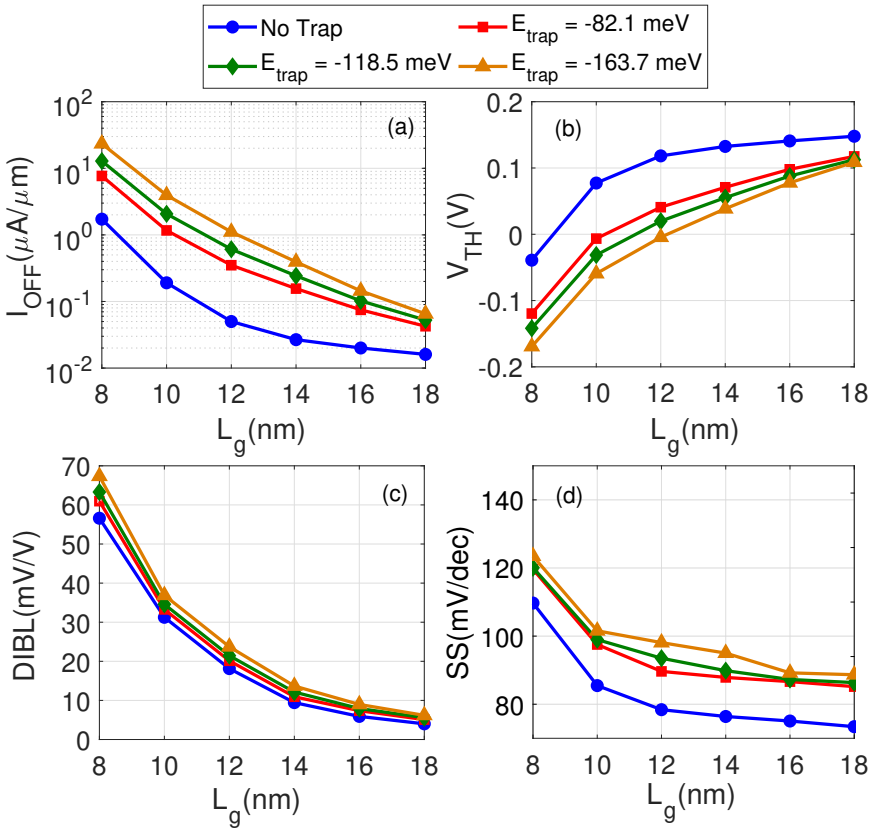

Figure 4.10: Short channel performance metrics of monolayer MoS_2-FET for a single trap at $x_t = 26$ nm with different E_{trap} at $V_{DS} = 0.5$ V: (a) OFF-state current (I_{OFF}), (b) V_{TH}, (c) DIBL, and (d) SS as a function of gate length (Lg). The OFF-state current is calculated at $V_{GS} = 0$ V and V_{TH} is determined using the constant current method at 1 μA/μm.

whereas the OFF-state current is enhanced by around 26.4× for $L_g = 8$ nm.

Fig. 4.10(b) shows that the V_{TH} of MoS_2-FET without interface trap states shifts considerably with decreasing L_g because of enhanced source-to-drain tunneling current. The interface traps further worsen the V_{TH} shifting due to an increment in the OFF-state current. Specifically, the interface trap with $E_{trap} = -163.7$ meV shifts the V_{TH} nearly by 0.25 V when L_g is scaled down from 16 nm to 8 nm. Interestingly, it is found that V_{TH} reduces considerably for L_g beyond 10 nm due to more pronounced short-channel effects. Thus, the scaling trend in I_{OFF} and V_{TH} suggests that reducing the lower energy traps close to $E_g/2$ is necessary to minimize the instability in the subthreshold characteristics of short-channel MoS_2-FET.

Fig. 4.10(c) illustrates the drain-induced barrier lowering (DIBL) as a function of L_g for different E_{trap}. The DIBL is determined by calculating the variation in V_{TH} between $V_{DS} = 0.05$ V and $V_{DS} = 0.5$ V and normalizing it by ΔV_{DS}. It is observed that the DIBL increases significantly with decreasing L_g. For $L_g = 12$ nm, the DIBL is approximately 18.21 mV/V, which is considerably lower than that of Si-based MOSFETs

[89]. This reduction is attributed to the single atomic thickness of MoS_2, which enhances the gate control over the channel region. The scaling trend in DIBL shows a marginal increment (around 1.2× for $E_{trap} = -163.7$ meV) in the presence of trap states close to $E_g/2$ compared to no trap case.

From Fig. 4.10(d), it is observed that the subthreshold swing (SS) deteriorates significantly compared to the no trap case for all the gate lengths, even in the presence of shallow trap states ($E_{trap} = -82.1$ meV). This is because a gradual charging of trap states with increasing V_{GS} reduces the gate control over the channel region. The variability induced by trap states in SS is also found to be significantly higher and enhanced with decreasing L_g. In summary, the 2-D MoS_2-FET is observed to be more susceptible to trap-induced variation in I_{OFF} and SS. For $L_g < 12$ nm, interface trap states close to $E_g/2$ lead to a significant enhancement in I_{OFF}, V_{TH}, and SS.

4.4.3 Effect of Single Trap on Temperature Dependency

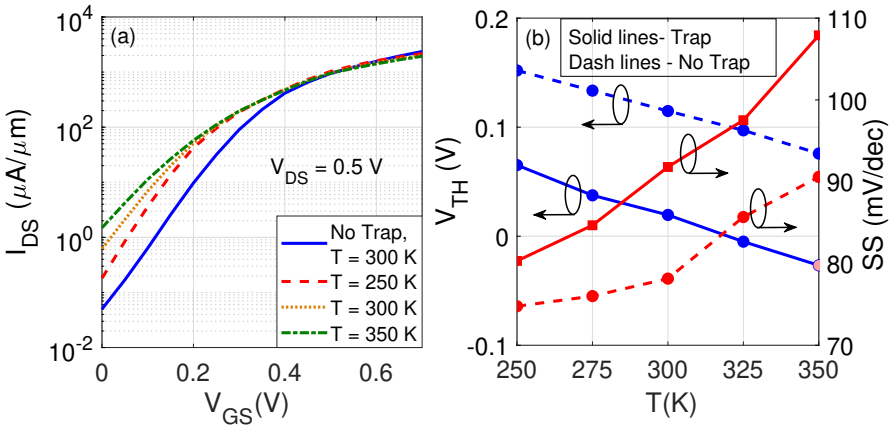

Figure 4.11: Temperature dependency on I_{DS}–V_{GS} characteristics of MoS_2-FET in the presence of single trap at $x_t = 26$ nm with $E_{trap} = -118.5$ meV: (a) I_{DS}–V_{GS} characteristics, and (b) V_{TH} and SS for the different device operating temperatures (T) at $V_{DS} = 0.5$ V.

Fig. 4.11(a) shows the I_{DS}–V_{GS} characteristics of MoS_2-FET for the different device operating temperatures when a single trap is placed at $x_t = 26$ nm with $E_{trap} = -118.5$ meV. It is observed that the current at low V_{GS} shows a significantly higher increment with rising temperature when trap states are present. This is because the inelastic phonon scattering highly depends on temperature through the Bose-Einstein statistics. Consequently, the source-to-drain tunneling current assisted by inelastic phonon increases with increasing the device operating temperature. On the other hand, the ON-state current at high V_{GS} shows a marginal reduction with increasing temperature. This is because the inelastic phonon scattering causes more charge carriers to backscatter, which results in a

marginal reduction in the thermionic current.

Fig. 4.11(b) shows V_{TH} and SS as a function of the device operating temperature for no trap and a single trap at $x_t = 26$ nm with $E_{trap} = -118.5$ meV for the $V_{DS} = 0.5$ V. The V_{TH} in the presence of the interface trap decreases by approximately 1.5 mV/K compared to around 1.1 mV/K for the no trap case. The SS for the $E_{trap} = -118.5$ meV degrades significantly from nearly 91.8 mV/dec at 300 K to 107.9 mV/dec at 350 K. In contrast, the SS for no trap case increases moderately from 78.15 at 300 K to 90.59 mV/dec at 350 K. This enhancement of SS dependency on temperature is due to the phonon-assisted tunneling current. It is found that this approach captures the essential I_{DS} temperature dependency as observed in the fabricated 2DM-FETs [90].

4.4.4 Impact of Multiple Interface Traps

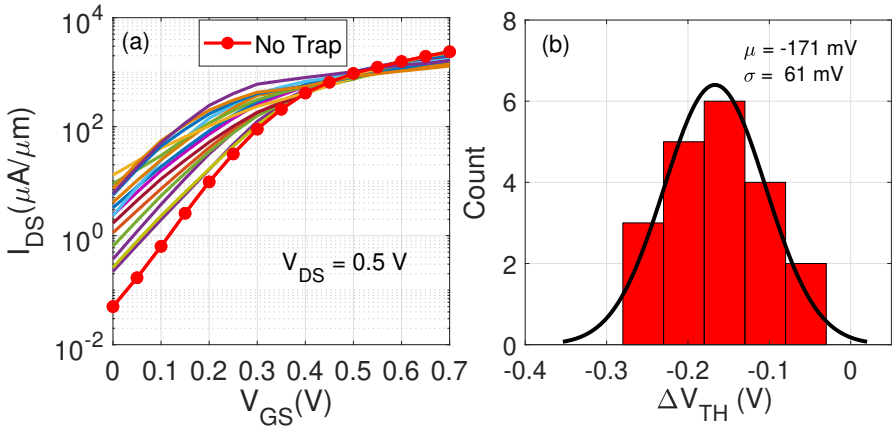

Figure 4.12: I_{DS}–V_{GS} characteristics and (b) ΔV_{TH} variability of MoS_2-FET for 20 random distributions of multiple traps within the channel region at $V_{DS} = 0.5$ V for L_g =12 nm. The areal density D_T of around 2.7×10^{11} cm^{-2} to 1.9×10^{12} cm^{-2} is achieved by varying the trap number in the range of around 2 to 8. Further, E_{trap} is also tailored from the range of -54.9 meV to -118.5 meV. The ΔV_{TH} is calculated as $(V_{TH,trap} - V_{TH,no-trap})$.

Fig. 4.12(a) and 4.12(b) show the I_{DS}–V_{GS} characteristics and threshold voltage variation between trap and no trap case (ΔV_{TH}), respectively for around 20 realizations of randomly distributed multiple traps with E_{trap} in the range of -54.9 meV to -118.5 meV. The trap numbers are in the range of 2 to 8, which corresponds to the aerial trap density (D_T) of around 2.7×10^{11} cm^{-2} to 1.9×10^{12} cm^{-2}. It is illustrated that the presence of multiple trap states could significantly affect the subthreshold current. The largest I_{OFF} degradation is observed around 1.4 μA/μm to 46.2 μA/μm when the multiple trap states with energies toward $E_g/2$ are present. It is observed from Fig. 4.12(b) that the variability distribution of ΔV_{TH} follows a normal distribution with the mean of around $\mu = -171$ mV and standard deviation of around $\sigma = 61$ mV. The normal distribution indicates that

the interface trap-induced V_{TH} variability significantly affects the I–V characteristics of MoS_2-FET.

It is also found in Fig. 4.12(a) that the presence of multiple trap states causes a significant reduction in I_{ON} than the single trap case. The reason for this behavior is that multiple trap states cause a considerably higher charge trapping, which leads to a considerable decrement in the inversion charge density. A high D_T (the worst case in Fig. 4.12) results in a larger variation in both I_{OFF} and I_{ON}, resulting in a lower ON-OFF current ratio (around 42.19). Most fabricated MoS_2-FETs also require a high V_{GS} window to achieve a significant ON-OFF current ratio [91, 92, 93]. This could be due to the high density of interface trap states, which should be examined closely to scale down the operating voltage window.

4.5 Discussions

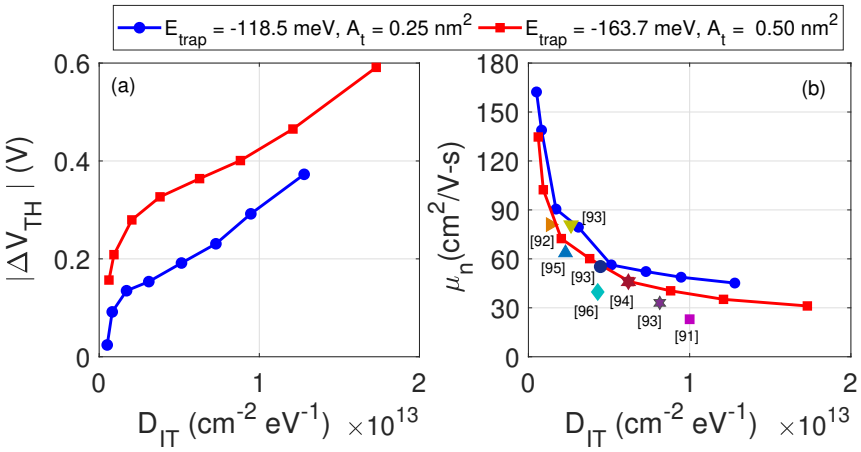

Figure 4.13: $|\Delta V_{TH}|$ and low field electron mobility (μ_n) of MoS_2-FET with respect to the interface trap density (D_{IT}) for $E_{trap} = -118.5$ meV, $A_t = 0.25$ m^2, and $E_{trap} = -163.7$ meV, $A_t = 0.50$ m^2. The low field mobility (μ_n) values are calculated from I_{DS}–V_{GS} characteristics using dR/dL method [93] and are benchmarked with experimentally reported mobility values for the different D_{IT} [91, 92, 93, 94, 95, 96].

After understanding the impact of interface traps on the I_{DS}–V_{GS} characteristics of MoS_2-FET, it is important to evaluate the accuracy of the theoretical model by validating it with experimental results. Fig. 4.13(a) shows the variation of the threshold voltage $|\Delta V_{TH}|$ between trap and no trap cases of MoS_2-FET as a function of interface trap density (D_{IT}) for the $E_{trap} = -118.5$ meV and $E_{trap} = -163.7$ meV. It is observed that $|\Delta V_{TH}|$ is increased by around 0.3 V in the presence of the trap density of around $D_{IT} = 1\times10^{13}$ cm^{2}eV^{-1} and $E_{trap} = -118.5$ meV. The $|\Delta V_{TH}|$ is found to increase further with increasing the trap area and trap energy toward the $E_g/2$. However, the matching of $|\Delta V_{TH}|$ with experimental data is only qualitative due to the significant difference between

simulated and fabricated long-channel MoS_2-FET with Schottky contacts.

Fig. 4.13(b) shows the low-field electron mobility (μ_n) of MoS_2-FET as a function of D_{IT} for the $E_{trap} = -118.5$ meV and $E_{trap} = -163.7$ meV. The μ_n values, which are computed using the dR/dL method [93] from I–V characteristics, are found to be nearly independent of L_g [63] and could be verified with recently reported experimental results. It is observed that μ_n of MoS_2-FET degrades by about six times when the trap density of around $D_{IT} = 1{\times}10^{13}$ cm^2eV^{-1} is present. The reported μ_n in this work for different trap energies is found to match well with experimental data for varying trap densities [92, 93, 94]. However, some experimental findings [91, 95, 96] exhibit a slight variance from the theoretical value of μ_n, possibly due to lower acceptor-type interface trap states from E_c and smaller trap cross-sectional area in the simulation. The model accurately captures essential physical aspects and demonstrates plausible behavior with experimental reported μ_n results. However, a density functional theory simulation can be further used to explore the detailed insights into the behavior of individual defect or trap states in MoS_2-FET.

It is found that the trapping of charge carriers at the interface trap states can significantly decrease the carrier mobility and increase the V_{TH}, leading to worsening device performance. Therefore, it is crucial to minimize the density of interface trap charges and develop strategies to mitigate their impact on device performance in MoS_2-FET. Based on the findings of this work, it is suggested to adopt the following design strategies to minimize interface trap effects in MoS_2-FETs: (i) the sulfur vacancy defect located in the middle of the MoS_2 channel plays a critical role in causing variability in device performance, which can be reduced through hydrogen passivation [97], and (ii) a larger-area of interface traps generated by the di-sulfur defects can cause significantly higher degradation in the performance of MoS_2-FETs. The formation of di-sulfur vacancy defects can be minimized by using high-pressure sulfur or selenium annealing [98]. Additionally, treating monolayer MoS_2 with a non-oxidizing organic superacid can also reduce di-sulfur vacancy defects [99].

4.6 Summary

Using a dissipated quantum transport modeling framework, a systematic investigation is performed to find the impact of interface traps on the I–V characteristics of MoS_2-FET by considering various trap energy levels and positions along the channel. Additionally, the degradation of low field electron mobility (μ_n) and threshold voltage

(V_{TH}) with increasing interface trap density is explained, and verified the mobility results with experimental data. The results have shown that the trap-induced inelastic tunneling current strongly affects I_{OFF}, V_{TH}, and SS for sub-18 nm gate length, while charge trapping marginally reduces I_{ON} of MoS_2-FET. By controlling the trap position and reducing the interface trap density close to the $E_g/2$, the variability in $I_{DS} - V_{GS}$ characteristics and temperature dependency can be reduced significantly. Further, a high aerial density trap could lead to a more significant degradation in both the OFF-state and ON-state currents, resulting in a lower ON-OFF current ratio. The proposed model and observations will provide valuable insights to optimize the interface trap effect in 2DM-FETs and could be helpful in expanding their application in memory and neuromorphic computing.

Chapter 5

3-D MOSFET with Single-Layer and Bi-Layer MoS_2

5.1 Introduction

Silicon (Si)-based gate-all-around (GAA) stacked nanosheet field-effect transistor (NS-FET) has been proposed to scale down the device dimension beyond the 2 nm technology node (N2) as they offer superior current drivability at the same area footprint over their FinFET counterpart [100]. However, enhanced surface roughness and quantum confinement effects with scaling down the technology node are severely degrading their switching benefits [25, 101]. To continue advancing the technology node, 2DMs, such as MoS_2, WSe_2, InSe, etc., are emerged as the most viable candidates with atomically thin structures and surfaces free of dangling bonds [12]. Among more than 1800 discovered 2DMs, MoS_2 demonstrates a higher readiness level of ultra-scale MOSFET due to considerable progress in easy and large-scale synthesis techniques with carrier mobility comparable to silicon [42, 102]. More interestingly, the recent achievement of excellent switching performance down to the ultimate scaling limit of 1 nm gate length [19] provides a new pathway to develop MoS_2-FET for attaining the next level of computing performance and energy efficiency. Early theoretical and experimental works on MoS_2-FET have mainly focused on the single gate structure [12, 63], with limited attention given to stacked multigate architectures. Recently, experimental efforts have demonstrated the performance potential of MoS_2 with the 2-layer and 3-layer stacked NS-FET for the gate length of around 370 nm [24] and 540 nm [25], respectively. More recently, Chung *et al.* has demonstrated the process feasibility of GAA nanosheet stacked with MoS_2 channel [26]. Their device has shown an excellent ON-current of 0.4 mA/μm with nearly zero drain-induced barrier lowering for the 40 nm gate length.

Despite 3-D integration of MoS_2 nanosheets promises scaling and switching advantages over a single channel, there are many questions that need to be answered before embarking on an aggressive pursuit of miniaturization: (i) What is the maximum achievable performance limit through the stacking of MoS_2 nanosheets; (ii) What are their performance benefits over existing Si NS-FET?; (iii) How do the switching advantages scale with technology node?; and (iv) What is the performance difference between

experimentally adopted Schottky barrier (SB)-type contact and CMOS-compatible doped-type contacts with MoS_2 NS-FETs?. In this chapter, an attempt is made to address these questions by investigating the short-channel performance metrics of SL- and BL-MoS_2 NS-FETs, and uniformly benchmarking their performance with Si NS-FET for sub-5 nm technology nodes.

This chapter presents a comprehensive performance analysis of SL- and BL-MoS_2 NS-FETs in CMOS-compatible architecture using fully experimental calibrated 3-D TCAD simulation, based on self-consistent solutions of the drift-diffusion, continuity, and Poisson's equations. This chapter shows that the integration of 2-D MoS_2 nanosheet into stacked 3-D NS-FET presents a promising avenue for scaling the device dimension beyond Moore's law.

5.2 Simulation Technique

5.2.1 Material Attributes for the TCAD Simulation

Table 5.1: Calibrated SL- and BL-MoS_2, and Initial Si Material Parameters for TCAD Modeling.

Parameter	**SL-MoS_2**	**BL-MoS_2**	**Si**
Thickness [t_{ch} (nm)]	0.65	1.38	5
Effective mass [m_x, m_y (m_0)]	0.57, 0.57	0.51, 0.51	0.19, 0.91
Bandgap [E_g (eV)]	1.80	1.60	1.11
Low-field mobility [μ_e (cm^2/V-s)]	34.5	50.75	1268
Dielectric constant [ϵ_r]	4.8	6.9	11.7
Effective Density-of-states [eDOS (cm^{-3})]	1×10^{19}	4×10^{18}	2.8×10^{19}

Mobility and other parameters of Si in TCAD simulation are further updated after including device models.

Table 5.1 lists key material attributes of SL-MoS_2 and BL-MoS_2, which are used to achieve a precise depiction in the TCAD tool. These parameters are obtained by performing DFT simulation [103]. However, to calibrate the TCAD simulations with experimental and NEGF-based simulations, the low-field electron mobility (μ_e) and the effective density-of-states (eDOS) are utilized as fitting parameters. From the data presented in Table 5.1, it can be inferred that the μ_e for BL-MoS_2 is approximately 1.7× higher than that of SL-MoS_2. These selected μ_e values align well with experimental data [104] and findings from simulation studies [105]. Furthermore, the material properties of silicon (Si) are defined in Table 5.1, with values sourced from the definitions within the TCAD tool.

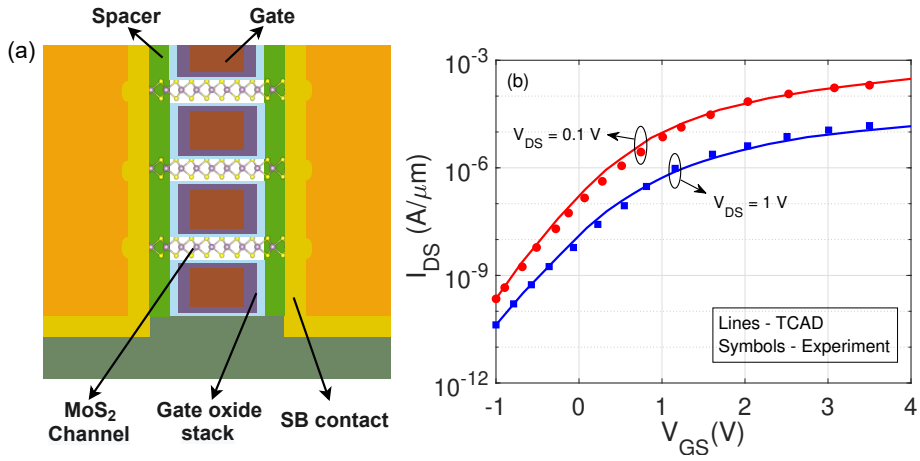

Figure 5.1: Experimental verification of simulation technique: (a) Simulated device geometry, and (b) transfer characteristics of three-channel stacked SL-MoS_2 NS-FET with SB-type contact from the 3-D TCAD simulation and experimental results [26] at V_{DS} = 0.1 V and V_{DS} = 1 V at 40 nm gate length.

5.2.2 Setup and Calibration of TCAD Simulation

A more rigorous 3-D Sentaurus Structure Editor (SDE) TCAD simulation is employed to accurately describe electronic transports in NS-FETs with high computational efficiency and adaptability while maintaining accuracy [106]. The TCAD simulation involves self-consistent solutions of drift-diffusion, continuity, and Poisson's equations combined with mobility and quantum correction terms for describing short-channel device physics [89]. In particular, Lombardi, and inversion and accumulation layer mobility models are used to incorporate the mobility degradation caused by the transverse field at the interface, and Coulomb and remote phonon scatterings, respectively. Furthermore, carrier generation-recombination and band-to-band tunneling are included using the Shockley-Read-Hall and Hurkx models, respectively.

To validate the accuracy of the modeling approach with experiments, a three-channel stacked SL-MoS_2 NS-FET is designed with gold (Au) metal serving as the source and drain regions, as depicted in Fig. 5.1. Here, the considered device geometry is identical to the experimental reported geometry with a gate length of around 40 nm [26]. Fig. 5.1 shows the transfer characteristics of three-channel stacked SL-MoS_2 NS-FET using the developed simulation approach and the experimental reported results [26]. To match the experimental results, the TCAD simulation is required to incorporate non-idealities parameters over the materials attributes that include Schottky-barrier height (Φ_{BH}) of approximately 0.276 eV for the MoS_2-gold contact, an interface trap charge density of $1{\times}10^{12}$ cm^{-2} at the oxide/channel interface, and source and drain resistances of approximately 100 $\Omega - \mu m$. It is observed that the transfer characteristics for both low

V_{DS} and high V_{DS} are in good agreement with experimental results. This proves that the developed modeling approach accurately captures the material aspects and device aspects of MoS_2 NS-FETs. Moreover, the simulation model for Si NS-FET is validated by benchmarking with experimental results, as performed in the previous work [89].

5.2.3 Dissipative Quantum Mechanical Simulation for Validation of Doped-type Contact MoS_2-FET

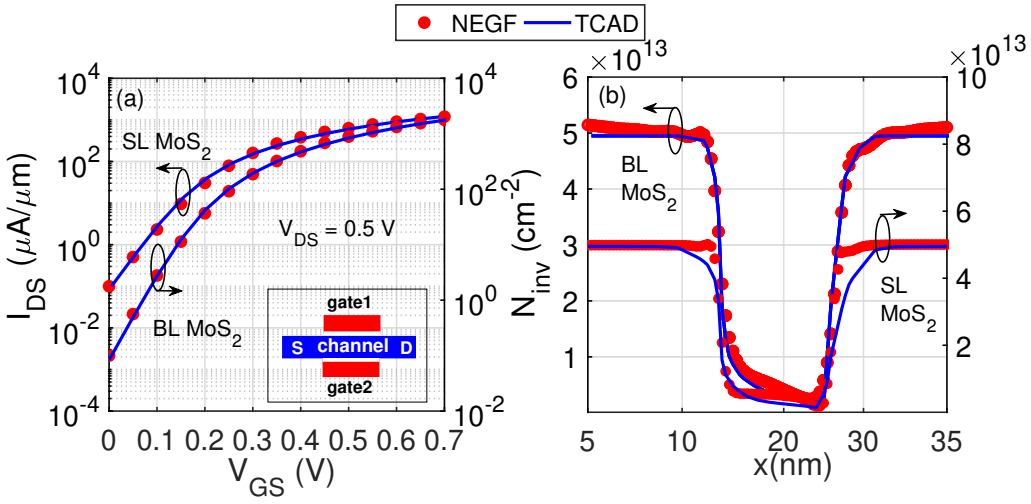

Figure 5.2: Verification of Modeling Approach for MoS_2-FETs with Doped-Type Contacts: (a) Transfer characteristics and (b) inversion charge density (N_{inv}) of SL- and BL-MoS_2-FETs in a double-gate configuration (shown in the inset) from the 3-D TCAD and dissipative NEGF simulations at $V_{DS} = 0.5$ V for the 1 nm technology node (N1).

The major focus of this chapter is to find the ultimate performance limit of MoS_2 in CMOS-compatible device architecture with doped-type source and drain contacts. To validate the accuracy of the transport models for doped-type contact MoS_2 NS-FETs, a self-developed atomistic simulation approach is utilized that relies on self-consistent solutions of dissipative Non-Equilibrium Green's Function (NEGF) and Poisson's equation. A comprehensive description of the simulation methodology can be found in chapter 4.

Fig. 5.2(a) and (b) illustrate the transfer characteristics and inversion charge density (N_{inv}), respectively, of SL- and BL-MoS_2 using TCAD simulation and NEGF-Poisson solver at $V_{DS} = 0.5$ V. In this simulation, a double gate (DG) MoS_2-FET is employed at 1 nm technology node (N1). The comparison reveals that the transfer characteristics and N_{inv} from the TCAD simulation closely align with the outcomes of the dissipative NEGF simulation. This shows that the simulation model accurately captures material and short channel transport properties of MoS_2-FET.

5.3 Performance of Doped-type Contact NS-FETs

5.3.1 3-D MOSFET Device Geometry

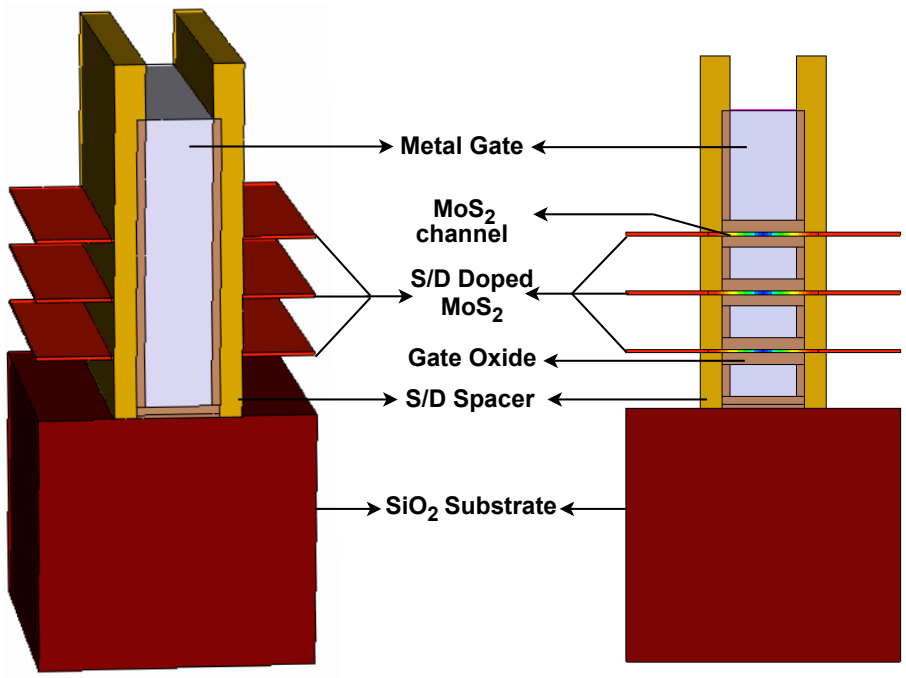

Figure 5.3: Simulated device geometry with doped source and drain contacts: (a) 3-D schematic and (b) cross-sectional view of the simulated three-channel stacked SL- and BL-MoS_2 NS-FET.

Fig. 5.3 shows the schematic of three-channel stacked SL-MoS_2 NS-FET with doped-type contacts, where the device design parameters are selected from the IRDS 2021 projection for the 1 nm technology node (N1) [13]. The channel region consists of a large-area MoS_2 nanosheet with a length of 12 nm, while the source (S) and drain (D) regions are assumed to be n-type doped MoS_2 with the molar fraction of $f_S = f_D = 2 \times 10^{-2}$. A uniform gate oxide with an equivalent oxide thickness (EOT) of around 0.9 nm is employed to cover the MoS_2 nanosheet. To ensure uniform benchmarking, the Si NS-FET (crystal orientation [100]) is designed with nearly identical geometry to that of MoS_2 NS-FET, except that the thickness of sheet is taken around 5 nm. Here, Si nanosheet with various widths are considered because their performance is found to rely heavily on the nanosheet width [89].

5.3.2 Current Characteristics and Performance Metrics

Fig. 5.4(a) shows the transfer characteristics of three-channel stacked SL-MoS_2, BL-MoS_2, and Si NS-FETs with various width (W= 10, 50, 100, 200, and 500 nm) at V_{DS} = 0.7 V. These characteristics are acquired by maintaining a fixed OFF-current

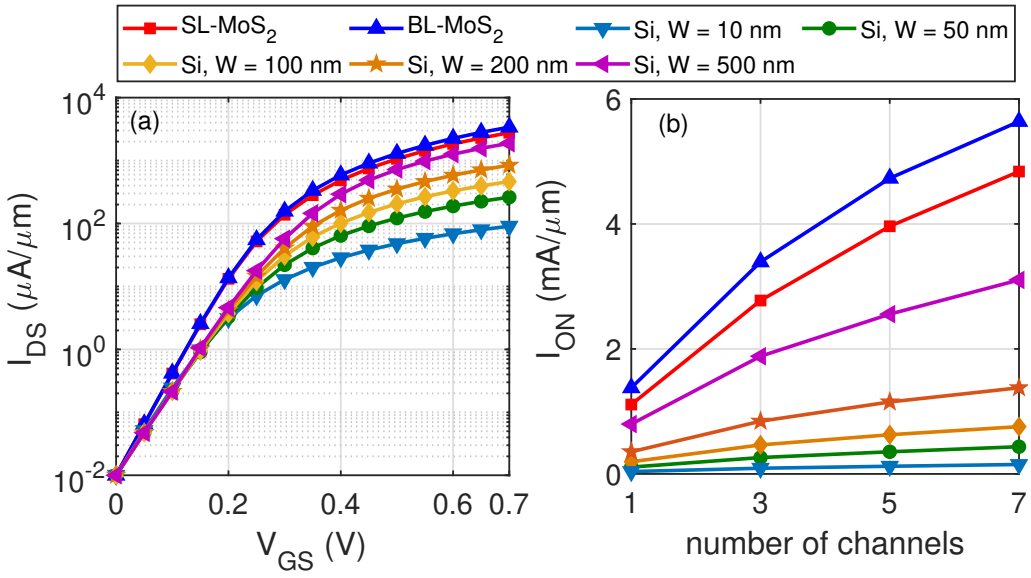

Figure 5.4: (a) Transfer characteristics of three-channel stacked SL-MoS_2, BL-MoS_2, and various width Si nanosheet (W= 10, 50, 100, 200, and 500 nm) NS-FETs at V_{DS} = 0.7 V, and (b) ON-current as a function of the number of channels for N1 node.

$[I_{OFF} = I_{DS}\,(V_{GS} = 0\,V$ and $V_{DS} = 0.7\,V)]$ of approximately 10 nA/μm through the adjustment of the gate-metal work function difference. It is observed that SL- and BL-MoS_2 NS-FETs offer superior drive currents over Si NS-FETs with W < 500 nm. The reasons for superior drive current with MoS_2 channel are threefold: (i) an atomically thin channel provides excellent gate control, (ii) a large effective mass of MoS_2 sheets significantly suppresses the OFF-state current due to reduced source-to-drain tunneling, and (iii) a higher transverse effective mass allows considerably higher contribution of thermionic current. The 2021 IRDS specification projects the ON-current $[I_{ON} = I_{DS}\,(V_{GS} = V_{DS} = 0.7V)]$ at approximately 1 mA/μm for the N1 node, which can be readily achieved by both SL- and BL-MoS_2 NS-FETs. Further, Si NS-FET requires a width greater than 200 nm for achieving the I_{ON} of nearly 1 mA/μm. However, achieving the Si nanosheet with a width exceeding 100 nm could pose challenges, as the presence of stress could cause significant deformation of nanosheets [107].

It is evident from Fig. 5.4 that the subthreshold swing (SS) of the Si NS-FET increases from 68.34 mV/dec to 73.45 mV/dec when the width is scaled from 10 to 50 nm. This trend is attributed to a wider channel reducing the electrostatic control over the channel region due to an increment in the drain-induced barrier lowering. In contrast, the performance modulation in the OFF characteristics becomes marginal as the sheet width increases beyond 50 nm. Consequently, the SS exhibits a slight increment from 73.45 mV/dec to 74.81 mV/dec as the width increases from 100 nm to 500 nm.

Fig. 5.4(b) displays the I_{ON} of three-channel stacked SL-MoS_2, BL-MoS_2, and Si NS-FETs as a function of the number of channels for the N1 node. It is observed that the I_{ON} of SL-MoS_2, BL-MoS_2, and various width (W= 10, 50, 100, 200, and 500 nm) Si NS-FETs exhibits a considerable increment with the number of channels stacked due to increment in the conducting paths. Importantly, BL-MoS_2 NS-FET demonstrates an approximately 1.25× higher I_{ON} compared to SL-MoS_2 NS-FET because of marginally higher low-field electron mobility and eDOS (as shown in Table 5.1). As the number of channel stacks increases from one to seven, SL- and BL-MoS_2 NS-FETs experience around 4.1× and 4.3× improvement in I_{ON}, respectively, while various width Si NS-FETs show nearly identical increment with approximately 3.9×. Further, the enhancement in I_{ON} with the number of channels is found to be not constant, primarily due to a decreasing reduction rate of contact resistances with increasing the number of channels [108]. Thus, BL-MoS_2 NS-FET is found to be a more compelling candidate for achieving a more effective enhancement in I_{ON} through multichannel stacking.

5.3.3 Impact of Equivalent Oxide Thickness Scaling

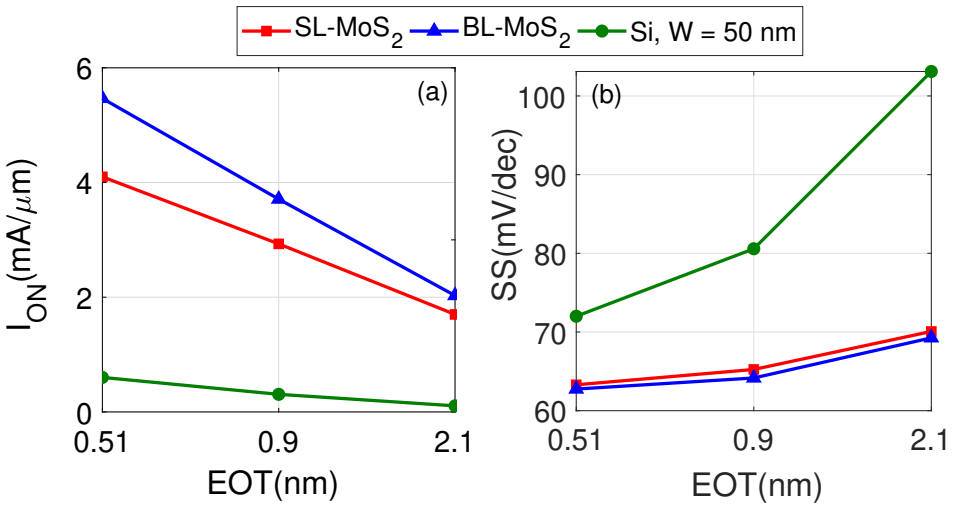

Figure 5.5: Effect of equivalent oxide thickness (EOT): (a) I_{ON} and (b) SS of three-channel stacked SL-MoS_2, BL-MoS_2, and 50 nm wide Si NS-FETs as a function of the EOT, at V_{DS} = 0.7 V.

Now the scaling behavior of the EOT is studied for SL-MoS_2, BL-MoS_2, and Si NS-FETs for the N1 node. Fig. 5.5(a) and (b) show the I_{ON} and SS of three-channel stacked SL-MoS_2, BL-MoS_2, and 50 nm wide Si NS-FETs for the different EOT. A smaller EOT value appears to have a positive effect on the OFF and ON-states of the device with a significant increment in the I_{ON} and decrement in the SS. This is due to the enhancement of the gate modulation efficiency. The I_{ON} of SL- and BL-MoS_2 NS-FETs is found to enhance

by approximately 2.4× and 2.7×, respectively, while 50 nm wide Si NS-FET shows much larger improvement in I_{ON} with around 5.5× enhancement as EOT scales down from 2.1 nm to 0.51 nm. It is found that SS of SL- and BL-MoS_2 NS-FETs decreases by around 10.6%, whereas Si NS-FET shows a considerably high decrement of around 41.5% with scaling down the EOT from 2.1 nm to 0.51 nm. This is because the atomic thick MoS_2 channel offers superior gate control over the channel region, which exhibits a relatively modest improvement in electrostatic control compared to Si NS-FETs. Therefore, scaling down the EOT can be a promising strategy to achieve high performance in both 2-D MoS_2 and Si NS-FETs.

5.3.4 Impact of Technology Node Scaling

Fig. 5.6 shows the short channel performance metrics of SL-MoS_2, BL-MoS_2, and Si NS-FETs as a function of the technology node at the fixed OFF-state current of around 10 nA/μm. Table 5.2 shows the key device design parameters, which are scaled proportionally with the technology node, while keeping other parameters constant. It is observed from Fig. 5.6(a) that SL- and BL-MoS_2 NS-FETs experience only a marginal increment in SS as the technology node scales down beyond N5 node. Conversely, Si NS-FETs with 50 nm and 500 nm widths exhibit a more gradual SS increment. Specifically, at the N1 node, the SS for SL-MoS_2 and BL-MoS_2 NS-FETs is observed to be approximately 64.18 mV/dec and 63.85 mV/dec, respectively, closely approaching the theoretically minimum achievable limit. Comparatively, 50 nm and 500 nm wide Si NS-FETs demonstrate a 1.23× higher SS (79.17 mV/dec). Moreover, at ultra-scaled N0.5 node, the SS of 50 nm wide Si NS-FET is observed around 97.48 mV/dec, which is found to be around 1.45× higher than that for BL-MoS_2 NS-FET. The reason for better SS with MoS_2 NS-FETs is that a larger mass effectively suppresses the contribution of source-to-drain tunneling current at OFF-state. The scaling trend in SS suggests that BL-MoS_2 NS-FET might be better suited for low-voltage operation at ultra-scale gate length.

Table 5.2: Classification of Technology Nodes with Corresponding Gate Lengths (L_g) and Spacer Thicknesses (t_{sp}) According to Roadmap by IRDS 2021 (N1-N5)[13] and ITRS 2013 (N0.5-N0.7) [109].

Technology Node (TN)	**N0.5**	**N0.7**	**N1**	**N2**	**N3**	**N5**
Gate length [L_g (nm)]	8	10	12	14	16	18
Spacer thickness [t_{sp} (nm)]	1	1.2	1.4	1.6	1.8	2

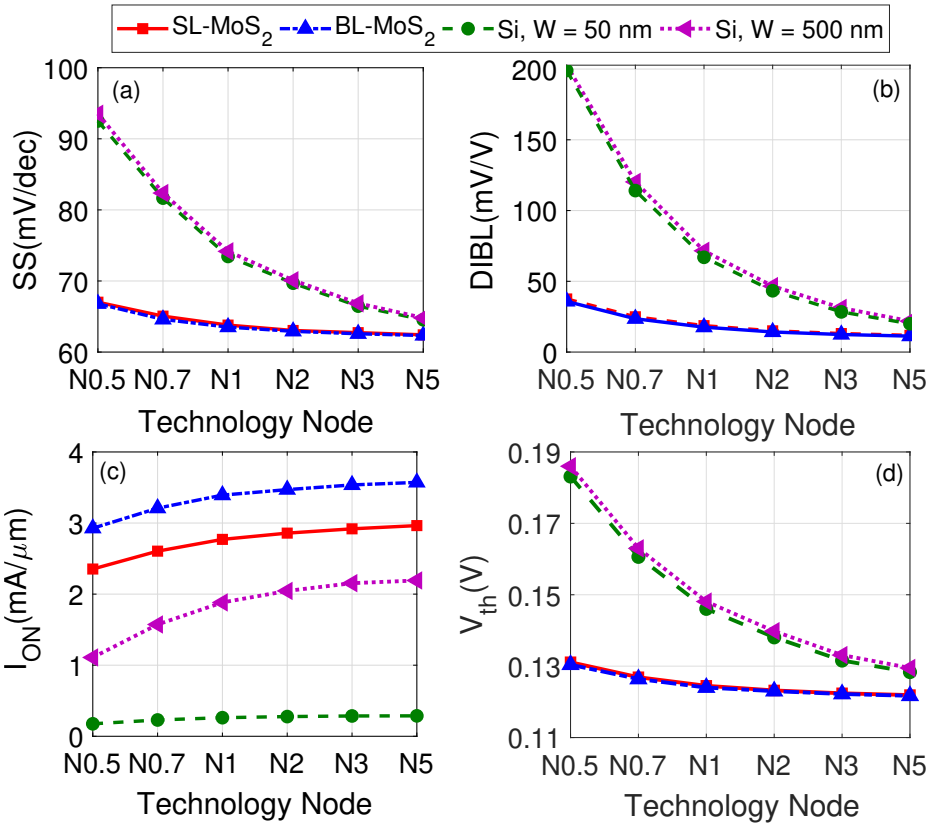

Figure 5.6: Key short channel performance metrics of SL-MoS_2, BL-MoS_2, and Si NS-FETs (W = 50 and 500 nm) at V_{DS} = 0.7 V.: (a) Subthreshold swing (SS), (b) drain-induced barrier lowering (DIBL) (c) I_{ON}, and (d) V_{TH} as a function of technology node (N). The device specifications for the N0.7 and N0.5 nodes are designed from the 2013 ITRS projection [109], while other nodes are considered from the 2021 IRDS projection [13].

In Fig. 5.6(b), it is evident that DIBL of the 50 nm wide Si NS-FET exhibits a nearly 9.29× increment with around 21.8 mV/V to 202.7 mV/V as the technology node is scaled from N5 to N0.5 node. Compared to Si NS-FET, DIBL of SL- and BL-MoS_2 NS-FETs shows a marginal increment with around 3.18× and 3.15×, respectively. This underscores the exceptional electrostatic control achieved in atomically thin MoS_2 channels. Fig. 5.6(c) shows that I_{ON} of SL- and BL-MoS_2 NS-FETs show marginal decrement with around 0.79× and 0.84×, respectively, as the technology node scales down from N5 to N0.5. However, 50 nm and 500 nm wide Si NS-FETs experience a significant reduction in I_{ON}, with values decreasing by around 0.61× and 0.51×, respectively. This notable decrement in I_{ON} for Si NS-FETs is attributed to the substantial increase in DIBL at lower technology nodes, as observed in Fig. 5.6(b). Consequently, Si NS-FETs require a much more negative V_{GS} to achieve the same OFF-state.

Fig. 5.6(d) shows the variation in threshold voltage (V_{th}) as a function of the technology node. The V_{th} here is determined using the constant current method at a

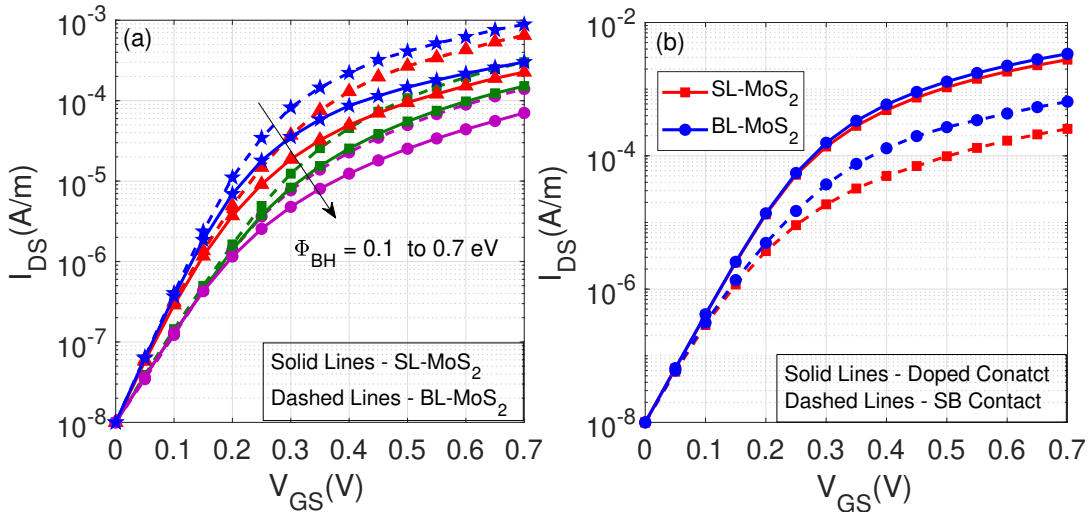

Figure 5.7: Effect of SB-type and doped-type contacts: Transfer characteristics of (a) SL- and BL-MoS_2 SB-type contact NS-FETs with varying Schottky-barrier height (Φ_{BH}), and (b) doped-type contact and SB-type contact ($\Phi_{BH} = 0.276$ eV) SL- and BL-MoS_2 NS-FET for N1 node at $V_{DS} = 0.7$ V.

current density of around 1 μA/μm. The V_{th} of the NS-FETs shows an increasing trend with scaling down the technology node. The V_{th} of SL- and BL-MoS_2 NS-FETs is observed to increase marginally by about 1.08× as the technology nodes scales from N5 to N0.5. In contrast, for Si NS-FET, V_{th} of 50 nm wide Si NS-FET shows a significant increment of around 1.43× with scaling down the technology node from N5 to N0.5. Therefore, SL- and BL-MoS_2 NS-FETs has been found to maintain the performance advantages even at extremely scale technology node. On the other hand, Si NS-FETs demonstrate pronounced degradation in short-channel performance metrics due to their larger sheet thickness and lower transport effective mass.

5.4 Comparison of Doped-Type Vs. Schottky-Type Contacts

Since most of the reported experimental works on multichannel stacked MoS_2 NS-FET have utilized SB-type S/D contacts [24, 25, 26], it becomes vital to find the difference in performance between doped-type contact and SB-type contact MoS_2 NS-FETs. Here only the S/D contact is modified with different metal work functions by keeping other parameters the same for uniform performance benchmarking. Fig 5.7(a) shows the transfer characteristics of SL- and BL-MoS_2 NS-FETs with SB-type S and D contacts, as a function of barrier height (Φ_{BH}) at the fixed I_{OFF} = 10 nA/μm. It is observed that the drive current of both SL- and BL-MoS_2 NS-FETs decreases significantly with increasing the SB height. This is because the broadening of source-channel potential

barrier width reduces the band-to-band tunneling current component. Additionally, the SS of both devices is found to deteriorate severely with increasing the Φ_{BH} due to the ambipolar transport near the OFF-state region of the current characteristics.

Fig. 5.7(b) displays the transfer characteristics of three-channel stacked SL- and BL-MoS_2 NS-FETs with both SB-type and doped-type contacts for the N1 node. It is evident that SL- and BL-MoS_2 NS-FETs with SB-type contacts exhibit inferior I_{ON}, which is approximately 0.12× and 0.19× smaller compared to doped-type contact NS-FETs. Furthermore, the SS of SL- and BL-MoS_2 NS-FETs with SB-type contacts is higher, exhibiting approximately 1.1× and 1.14× greater than that of their counterparts with doped-type contacts. Therefore, SL- and BL-MoS_2 NS-FETs with doped-type contacts are expected to offer a promising solution for achieving high I_{ON} and low SS.

5.5 Power Versus Frequency Characteristics of SL and BL MoS_2-based CMOS Inverters

Fig. 5.8 presents the power versus frequency characteristics of CMOS inverters based on SL-MoS_2, BL-MoS_2, and Si nanosheets with widths of 50 nm and 500 nm for the 1 nm technology node at a fixed I_{OFF} of 10 nA/μm. Among the Si nanosheet-based inverters with varying widths, it is evident that devices with higher I_{ON} exhibit higher frequency but also consume more power at the same supply voltage (V_{DD}). At V_{DD} = 0.7 V, the 500 nm wide Si nanosheet-based inverter shows 1.46× higher frequency while consuming 2.7× higher power as compared to 50 nm wide Si nanosheet-based inverter. However, 50 nm wide Si nanosheet-based inverter shows higher frequency at iso-power and lower power consumption at iso-frequency when compared to 500 nm wide Si nanosheet-based inverter.

The inverters based on SL- and BL-MoS_2 do not conform to the power-frequency trend observed among Si nanosheets of varying widths. In comparison to 500 nm wide Si nanosheet-based inverters, SL- and BL-MoS_2 nanosheet-based inverters demonstrate significantly lower power consumption at iso-frequency and superior operating frequency at iso-power. SL-MoS_2 and BL-MoS_2 offer considerably better performance over 500 nm wide Si nanosheet, having nearly 1.33× and 1.57× higher frequency, respectively, for the same power consumption of 44.7 μW/m. On the other hand, at a high frequency of approximately 256 GHz, BL-MoS_2 demonstrates approximately 0.52× lower power dissipation compared to the 500 nm wide Si nanosheet. The significantly improved power consumption with MoS_2 is due to the enhanced electrostatic control facilitated by higher I_{ON} and lower SS. In addition, BL-MoS_2 displays around 1.58× higher frequency while consuming 1.04× higher power as compared to the 500 nm wide Si nanosheet at V_{DD} = 0.7

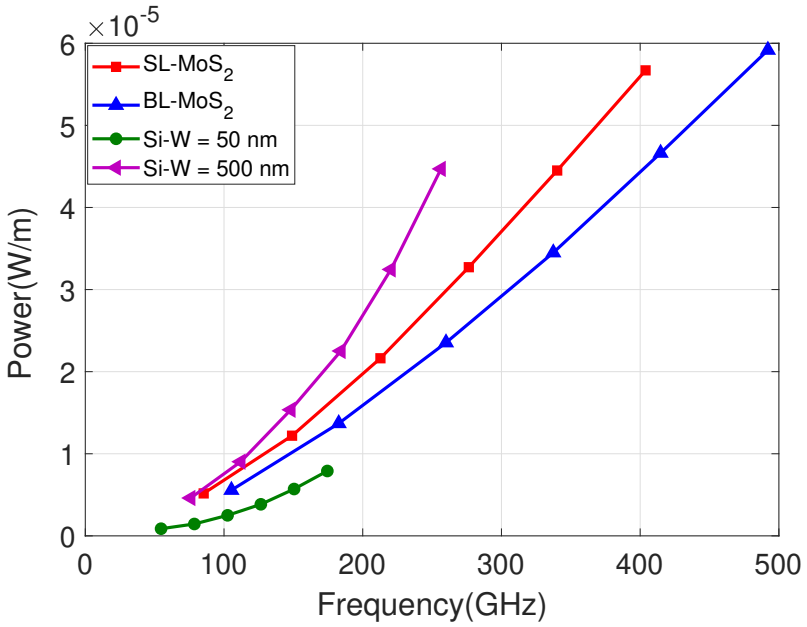

Figure 5.8: Power (P) vs. frequency (f) of the CMOS inverters based on SL-MoS_2, BL-MoS_2, and various width ($W = 50$ and 500 nm) Si nanosheets for the N1 node. The V_{DD} for this analysis is scaled in the range of 0.3 V to 0.8 V.

V. Therefore, a higher operating frequency and a lower power consumption make BL-MoS_2 a promising candidate for future high-speed and low-power logic applications.

5.6 Summary

The short-channel performance of SL- and BL-MoS_2 NS-FETs and their switching performance benefits over Si NS-FET with different widths using fully calibrated 3-D TCAD simulation is investigated. The findings indicate that integrating atomically thin SL- and BL-MoS_2 in stacked NS-FET provides a promising opportunity to achieve high ON-current and ON-OFF current ratio, while maintaining a near-ideal SS. The BL-MoS_2 NS-FET has exhibited more favorable switching characteristics compared to both SL-MoS_2 and Si NS-FETs for sub-5 nm nodes. Furthermore, the switching performance metrics of MoS_2 NS-FET can be further enhanced by increasing the number of layers and selecting a smaller equivalent oxide thickness. The study has also observed a significantly inferior switching performance with Schottky barrier-type contact, even with the lowest SB height compared to the doped-type contact NS-FETs. The CMOS inverter with BL-MoS_2 has found to maintain its performance advantages with showing a higher operating frequency at nearly the same power and lower power dissipation at a nearly identical frequency compared to that of the SL-MoS_2 and Si NS-FETs. This study provides a solid foundation for understanding stacked two-dimensional material-based NS-FETs and creating valuable insights into device design and experimental realizations.

Chapter 6

CMOS Inverters Based on 2-D Materials

6.1 Introduction

A complementary metal-oxide-semiconductor (CMOS) inverter, comprising pull-up p-MOS and pull-down n-MOS, is the most fundamental unit for digital ICs. The static and dynamic performance metrics of CMOS inverter can be used to derive the device performance in more complex digital circuits. As 2DM-based devices are still in their early stage of development, the performance projection of 2DMs in CMOS configuration could provide a solid foundation for mainstream logic and memory applications. CMOS inverter based on the two-dimensional channel was first demonstrated by integrating p-type, and n-type transistors on the monolayer graphene sheet [35]; however, this inverter is limited by high leakage current due to zero energy gap of graphene. After that, homogeneous CMOS inverters using electrostatic, chemical, and contact metal work function doping on single 2DM sheets, such as MoS_2, WSe_2, and BP, have developed rapidly and demonstrated excellent switching dynamics and better electrostatic behavior [15, 36, 110, 111, 112]. Furthermore, heterogeneous CMOS inverter configurations with two different layered materials for the channel, such as n-MOS using MoS_2, and p-MOS using α-$MoTe_2$, BP, WSe_2, and Si-nanowire, have actively been investigated for larger gain, noise margin and speed [15, 39]. Recently, p-type WSe_2 and n-type MoS_2 based CMOS inverters have attracted much interest for high gain and low-power applications because WSe_2 and MoS_2, respectively, possess higher room temperature electron and hole mobilities, among 2DM-FETs [40, 41, 113]. However, most of the work done till now on CMOS inverters based on 2DMs are arbitrary and lacking a comprehensive analysis. Moreover, the channel length is much larger than the current (Si) CMOS technology. Therefore, 2DM-based inverters need a complete performance analysis at deep nanometer-scale channel length to guide the experiments and trigger more efforts.

In this chapter, the static and dynamic performance of homogeneous inverter configurations based on MoS_2, WS_2, WSe_2, WTe_2, BP, and heterogeneous CMOS inverter configuration based on WSe_2-MoS_2 is examined. To assess their performance potential, 2DM-FETs and inverters are systematically benchmarked with ultrathin-body

Si counterparts. These six configurations are particularly employed as they exhibit a higher degree of readiness for ICs development [15, 114, 115]. The performance projection and benchmarking of 2DM-CMOS inverters in sub-10 nm channels is done using a multi-scale modeling approach that connects the three design levels, such as material, device, and circuit. Using material properties, firstly atomistic simulation is performed which is based on the self-consistent solutions of 2-D Poisson's equation and non-equilibrium Green's function (NEGF) formalism. Subsequently, the drain current and terminal charges from Green's function are implemented in the Cadence circuit simulator using the Verilog-AMS interface to evaluate the circuit-level performance metrics.

6.2 Device Geometry

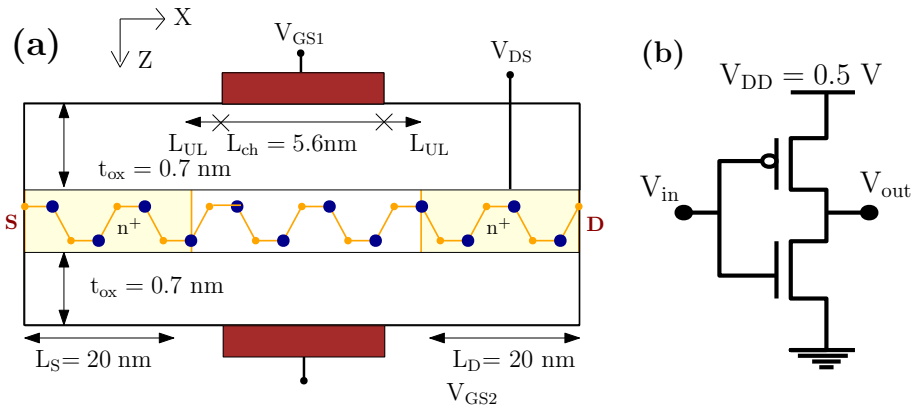

Figure 6.1: (a) Simulated device geometry, and (b) circuit schematic of CMOS inverter.

Fig. 6.1(a) shows the schematic of 2DM-based double-gate MOSFET, which is used in the simulation. The structural parameters for n-type and p-type 2DM-FETs are taken from low power ITRS 2028 projection [109]. The intrinsic monolayer 2DM sheet of L_{ch} = 5.6 nm length is considered as the channel material, whereas 2DM sheet doped to p-type/n-type with the concentration of 5×10^{13} cm^{-2} and length $L_S = L_D$ = 20 nm are considered as the source and drain regions for p-MOS and n-MOS. An underlap of L_{UL} = 0.7 nm length is used on both the source-channel and channel-drain sides to counter fringing field effects and reduce the DIBL [79]. The hafnium oxide (HfO_2) with a dielectric constant of 20 and thickness of 2.19 nm is considered as top and bottom gate oxide materials that corresponds to the equivalent oxide thickness of 0.45 nm. For Si-FET, the ultra-thin body of 3 nm is considered for simulation in this work, while other device design parameters are kept the same as mentioned in Fig. 6.1(a). The channel length of p-MOS and n-MOS is varied in the simulation as per the ITRS 2028 requirement for LP (low power) technology [109], to explore their impact on inverter performance.

Table 6.1: Material Attributes for 2DMs from First-Principle DFT Simulations [117, 118, 119, 120, 121, 122]

Material	m_{e_x}	m_{e_y}	m_{h_x} **(m$_0$)**	m_{h_y}	**a$_c$ (nm)**	**E$_{gap}$ (eV)**	μ_n $(\frac{cm^2}{Vs})$	μ_p $(\frac{cm^2}{Vs})$
BP	0.17	1.12	0.15	6.35	0.457	1.61	94	116
MoS_2	0.46	0.46	0.56	0.56	0.318	1.8	81	60
WS_2	0.309	0.309	0.412	0.412	0.318	1.82	185	185
WSe_2	0.346	0.338	0.462	0.451	0.332	1.53	202	200
WTe_2	0.302	0.299	0.40	0.40	0.355	1.06	185	185
Si	0.22	0.98	$m_{lh} = 0.224$ $m_{hh} = 0.268$ $m_{so} = 0.225$	-	0.54	1.12	200	150

Further, the considered scaling specifications are very near to IRDS requirement [116], which provides the future road map for Gate All Around (GAA) device. Fig. 6.1(b) shows the 2DM-based CMOS inverter schematic, in which same geometry for n-MOS and p-MOS is used, as they have nearly the same current driving capabilities.

6.3 Simulation Technique

The initial step in the multi-scale modeling methodology is to acquire the material attributes from reported experiments and DFT simulations, as shown in Table 6.1. Due to its high anisotropy, BP exhibits considerably different effects in the armchair and zigzag directions [123]. For BP, transport is conducted along the low effective mass armchair direction. To ensure uniform performance comparison, ultra-thin body Si-based p-MOS and n-MOS devices are simulated using the same approach, taking into account transport along the <100> orientation.

6.3.1 Quantum Transport Simulation

To accurately estimate the short channel performance of the 2DM-FETs, atomistic device simulation is utilized based on self-consistent solutions of the ballistic non-equilibrium Green function (NEGF) formalism and 2-D Poisson's equation, as described in Chapter 2. Further, the dissipative electronic transport is considered in the simulation by incorporating the backscattering coefficient. The dissipative source-to-drain

current density can be given as

$$I_{DS} = \frac{2q}{hW} \times \left(\frac{1-r}{1-r}\right) \times \int_{BZ} dk_y \int dE T(E,k_y)[f_S(E) - f_D(E)] \tag{6.1}$$

Where h is the Planck's constant, r is is the backscattering coefficient calculated as $r = l_c/l_c + \lambda$, W is the device width, and $T(E,k_y)$ is the transmission coefficient that can be computed as $T(E,k_y) = \Gamma_S(E,k_y)D_D(E,k_y)$. The critical length l_c, is the distance from top of the conduction band to the position where the potential drops by K_BT/q and λ is the mean free path and computed as $\lambda = \frac{2\mu_0}{V_T} \times \frac{k_BT}{q} \times \left(\frac{F_0(\eta_F)}{F_{-1/2}(\eta_F)}\right)$; where $F_j(\eta_F)$ is the Fermi-Dirac integral of order j, V_T is thermal velocity of the 2-D electron gas and calculated as $V_T = \sqrt{2k_BT/\pi m_y}$. The μ_0 is the experimentally measured low field mobility, which provides an analytical relation between the mobility and scattering strength [124].

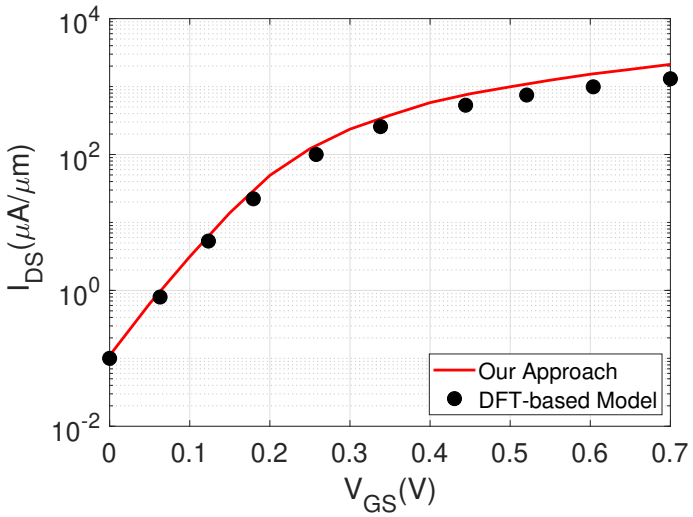

Figure 6.2: Transfer characteristics ($I_D - V_{GS}$) of MoS_2-FET by the developed model in this work and full-band NEGF simulation model by Szabo et al. [63] at $V_{GS} = 0.68$ V.

The accuracy of the back-scattering model can be verified by calibrating results with full-band DFT simulation-based NEGF model [63]. Fig. 6.2 shows I-V characteristics of MoS_2-FET with dissipative NEGF model [63] and the methodology used for this work. It is observed that I-V characteristics of MoS_2-FETs have also shown an excellent match with a more sophisticated full-based NEGF simulation. However, the agreement with experiments is qualitative due to a big difference between the considered simulation and limitations, such as Schottky contact, channel length, interface effect, and contact resistances, of currently fabricated 2DM-FETs.

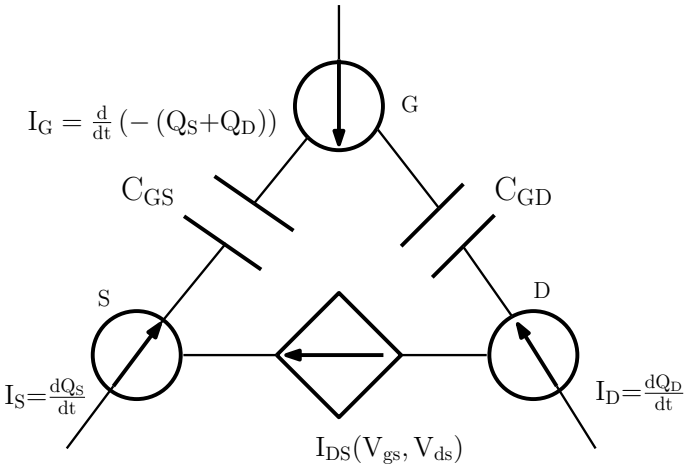

Figure 6.3: Verilog-AMS model for 2DM-FETs.

6.3.2 CMOS Inverter Simulation

To evaluate the circuit-level behavior of 2DM-FETs, a Verilog-AMS model based on a look-up table is utilized. Fig. 6.3 illustrates the implemented Verilog-AMS model for 2DM-FETs. This model comprises two-dimensional tables representing the terminal current, $I_{DS}(V_{DS}, V_{GS})$, the source terminal charge, $Q_S(V_{DS}, V_{GS})$, and the drain terminal charge, $Q_D(V_{DS}, V_{GS})$. The source and drain charges are calculated by extracting the local-density-of-states (LDOS) of the source and drain contacts (as depicted in Eq. 2.39 in Chapter 2) and then multiplying them by the source and drain Fermi functions. In order to provide a more realistic simulation, external parasitic capacitances are added to the intrinsic capacitances. The static and dynamic performance metrics of inverters are subsequently derived from the Cadence simulation.

6.4 Results

Fig. 6.4(a) and (b) show the transfer characteristics of MoS_2, WS_2, WSe_2, WTe_2, BP, and Si-based p-MOS and n-MOS, respectively, at $|V_{DS}| = 0.5$ V. These transfer characteristics of 2DMs and Si-FETs are obtained at fixed OFF-state current of around 50 nA/μm by adjusting the gate metal work-function difference. The p-MOS and n-MOS based on 2DMs have nearly symmetric transfer characteristics due to nearly the same conduction and valance band effective masses, as shown in Table 6.1. The matched current levels for p-MOS and n-MOS could overcome the sizing problem for CMOS technology that can lead to significant improvement in packaging density and energy efficiency. It is observed that at high V_{GS}, p-MOS and n-MOS based on 2DMs have higher drive current than that for Si-FETs, while Si-FETs exhibit higher current densities at low V_{GS}. It is seen

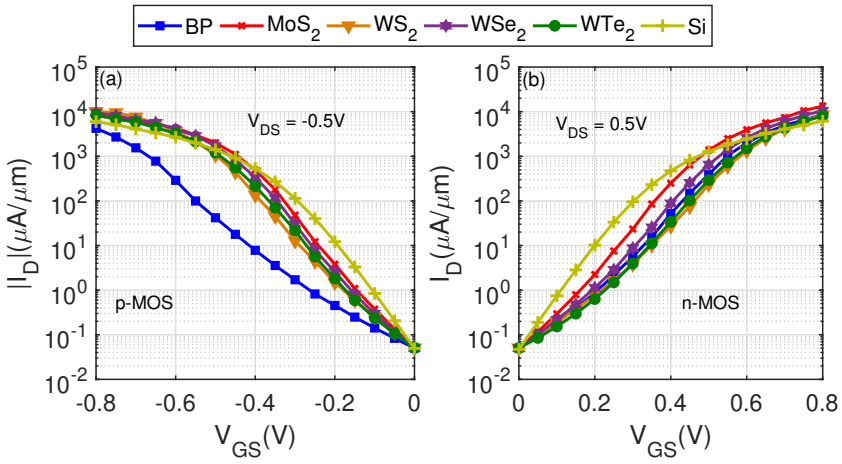

Figure 6.4: Transfer characteristics ($I_D - V_{GS}$) of BP, MoS_2, WS_2, WSe_2, WTe_2, and Si-based FETs at fixed $I_{OFF} = 50\ nA/\mu m$ for (a) p-MOS at V_{DS} = -0.5 V and (b) n-MOS at $V_{DS} = 0.5$ V.

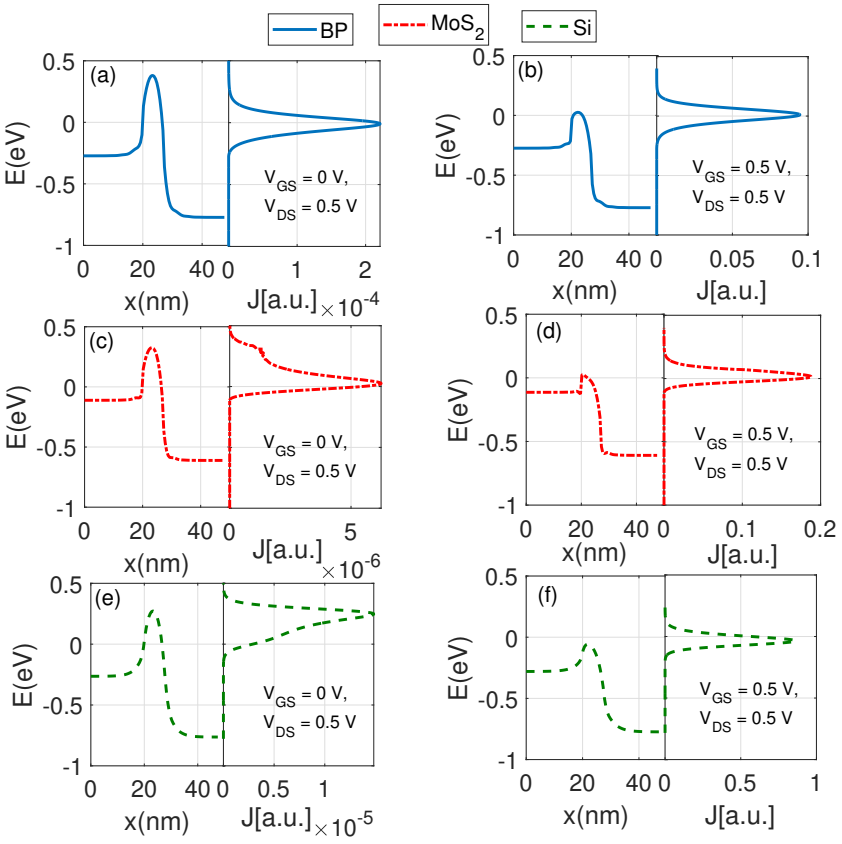

Figure 6.5: Potential energy profile and the corresponding current spectra of (a)-(b) BP-FET, (c)-(d) MoS_2-FET, and (e)-(f) Si-FET for V_{GS}= 0 V (left side), and V_{GS} = 0.5 V (right side) at $V_{DS} = 0.5$ V.

in Fig. 6.5 that, at low V_{GS}, the current is essentially due to source-to-drain tunneling, and lower transport mass in Si leads to higher source-to-drain tunneling current. However, at high V_{GS}, the thermionic current contribution becomes significant with increasing the

channel potential, as shown in Fig. 6.5. A lower transverse effective mass gives low density-of-states and hence, a lower thermionic current component.

It is observed that WSe_2-based p-MOS and MoS_2-based n-MOS have shown nearly the same I-V characteristics. The current density for these devices is also higher among 2DM-FETs, making them more suitable for high-performance CMOS technology. Even though BP-based n-MOS has excellent switching characteristics, the drive current of BP-based p-MOS is significantly lower among 2DM-FETs. The reason is that a lower effective mass material of BP increases the source-channel tunneling leakage current at the OFF-state, which requires a much larger negative gate bias to achieve the fixed OFF current. Consequently, it reduces the ON-state drive current at a fixed value of V_{DS}. It is found that higher effective mass materials, such as MoS_2 for n-MOS and WTe_2 for p-MOS, have higher drive currents as they require a smaller part of V_{GS} to shut the device OFF-state. Therefore, a higher effective mass material could have a considerable advantage of high drive current for ultra-scale devices.

6.4.1 Gate Capacitance of 2DM-FETs

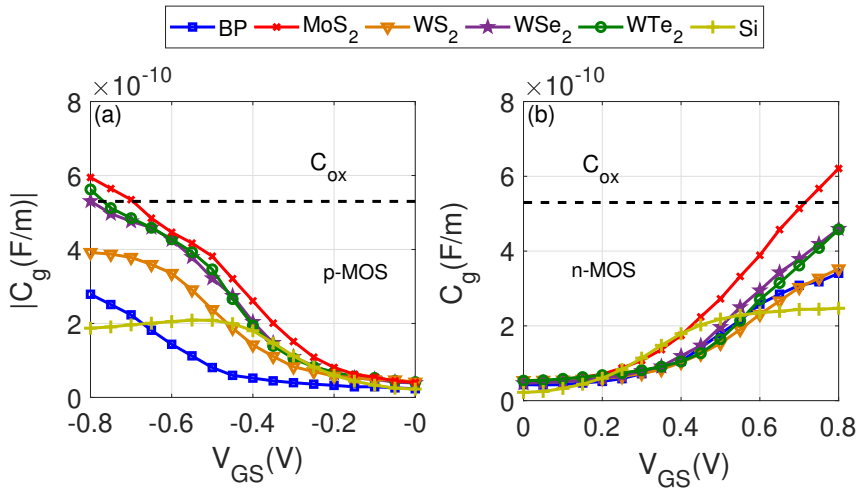

Figure 6.6: Gate capacitance (C_g) as a function of V_{GS} for BP, MoS_2, WS_2, WSe_2, WTe_2, and Si-based FETs at fixed I_{OFF} = 50nA/μm for (a) p-MOS at V_{DS} = -0.5 V and (b) n-MOS at V_{DS} = 0.5 V.

Fig. 6.6(a) and (b) show the gate capacitance (C_g) for BP, MoS_2, WS_2, WSe_2, WTe_2, and Si-based p-MOS and n-MOS, respectively, at $|V_{DS}| = 0.5$ V. It is observed that p-MOS and n-MOS based on MoS_2 have higher C_g among 2DM-FETs and Si-FETs. The C_g represents the series combination of oxide capacitance (C_{ox}) and quantum capacitance (C_q), i.e. C_g=$C_{ox}C_q/(C_{ox}+C_q)$. Because of ultra-thin high-k gate oxide, 2DM-based devices operate in the quantum-capacitance limit ($C_{ox} > C_q$). In quantum-capacitance

limit, the C_g is nearly equal to the C_q. As a result, a heavier effective mass MoS_2 gives larger value of quantum capacitance C_q as $C_q \propto m^*$ [125].

6.4.2 Short Channel Performance Metrics of 2DM-FETs

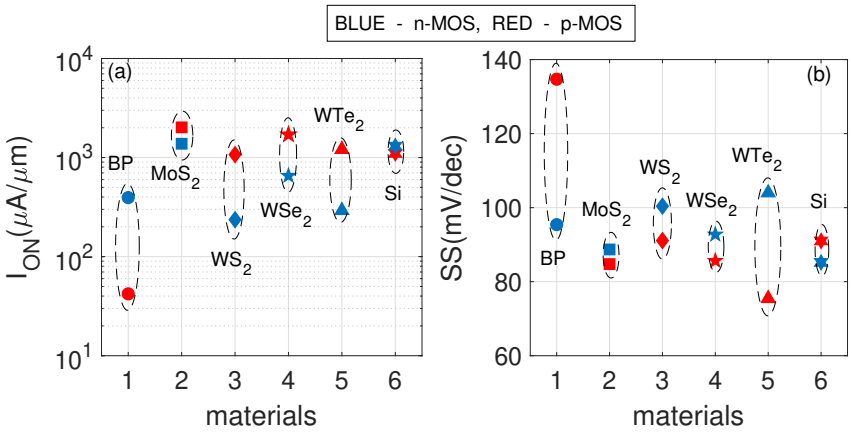

Figure 6.7: Short channel performance of p-MOS and n-MOS based on BP, MoS_2, WS_2, WSe_2, WTe_2, and Si at the fixed I_{OFF} = 50nA/μm: (a) I_{ON} for $|V_{DS}|$ = 0.5 V, and (b) sub-threshold swing (SS).

Fig. 6.7(a) and (b) show the ON-state current (I_{ON}) and minimum sub-threshold swing (SS), respectively, at $|V_{DS}|$ = 0.5 V for BP, MoS_2, WS_2, WSe_2, WTe_2, and Si-based p-MOS and n-MOS. The I_{ON} is computed from the considered OFF-state $I_{OFF} = I_D(V_{GS} = V_{OFF}, V_{DS} = V_{DD})$ as $I_{ON} = I_D(V_{GS} = V_{OFF} + V_{DD}, V_{DS} = V_{DD})$. It is observed from Fig.6.7(a) that the ON current is in the range of 0.1-10 $mA/\mu m$ and ON-OFF current ratio in the range of $2 \times 10^3 - 2 \times 10^5$ at 5.6 nm channel length, which promises the excellent switching performance with short channel 2DM-FETs. It is found that MoS_2, WSe_2 based p-MOS, and WTe_2-based p-MOS exhibit higher ON current and promise better logic performance over Si-FET. However, p-MOS and n-MOS based on BP exhibit a large difference in ON current, and hence, need to be properly sized for energy-efficient CMOS technology.

Fig. 6.7(b) shows that 2DM-FETs, except BP-based p-MOS and WTe_2-based n-MOS, exhibit sub-threshold swing (SS) well below 100 mV/decade, which is a practically acceptable limit for short channel device. It is observed that lower effective mass materials, such as BP-based p-MOS and WTe_2-based n-MOS, have a sub-threshold swing larger than 100 mV/decade. This is because a lower effective mass material enhances the direct source-to-drain tunneling current at low V_{GS}, as shown in Fig. 6.5. It is found that MoS_2 and WSe_2 can offer lower SS than that of Si-FETs. Therefore, a higher effective mass material might be better suited for low-voltage applications with higher drive-current and

strong SS characteristics.

6.4.3 Static Performance of 2DM-based CMOS Inverters

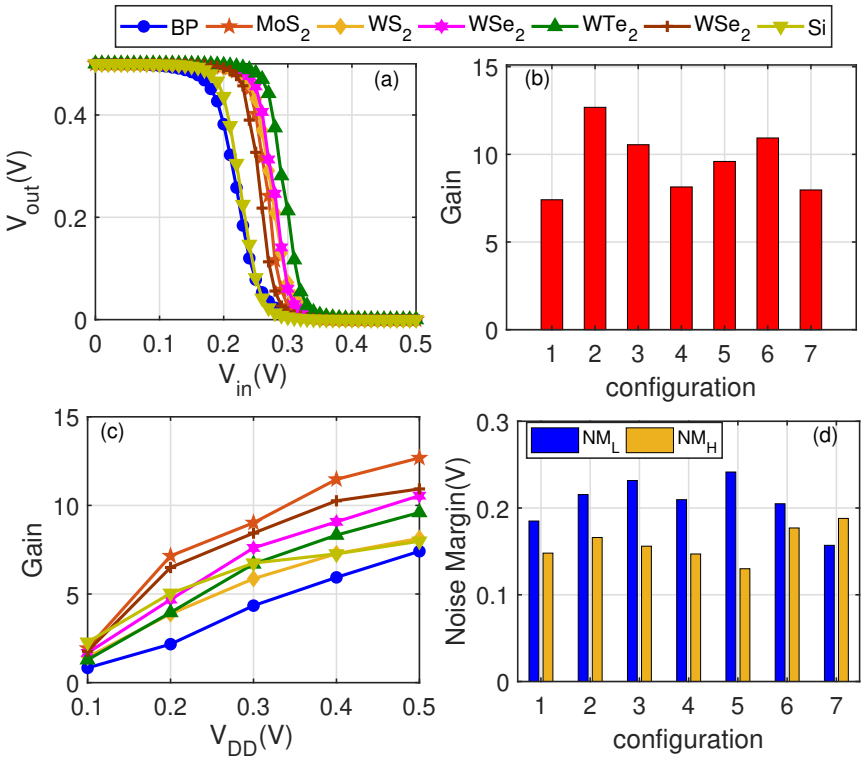

Figure 6.8: Static Performance of 2DM and Si-based CMOS Inverters at V_{DD} = 0.5 V: (a) voltage-transfer characteristics (VTC) for V_{input} in the range of 0 V to 0.5 V, (b) maximum DC gain , (c) maximum DC gain as a function of supply voltage (V_{DD}), and (d) logic-low (NM_L) and logic-high (NM_H) noise margins. CMOS configurations are defined as 1: BP, 2: MoS_2, 3: WSe_2, 4: WS_2, 5: WTe_2, 6: WSe_2-MoS_2, and 7: Si.

Fig. 6.8(a) shows the voltage-transfer characteristics (VTC) of CMOS inverter configurations based on BP, MoS_2, WS_2, WSe_2, WTe_2, WSe_2-MoS_2, and Si at V_{DD} = 0.5 V for V_{input} in the range of 0 to 0.5 V. Despite having same size p-MOS and n-MOS devices, 2DM-based inverters exhibit well-behaved VTC with sharp transitions, narrow transition region of around 130-155 mV, and a high-to-low output dynamic that reach the rail-to-rail supply voltage range. This is because the strong sub-threshold characteristics of both n-MOS and p-MOS devices are not degrading the high and low logic states. The WSe_2-MoS_2 configuration observes a sharp transition in VTC with the switching threshold voltage of around 0.25 V ($V_{DD}/2$) because of the matched current levels for both devices. The VTC demonstrates that strong low-logic for BP and Si-based inverters are observed because of lower value of drive current for their p-MOS. Therefore, highly symmetric I-V characteristics of p-MOS and n-MOS could be attributed to the sharp transition in VTC that means high gain and better noise margin.

Fig. 6.8(b) shows that the maximum DC gain $\left(\frac{dV_{out}}{dV_{in}}\right)$ for 2DM and Si-based CMOS inverters that are extracted from VTC at $V_{DD} = 0.5$ V. It is observed from Fig. 6.8(b) that DC gain of 2DM-based inverters, except BP-based inverter, is in the range of 8-12.7 V/V for 5.6 nm channel, which is higher than the gain of Si-based CMOS inverter. The MoS_2-based inverter has shown a higher gain of around 12.68 V/V, whereas BP and Si-based inverter provide the lower gain of 7.1 V/V and 7.9 V/V, respectively. Fig. 6.8(c) shows the inverter gain for different supply voltage in the range of 0.1 to 0.5 V. It is found that the gain of the inverter reaches around 1 when the supply voltage scales down to 0.1 V. At such low supply voltage, both p-MOS and n-MOS are in the OFF-state. An inverter with a gain greater than 1 is much desirable for multistage logic circuits because it makes the circuit robust to errors and regenerative. It is observed that MoS_2-based inverter has exhibited a decent gain of above 5 even for $V_{DD} = 0.2$ V, making it the best candidate for low voltage applications. However, the gain of BP-based inverter significantly decreases with scaling down the supply voltage and reaches around 0.5 at $V_{DD} = 0.1$ V.

Fig 6.8(d) shows the high-level noise margin (NM_H) and low-level noise margin (NM_L) for 2DM and Si-based inverters that are extracted from VTC as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$, respectively. It is observed that high-level and low-level noise margins for 2DM-based inverters are in the range of $0.26V_{DD}$-$0.35V_{DD}$ and $0.37V_{DD}$-$0.5V_{DD}$ for the supply voltage of 0.5 V, which represent the tolerance to signal fluctuations. These noise margin values are well above the minimum noise margin requirement, which is around 10% of supply voltage. Among 2DM and Si-based inverters, WSe_2-MoS_2 outperforms in noise margin with maximum value of NM_L of around $0.35V_{DD}$ and nearly same NM_H of $0.5V_{DD}$, as that for Si-based inverter. Thus, the relatively high noise margins suggest that the WSe_2-MoS_2 configuration can be adopted in multistage circuit development.

6.4.4 Dynamic Performance of 2DM-based CMOS Inverters

Fig. 6.9(a) shows the delay for 2DM and Si-based inverter configurations that is computed by taking the time difference between 50% transitions of the input and output pulse. The delay of inverter can be approximated as $\tau = C_L V_{DD}/I_D$, where load capacitance ($C_L = C_{gp} + C_{gn} + C_f$) is consisted of gate capacitance of p-MOS (C_{gp}), gate capacitance of n-MOS (C_{gn}), and the external parasitic capacitance (C_f). The C_f is considered to be around $0.01 fF/\mu m$, which is the minimum reported value for 2DM-FETs [62]. It is observed from Fig. 6.9(a) that the delay of Si-based inverter is marginally lower than that for 2DM-based inverters. On the other hand, MoS_2-based inverter has lower

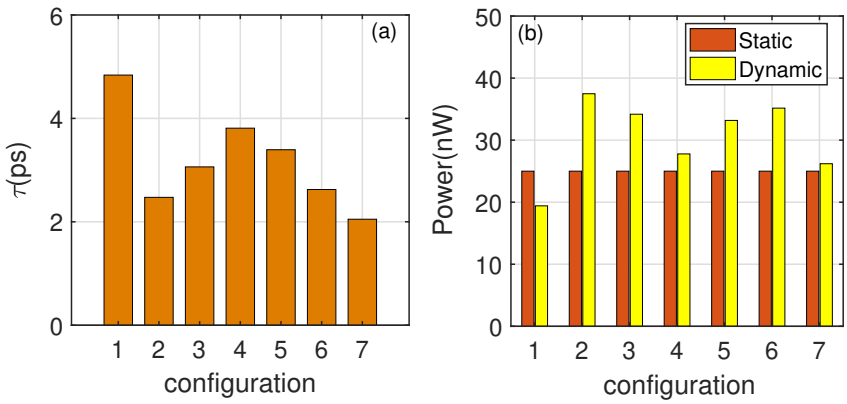

Figure 6.9: Static and dynamic performance of 2DM and Si-based CMOS inverters: (a) delay, and (b) static and dynamic power dissipations. Where CMOS inverter configurations are defined as 1: BP, 2: MoS_2, 3: WSe_2, 4: WS_2, 5: WTe_2, 6: WSe_2-MoS_2, and 7: Si.

delay among 2DMs and its delay (2.5 ps) is nearly same as that for Si-based inverter (2.1 ps). Among 2DM-based inverters, the switching speed of WSe_2-MoS_2 based inverter is also found to be comparable to the lowest delay MoS_2-based inverter, as they are having nearly identical drive current. Therefore, inverters based on higher electron and hole masses, such as MoS_2 and WSe_2-MoS_2, could be more beneficial for high-speed ICs.

Fig. 6.9(b) shows the static power ($P_s = V_{DD}I_D$) and dynamic power dissipation of 2DM and Si-based CMOS inverter configurations. The dynamic power dissipation can be approximated as $P_d = C_L V_{DD}^2 f$, where f is the clock frequency and taken to be 200 MHz. It is found that, among the Si and 2DM-based inverters, BP-based inverter has smaller switching energy due to their significantly smaller gate capacitance. Due to their higher gate capacitances, MoS_2 and WSe_2-MoS_2 exhibit around 40% and 35% higher dynamic power dissipation than that of Si and BP-based inverters. The contribution of static power dissipation at 50 nA/μm is found to be around 40% of the total power dissipation. This contribution can be minimized further by proper device design. The switching energy of inverter is related to their gate capacitance. Consequently, inverter based on lower effective mass 2DMs has a fundamental advantage in dynamic power dissipation as $C_q \propto m^*$. Therefore, low effective mass BP-based inverter configuration is more favorable candidate among Si and 2DM-based inverters for low-power applications.

6.4.5 Impact of Contact Resistance

Fig. 6.10(a) and (b) show the delay and power-delay product (PDP), respectively, as a function of contact resistance (R_c) for BP, MoS_2, WS_2, WSe_2, WTe_2, WSe_2-MoS_2, and Si-based inverters. The value of contact resistance is in the range of 50-200 $\Omega - \mu$m for

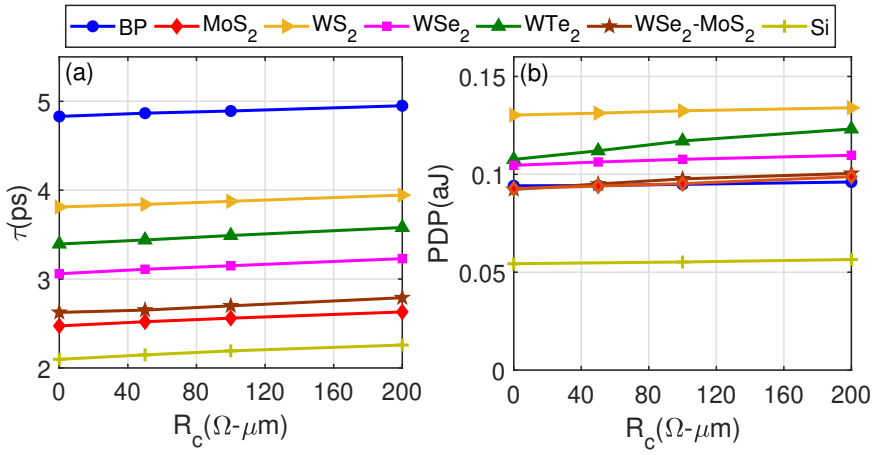

Figure 6.10: (a) Delay and (b) power-delay product (PDP) of 2DM and Si-based inverters as a function of contact resistance (R_c).

the simulation of this work, whereas 200 $\Omega - \mu$m is close to the minimum value of contact resistance reported for 2DM-FETs [126], [127]. It is observed that the delay and PDP increase with the increasing contact resistance. The reason for that is the drive current of the CMOS inverter reduces with increasing contact resistance. The reduced value of drive current takes more time to charge and discharge the load capacitance, and thereby results in a marginal increase in delay and PDP. Therefore, the minimum possible value of contact resistance in 2DM-FETs will help in achieving low-power and faster speed operations in CMOS circuits.

6.4.6 Impact of External Parasitic Capacitances and Interconnect Parasitics

Fig. 6.11(a) and (b) show the delay (τ) and dynamic power (P_d) dissipation, respectively, as a function of external parasitic capacitance (C_f) for 2DM and Si-based inverter configurations. Further, Fig. 6.11(c) shows the ratio of external parasitic capacitance to the load capacitance (C_f/C_L) as a function of external parasitic capacitance for 2DM and Si-based inverters. The value of external parasitic capacitances, due to the fringing field, considered is in the range of 0.01-0.5 fF/μm for the simulation of this work, which are minimum values reported for 2DM-FETs [62]. It is observed from Fig. 6.11(a) and (b) that delay and power dissipation increase significantly with marginal increment in the parasitic capacitances. This is because the intrinsic gate capacitance of 2DM-based devices is comparable to the parasitic capacitance value. This can also be inferred from Fig. 6.11(c) that the external parasitic capacitance starts dominating on load capacitance, when the C_f increases beyond 0.2 fF/μm. Since the delay and dynamic power is directly proportional to load capacitance, they increase approximately 2× with

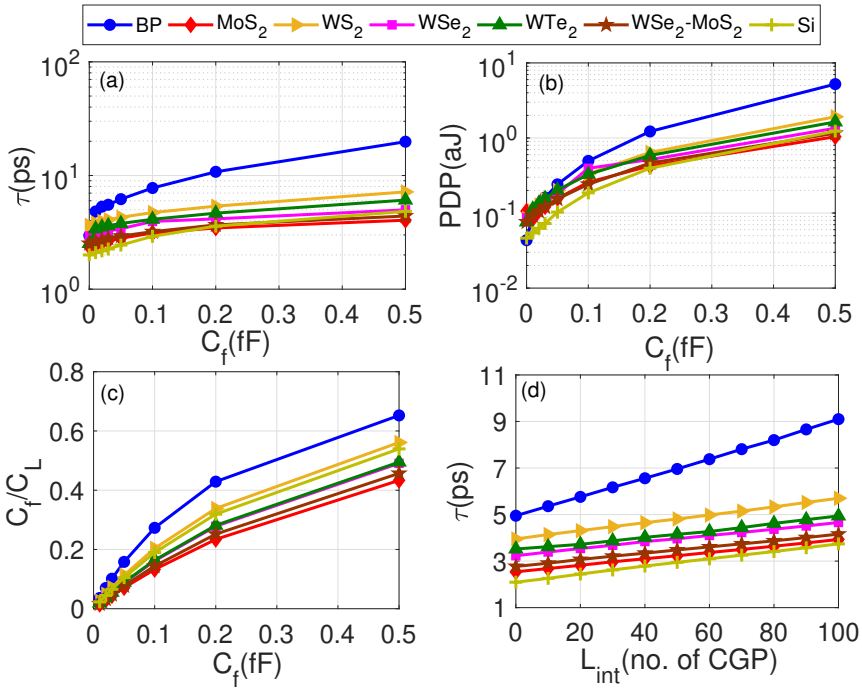

Figure 6.11: (a) Delay and (b) power-delay product (PDP) of 2DM and Si-based inverters as a function of external parasitic capacitance (C_f) (c) Ratio of external parasitic capacitance to load capacitance (C_f/C_L) versus external parasitic capacitance (C_f) (d) Delay of 2DM and Si based Inverters as a function of interconnect length at R_c = 200 $\Omega - \mu$m.

increasing the parasitic capacitance value. It is also found that at higher C_f, the delay of Si-based inverter can become larger compared to MoS_2 and WSe_2-MoS_2 based inverters. Therefore, optimizing the device geometry for low external parasitic capacitances would be of great significance to achieve high-speed and low-power CMOS technology.

Fig. 6.11(d) shows the delay of 2DMs and Si-based CMOS inverter configurations as a function of interconnect length at fixed contact resistance. The value of contacted gate-pitch (CGP) of 45 nm interconnect length is considered with interconnect parasitic resistance per unit length of R_{int} = 317.4 Ω-μm and capacitance per unit length of C_{int} = 153 aF/μm [128]. It is observed from the Fig. 6.11(d) that delay of the 2DM-based inverters considerably increases with increase in the value of interconnect length. The BP-based inverter shows maximum degradation in delay with interconnect length, and delay becomes almost double at 100 CGP interconnect length. The most of the 2DM-based inverters show a marginal increment in delay with increasing interconnect length, and delay reaches around 1.38-1.54× at maximum interconnect length. Thus, interconnect with low values of parasitic capacitance and resistance is more suitable to attain high speed switching in 2DM-based inverters.

6.4.7 Impact of Channel Length

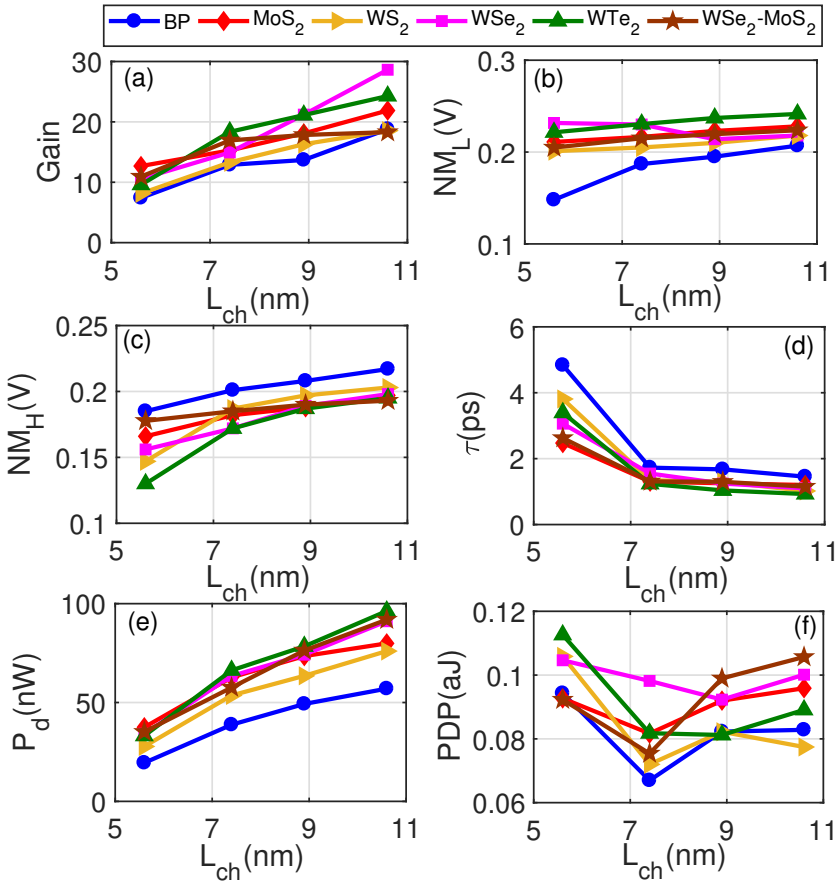

Figure 6.12: Static and dynamic performance dependency on the device channel length at fixed OFF-state current 50 nA/μm for $V_{DD} = 0.5$ V: (a) gain, (b) logic-low noise margin (NM_L), (c) logic-high noise margin (NM_H), (d) delay (τ), (e) dynamic power dissipation (P_d), and (f) power-delay product (PDP) as a function of channel length.

Fig. 6.12 shows the static and dynamic performance metrics of the 2DM-based inverters as a function of channel length at fixed OFF-state current of around 50 nA/μm and $V_{DD} = 0.5$ V. It is observed from Fig. 6.12(a) that the peak gain of 2DM-based inverters considerably reduces as the channel length decreases. The BP-based inverter exhibits significant performance degradation in the maximum gain from 22 to 5 with decreasing channel length from 10.6 nm to 5.6 nm. It can be attributed to a significant increment in source-to-drain tunneling for lower effective mass material that degrades the drive current and SS characteristics. For $L_{ch} > 7$ nm, inverters based on moderately higher effective mass materials, such as WSe_2 and WTe_2, have marginally higher gain among 2DM-based inverters, whereas inverter based on heavier mass material, such as MoS_2, attains higher gain for $L_{ch} < 7$ nm because of higher drive current.

Fig. 6.12(b) and (c) show that NM_L and NM_H for 2DM-based inverters decrease marginally with decreasing the channel length. In contrast, the BP-based inverter

exhibits a significant reduction in NM_L as its lower transport effective mass results in a considerably smaller drive current. Among 2DM-based inverters, the noise margins of WSe_2-MoS_2 inverter are marginally decreased with decreasing the channel length and found to be around 35% of V_{DD} at 5.6 nm channel length. It is observed from Fig. 6.12(d) that the delay of 2DM-based inverters moderately increases as the L_{ch} scale down to 7 nm, but it suddenly rises at 5.6 nm channel length. However, the delay of BP-based inverter increases significantly compared to other 2DM-based inverters because of significant drive current reduction with scaling down the channel length. Fig. 6.12(e) shows that the dynamic power dissipation for 2DM-based inverters considerably reduces as the channel length decreases. This is because the amount of charge induced during the ON to OFF transition decreases marginally. Fig. 6.12(f) shows that power-delay product (PDP) decreases significantly for $L_{ch} > 7$ nm, then it is suddenly increased at $L_{ch} < 7$ nm. The current and gate capacitance decrease as channel length decreases, but the drive current decreases significantly for $L_{ch} < 7$ nm. Therefore, WSe_2-MoS_2 could be a more attractive candidate for sub-10 nm channel length with a higher noise margin, higher speed, and immunity to short channel effects.

6.4.8 Performance Projection of CMOS Inverter at 3 nm Channel Length

Fig. 6.13 shows the static and dynamic performance metrics for MoS_2, WSe_2, MoS_2-WSe_2 based inverters at 3 nm channel length. It is found that among 2DM-FETs, MoS_2-FETs and WSe_2-FETs are the only candidates that allow OFF-state current below $I_{OFF} = 50\ nA/\mu$m at 3 nm channel length. At 3 nm channel length, there exists a considerable direct source-to-drain tunneling current. As a result, lower effective mass materials, such as BP, WS_2, WTe_2, have a significant increment in OFF-current. It is observed from Fig. 6.13(a) that the VTC of 3 nm inverters exhibit a wide transition region because both p-MOS and n-MOS are weakly conducting and require high V_{DD} to achieve the saturation. The wide transition region in VTC contributes to the peak gain of around 1.4-3.3 for V_{DD} in the range of 0.2-0.5 V, and noise margin of about 17.4-29.2% of V_{DD}, as shown in Fig. 6.13(b) and (c). The gain and noise margin decrease to 25% and 67% from 5.6 nm values. It is observed from Fig. 6.13(d) that the delay and PDP of 2DM-based inverters are also increased to around 4.5× and 1.25× from 5.6 nm channel length values. On the other hand, MoS_2-based CMOS inverter holds promise at 3 nm channel length with gain of 3.3, noise margin of $\mathrm{NM}_L = 0.27V_{DD}$ and $\mathrm{NM}_H = 0.23V_{DD}$, delay of around 13.54 ps, and power-delay product of 0.19 aJ. The static and dynamic

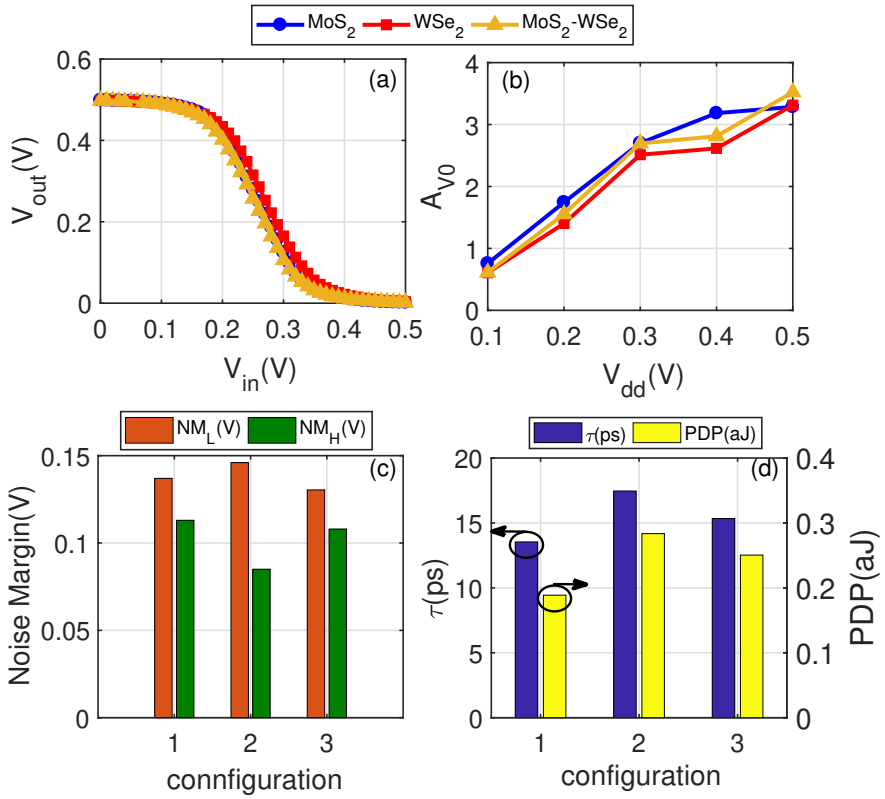

Figure 6.13: Static and dynamic performance of MoS_2, WSe_2, and MoS_2-WSe_2 based inverters at 3 nm channel length: (a) VTC for V_{input} in the range of 0 V to 0.5 V, (b) maximum DC gain as a function V_{DD}, (c) logic-low (NM_L) and logic-high (NM_H) noise margins, and (d) delay (τ) and power-delay product (PDP). Where CMOS inverter configurations are defined as 1: MoS_2, 2: WSe_2, and 3: MoS_2-WSe_2.

performance metrics for 2DM-based inverters are much better compared to the reported experimental results for long channel MOSFET [15, 39]. This shows that a larger room available for further improving the performance of 2DM-based CMOS inverters in the experiments.

6.5 Summary

Using a multi-scale modeling approach, a comprehensive performance analysis of CMOS inverter configurations based on 2DMs, such as BP, MoS_2 WSe_2, WS_2, WTe_2, WeS_2-MoS_2 is performed and then benchmarked against their Si counterpart for sub-10 nm channel length. The 2DM-based p-MOS and n-MOS have promised excellent switching performance with $I_{ON}/I_{OFF} > 10^3$ and SS $<$ 100 mV/dec at 5.6 nm channel length. Among 2DM-based inverters, heterogeneous WSe_2-MoS_2 CMOS inverter has got more suitability for logic applications with larger noise margins, nano-watt power dissipation, and comparative delay to Si-based inverter. From the switching energy perspective, the BP-based inverter has presented the best choice with the lowest power dissipation of

around 45 nW; however, it has around 50% slower speed than the WSe_2-MoS_2 CMOS inverter. It has been found that inverters based on higher electron and hole effective masses can be more favorable to scaling down the channel length below 3 nm. This chapter not only provides a solid understanding of 2DM-based devices and CMOS inverters performance for ultra-scale channel length but also gives insights into proper material selection, and device design and optimization in experiments.

Chapter 7

Conclusion

7.1 Summary

As electronic devices based on 2DMs are still in the early stages of development, this work has made numerous contributions to exploring novel 2DMs, understanding reliability issues, assessing performance in novel device architectures, and evaluating circuit-level performance. The primary goal of this research is to unlock the potential of 2DMs for digital IC development using a multi-scale modeling methodology. The major contributions and respective conclusions are as follows:

- The initial effort involves the development of a multiscale modeling methodology that connects three design levels, including material, device, and circuit.
  - This approach relies on a dissipative quantum transport model, with input material parameters extracted from first-principle DFT simulations. These obtained material attributes are subsequently utilized to develop the dissipative NEGF and Poisson solver for assessing device performance. Finally, the models are integrated into a circuit simulator to streamline the design and simulation of integrated circuits. This approach significantly reduces the number of required fitting parameters and enhances the accuracy of the resulting modeling environment compared to traditional TCAD-based methods.
  - The adoption of a 1-D elementary cell assumption has led to the development of a unique tight-binding Hamiltonian matrix for 2DMs, which significantly reduces the computational cost and provides similar results to full real-space calculations for 2DM-based FETs when the potential along the width direction is uniform.
  - The overall accuracy of the quantum transport has been assured by monitoring the bandstructure and verifying the current throughout the device with a full-band DFT-based simulation model.
- Using the multiscale modeling methodology, 40 novel 2DMs are investigated in N-MOSFET and P-MOSFET configurations, conducting performance analysis from

the device to the circuit level. Five of this extensive collection of electronic materials are identified to develop high-speed and low-power electronic circuits.

Table 7.1: Summary of Performance Metrics of FET, Inverter, SRAM, and ALU at V_{DD} = 0.6 V for the 1 nm Technology Node.

Material	FET		Inverter		SRAM		ALU		
	I_{ON}(P) mA/μm	I_{ON}(N) mA/μm	Delay (ps)	PDP (fJ/μm)	Delay (ps)	PDP (fJ/μm)	Energy (fJ)	Delay (ps)	Throughput (TIOPS/cm^2)
GeTe	2.52	2.49	1.02	0.48	3.07	1.2	24.10	1020	2.79×10^4
PbS	2.32	2.62	1.1	0.50	3.26	1.25	25.03	1092	2.63×10^4
Sn_2S_2	2.35	2.63	0.99	0.41	2.98	1.15	23.05	990	2.877×10^4
$Ti_2N_2Cl_2$	2.345	2.21	1.28	0.54	3.83	1.36	27.15	1280	2.24×10^4
$Ti_2Br_2N_2$	2.42	2.39	1.05	0.47	3.14	1.12	23.55	1050	2.73×10^4
Si	0.627	0.603	4.16	1.13	13.5	2.13	20.76	1782	3.37×10^3

  - Table 7.1 benchmarks the key switching performance metrics of five 2DMs with 50 nm wide Si nanosheet in NFET, PFET, CMOS Inverter, 6-T SRAM, and 32-Bit ALU configurations for N1 node at $V_{DD} = 0.6$ V. The Si data in the table is for a three-channel stacked gate-all-around nanosheet field-effect transistor (NS-FET). It is observed that the selected 2DMs offer considerably higher I_{ON} of around 3.75×–4.02× in PFET and 3.66×–4.34× in NFET, as compared to Si NS-FET. It is also observed that Sn_2S_2 based inverter and SRAM can provide around 8.2× higher speed increment compared to Si NS-FET. Additionally, 32-bit ALU with 2DMs offers a significantly higher throughput of around 6.6×–8.5×, compared to Si NS-FET.
  - The objective of this study is to provide the community with a comprehensive atlas of 2DMs capable of challenging Si devices and to inspire engineers working on the development of next-generation 2-D FETs.

- To understand the factors affecting the transfer characteristics of short-channel MoS_2-FET for overcoming the variability issue, a quantum mechanical modeling framework is proposed, which describes the interface trap state in MoS_2-FET.
  - The trap-induced inelastic tunneling current strongly affects I_{OFF}, V_{TH}, and SS for sub-18 nm gate length, while charge trapping marginally reduces I_{ON} of MoS_2-FET.

Table 7.2: Benchmarking of Device and Inverter Level Performance of SL-MoS_2, BL-MoS_2 and Si at $V_{DD} = 0.7$ V and Fixed I_{OFF} =10 nA/μm For N1 Node.

Attributes	**SL-MoS_2**	**BL-MoS_2**	**50 nm Si**	**500 nm Si**
I_{ON} (mA/μm)	2.97	3.71	0.297	2.13
I_{ON}/I_{OFF}	3×10^5	3.7×10^5	3×10^4	2.1×10^5
SS (mV/dec)	64.18	63.85	73.45	73.95
DIBL (mV/V)	18.67	17.58	66.96	71.54
f (GHz)	340.2	414.7	150.5	220.4
P (μW/m)	44.5	46.7	5.71	32.4

  - A high aerial density trap could lead to a more significant degradation in both the OFF-state and ON-state currents, resulting in a lower ON-OFF current ratio.
  - By controlling the trap position and reducing the interface trap density close to the $E_g/2$, the variability in $I_{DS} - V_{GS}$ characteristics and temperature dependency can be reduced significantly.

- Table 7.2 benchmarks the key switching performance metrics of SL-MoS_2, BL-MoS_2 and Si NS-FETs for N1 node at $V_{DD} = 0.7$ V. It is found that a large-area BL-MoS_2 NS-FET can deliver 12.5× higher I_{ON} and I_{ON}/I_{OFF} over 50 nm Si NS-FET with excellent short channel behavior (DIBL ∼17.58 mV/V and SS ∼63.85 mV/decade) for N1 node. It is found that BL-MoS_2 technologies are capable of around 2.7× speed increment as compared to widely investigated 50 nm wide Si NS-FETs. Thus, a larger transport effective mass and atomic thickness of SL- and BL-MoS_2 nanosheets offer more advantages in a multichannel architecture over the Si channel by enhancing the I_{ON} and reducing the OFF-state current.
  - The short-channel performance of SL- and BL-MoS_2 NS-FETs is investigated, and benchmarked their switching performance benefits over Si NS-FET with different widths using fully calibrated 3-D TCAD simulation.
  - The study has also observed a significantly inferior switching performance with Schottky barrier (SB)-type contact, even with the lowest SB height compared to the doped-type contact NS-FETs.
  - The CMOS inverter with BL-MoS_2 has been found to maintain its performance

advantages by showing a higher operating frequency at nearly the same power and lower power dissipation at a nearly identical frequency compared to that of the SL-MoS_2 and Si NS-FETs.

- Using a multi-scale modeling approach, Chapter 6 has done a comprehensive performance analysis of CMOS inverter configurations based on 2DMs, such as BP, MoS_2 WSe_2, WS_2, WTe_2, WeS_2-MoS_2 and benchmark against their Si counterpart for sub-10 nm channel length.
  - Among 2DM-based inverters, heterogeneous WSe_2-MoS_2 CMOS inverter has more suitability for logic applications with larger noise margins, nano-watt power dissipation, and comparative delay to Si-based inverter.
  - CMOS inverter with MoS_2, WSe_2, MoS_2-WSe_2 can be more favorable to scaling down the channel length below 3 nm.

  The important findings of this thesis can be directly applied to practical devices, as most of the modeling in this thesis has adopted a quantum transport mechanism. Furthermore, the results have been presented with non-ideal factors, such as contact resistance, interface trap charges, and parasitic effects. These conclusions could provide important guidance for optimizing and catalyzing further experiments in the field of 2DM-based devices.

7.2 Scope for Future Research

7.2.1 NEGF Approach for Modeling Novel Devices

For the future prospects of this thesis work, there exist several intriguing areas for exploration within the realm of applying NEGF in quantum transport simulations to novel devices. Firstly, the potential for NEGF extends to the investigation of advanced device architectures beyond the scope of GAA NS-FETs, which can offer much deeper insights into newer semiconductor technologies. The NEGF formalism applicability can be expanded to encompass a wider range of optoelectronic devices. This broader scope presents the opportunity to acquire a more profound comprehension of the intricate interactions between photons and electrons, ultimately paving the way for the design and fabrication of exceptionally efficient optoelectronic devices. Moreover, the NEGF formalism can be expanded to encompass emerging memory and sensing devices, further pushing the advancements in-memory technology and the development of adaptable sensors with multifaceted applications.

7.2.2 ML-based Approach for Enhancing Computational Efficiency of NEGF simulation

While the NEGF formalism offers valuable insights into the quantum transport of nanoelectronic devices, its computational demands increase significantly when the scattering mechanisms are considered within the formalism. To address this issue, a novel simulation approach will be developed that integrates machine learning (ML) techniques with the quantum transport simulator developed in this thesis, which can alleviate the computational costs associated with dissipative NEGF simulations. The initial step will involve acquiring a concise representation of a specific quantum transport property, followed by training a model to provide the quantitative connection between device parameters and properties. This approach can be tested to assess its with a wider range of materials and device architectures. The ML-based approach for device modeling has the potential to drastically reduce simulation times while maintaining a high level of accuracy.

7.2.3 Modeling Thermo-Electric Effect

One of the critical challenges for scaled 2DM-FETs pertains to the self-heating of the channel during device operation. The flow of electrical currents within the device leads to an overpopulation of phonons, which in turn, can impede transport and increase scattering with electrons due to the strong electron–phonon interaction. Joule heating and heat dissipation are fundamental processes governing charge transport, arising from the interaction between electronic charge carriers and molecular vibrations. These processes pose significant stability concerns in these devices. To incorporate these effects, electrical transport will be modeled using the NEGF formalism, taking into account phonon scattering, while thermal transport will be implemented using Fourier's law with modified boundary conditions.

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List of Publications

Journals

1. **Akhilesh Rawat**, Avinash Kumar Gupta and Brajesh Rawat, "Performance Projection of Two-dimensional Material based CMOS Inverters for Sub-10 nm Channel Length," ***IEEE Transactions on Electron Devices,*** vol. 68, no. 7, pp. 3622-3629, July 2021.

2. **Akhilesh Rawat**, and Brajesh Rawat, "The Role of Interface Trap States in MoS_2-FET Performance: A Full Quantum Mechanical Simulation Study," ***IEEE Transactions on Electron Devices***, vol. 70, no. 9, pp. 4913-4920, Sept. 2023.

3. Anjali Goel, **Akhilesh Rawat**, and Brajesh Rawat, "Benchmarking of Analog/RF Performance of Fin-FET, NW-FET, and NS-FET in the Ultimate Scaling Limit," ***IEEE Transactions on Electron Devices***, vol. 69, no. 7, pp. 1298-1305, March 2021.

4. **Akhilesh Rawat**, and Brajesh Rawat, "3-D Multichannel MOSFETs with Two-Dimensional MoS_2 Nanosheet for Future Technology Node," under revision in ***IEEE Transactions on Electron Devices***.

5. **Akhilesh Rawat**, and Brajesh Rawat, "Novel 2DMs Beyond MoS_2 for Post-Silicon Electronics: Atom-to-Circuit Level Simulation," under submission in ***ACS Applied Electronic Materials***.

6. **Akhilesh Rawat**, Vedant Sati, and Brajesh Rawat, "Analytical Model of Source-to-Drain Tunneling Current in Ultra-scaled Two-dimensional Material-based Field-Effect Transistors," under submission in ***IEEE Transactions on Electron Devices***.

Conference Proceedings

1. **Akhilesh Rawat**, Avinash Kumar Gupta, and Brajesh Rawat, " High-Performance Single and Multilayer Black Phosphorous-Based CMOS Inverter for Deep Sub-10nm Technology," *XXth International Workshop on Physics of Semiconductor Devices: IWPSD*, Kolkata , Dec. 2019.

2. Arjun Kumar, **Akhilesh Rawat**, and Brajesh Rawat, "Prospects of Two-dimensional Material-based Field-Effect Transistors for Analog/RF Applications," *34th IEEE International Conference on VLSI Design*, 2021.

3. Anjali Goel, **Akhilesh Rawat**, and Brajesh Rawat, "Performance Projection of Stacked Silicon Nanosheet-FET Architectures for Future Technology Node," XXIst International Workshop on Physics of Semiconductor Devices: IWPSD 2021, Delhi, India.

4. **Akhilesh Rawat**, Anjali Goel, and Brajesh Rawat, " Role of Interface Trap Charges in the Performance of Monolayer and Bilayer MoS_2-based Field-Effect Transistors ," *35th IEEE International Conference on VLSI Design*, March 2022 (Online).

5. **Akhilesh Rawat**, Anjali Goel, and Brajesh Rawat, "Performance of Two-Dimensional MoS_2 Field-Effect Transistor in the Presence of Oxide-Channel Imperfection ," *6th IEEE International Conference on Emerging Electronics (ICEE)*, Bengaluru, Dec. 2022.

6. Anjali Goel, **Akhilesh Rawat**, and Brajesh Rawat, "Finding Analog/RF Performance of Inserted High-K FinFET for Sub-5 nm Technology Node," 2022 IEEE International Conference on Emerging Electronics (ICEE), Bengaluru, India, Dec. 2022.

7. Rahul Gond, **Akhilesh Rawat**, Mayank Baghoria, Bhanu Prakash, and Brajesh Rawat, "Fabrication and Characterization of Liquid Phase Exfoliated MoS_2 Nanosheet for Gas Sensing Application," *2023 IEEE Applied Sensing Conference (APSCON)*, Bengaluru, India, Jan. 2023.

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Research Interests:

- Dissipative quantum transport simulation.
- Quantum transport modeling of interface traps.
- TCAD Modeling of multigate devices at advanced technology nodes.