# Analysis and Design of Fault-Tolerant Scheme for DC-DC and DC-AC Power Conversion Stages in Solid-State Transformer

*by*

**Priya Singh Bhakar**


**DEPARTMENT OF ELECTRICAL ENGINEERING**

INDIAN INSTITUTE OF TECHNOLOGY ROPAR, INDIA

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**Priya Singh Bhakar**

*to the*


**DEPARTMENT OF ELECTRICAL ENGINEERING**

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**March, 2024**

Dedicated

to

**my family and friends**

# CERTIFICATE

This is to certify that the thesis entitled "***Analysis and Design of Fault-Tolerant Scheme for DC-DC and DC-AC Power Conversion Stages in Solid-State Transformer***", submitted by **Priya Singh Bhakar (2018eez0007)** for the award of the degree of Doctor of Philosophy of Indian Institute of Technology Ropar, is a record of bonafide research work carried out under my guidance and supervision. To the best of my knowledge and belief, the work presented in this thesis is original. It has not been submitted, either in part or full, for the award of any other degree, diploma, fellowship, associate or similar title of any university or institution.

In my (our) opinion, the thesis has reached the standard of fulfilling the requirements of the regulations relating to the degree.

**(Dr. J. Kalaiselvi)**
Assistant Professor

Department of Electrical Engineering
Indian Institute of Technology Ropar
Rupnagar, Punjab, India 140001

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**Priya Singh Bhakar**

406, Power Electronics Applications and Research Lab

JC Bose Block, Indian Institute of Technology Ropar

Rupnagar, Punjab, India 140001

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## ABSTRACT

Power electronic converters are extensively used in grids and microgrids. They can be combined with renewable energy sources for a variety of applications. Inverters, DC-DC converters, and rectifiers are frequently used in solid-state transformers (SST) and two-stage single-phase inverters or rectifiers. SSTs have progressed swiftly since they possess characteristics such as medium-frequency (MF) isolation stage, connection to medium voltage (MV), controllability, size and weight constraints, and improved power conversion efficiency. The SST and two-stage single-phase inverters are difficult to build and operate reliably since they include semiconductor components, gate drivers, cooling system, heat sink, control circuit, and other auxiliary circuits. As a result, the system's overall reliability is ensured by improving the reliability of each individual converter.

Dual active bridge converter (DAB) with galvanic isolation is a type of DC-DC converter that is commonly used in a variety of applications such as SST, electric car battery charger, UPS, fast-charging station, renewable energy system, traction application, etc. The continuous operation of the converter is vital in telecommunications, renewable energy systems, and machine-critical applications. The fault tolerance feature of the converter allows the network to be used even after unexpected failures. Semiconductor device failures in power converters are classified as either open-circuit (OC) or short-circuit (SC). SC faults are catastrophic and must be isolated as soon as possible. While the long-term current/voltage stress produced by OC failures can destroy switches and other related components. As a result, the objective of continuous converter operation and the rated output voltage demands the implementation of a fault-tolerant (FT) technique. An FT method to support the continuous operation of a DAB converter is proposed which includes a fault-tolerant capacitor ($C_f$) with appropriate control of duty and phase shift. Rated voltage is achieved in the post-fault correction for primary or secondary-side faults. Also, the transition from faulty condition to post-fault correction is smooth and within the defined limits.

A fault-tolerant converter is one that can continue to work even after a sudden failure. The self-reliant feature, on the other hand, refers to utilising existing hardware (no new power circuit) to achieve fault-tolerance for the respective fault. The self-reliance of a converter is determined by the type of converter, the location of the faulty switch, and the type of fault (OC/SC fault). A single primary switch failure results in half the pre-fault voltage and less power at the output. A secondary side SC failure results in minimal voltage and power, resulting in discontinuous converter operation. The SRC behaviour in the post-fault scenario differs when more than one switch fault occurs on any side. This thesis proposes the self-reliant characteristic for single and two

switches open/short-circuit fault on the primary and secondary side of SRC. A post-fault correction that maintains operating continuity and the rated output voltage at the load is presented for various fault conditions. A fault-tolerant capacitor is used in conjunction with control parameter variation to carry out post-fault correction for a single switch and different combinations of two switch faults. For more than one switch fault, the fault-tolerant and self-reliant feature of the converter is dependent on the combination of faulty switches.

The development in the field of smart transformer essentially requires a robust and reliable inverter. A fault-tolerant inverter keeps the converter running even after sudden failures, ensuring the converter's reliability against various faults. A semiconductor switch failure in an inverter can cause the majority of circuit faults, followed by electrolytic capacitor failures. Semiconductor failures can cause switch/leg short-circuits, open-circuits, and single/multiple switch faults. These issues necessitate the use of additional components to isolate and repair the damaged switch. Redundancy in form of switches, legs or modules in inverter functioning is frequently used for a variety of unique goals such as ripple compensation, fault tolerance, etc. Ultimately, the number of redundant components grows as a result of multiple goals being achieved within a unit. This thesis presents a method to maximize the use of the redundant leg. A new transition technique is designed to enhance the benefits of the redundant leg by properly transitioning the converter operation from pre-fault to post-fault correction (fault-tolerant mode). The redundant leg in the pre-fault situation serves to extend the lifespan of the DC-link capacitor by ensuring 0-100% compensation of the second harmonic ripple (SHR) in the DC-link current. The same leg is used to achieve fault tolerance in post-fault repair when adopting the suggested post-fault correction approach.

This thesis investigates several fault-tolerant techniques for DC-DC converters and inverters which can be used in solid-state transformers and DAB inverters. All fault-tolerant techniques are empirically tested and validated on the designed hardware prototypes.

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# Glossary

*Abbreviations*

| | |
|---|---|
| **AC** | Alternating Current |
| **DAB** | Dual active bridge |
| **DC** | Direct current |
| **DPS** | Dual-phase shift control |
| **EPS** | Extended-phase shift control |
| **FB** | Full-bridge |
| **FT** | Fault-tolerant |
| **HB** | Half-bridge |
| **IGBT** | Insulated Gate Bipolar Transistor |
| **LFT** | Low-frequency distribution transformer |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **PV** | Photovoltaic |
| **PWM** | Pulse Width Modulation |
| **RMS** | Root Mean Square |
| **SHR** | Second harmonic ripple |
| **Si** | Silicon |
| **SPS** | Single-phase shift control |
| **SPWM** | Sinusoidal Pulse Width Modulation |
| **SRC** | Series resonant converter |
| **SST** | Solid-state transformer |
| **SVPWM** | Space Vector Pulse Width Modulation |
| **TPS** | Triple-phase shift control |
| **ZCS** | Zero current switching |
| **ZVS** | Zero voltage switching |

# Chapter 1

# Introduction

## 1.1 General

Power electronic converters are commonly utilised in grids and microgrids. They can be used in conjunction with renewable energy sources [1, 2, 3, 4, 5, 6]. Power electronic converters like rectifiers, DC-DC converters, and inverters are frequently employed in solid-state transformers and two-stage single-phase inverters or rectifiers [2, 3, 4, 5]. A solid-state transformer, as shown in Fig. 1.1 can be utilized for traction applications, smart grids, and integrating renewable energy sources. The most common SST setup has three stages: an AC to DC converter, a DC-DC converter, and a DC to AC converter [5]. The AC to DC converter is a rectifier unit. The DC-DC converter is a galvanically isolated converter, such as a dual active bridge (DAB) or series resonant converter (SRC). The third stage is an inverter stage that performs DC to AC conversion. The DC-DC converter unit employs a medium frequency transformer, which reduces the system's volume and weight when compared to using a low-frequency distribution transformer (LFT) [6, 7]. SST preserves various other functionality over LFTs, including the use of semiconductor devices for voltage and current regulation, power flow management, fault current limiting, renewable energy source integration at the DC bus, etc [6]. As a result, the benefit of reduced volume and weight cannot be guaranteed without a careful design.

Two-stage single-phase rectifiers and inverters are often utilised in low to medium power conversions. Fig. 1.2 depicts the block diagram of a two-stage DC-AC converter. DAB inverters are widely used in a variety of applications [1, 8, 9]. They employ a dual active bridge converter as the DC-DC stage and an inverter as the DC-AC converter stage. Although the SST and two-stage single-phase inverters provide many additional features, their design, and reliability are challenging since they include semiconductor devices, gate drivers, cooling system, control circuit, and other auxiliary circuits [6]. The overall reliability in the system is assured by improving


**Figure 1.1:** Block diagram of SST.

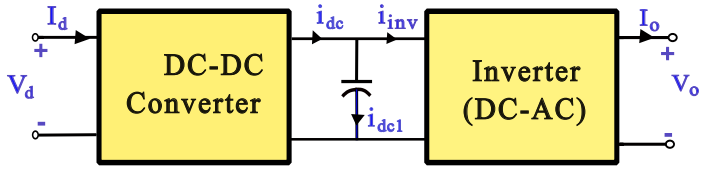



**Figure 1.2:** Block diagram of two-stage DC-DC converter and inverter.

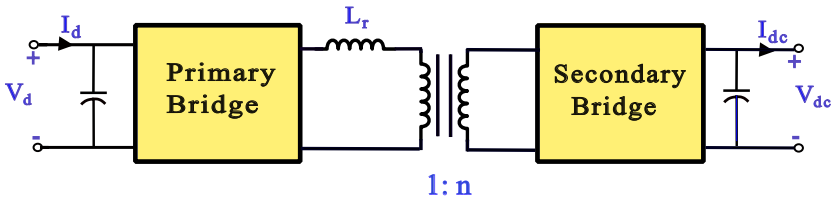



**Figure 1.3:** Block diagram of DAB converter.

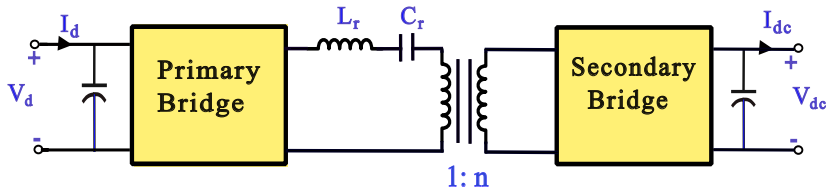



**Figure 1.4:** Block diagram of SRC.

the reliability of all the individual converters. Power converters are prone to malfunction since semiconductors account for the majority of faults [10]. Both SST and DAB inverters have a high number of semiconductors, affecting their reliability. In cases involving PV inverters, low reliability concerns may also arise. Such issues must be addressed because a PV array has a good life expectancy of about twenty years. However, a PV inverter could fail much earlier [3].

As illustrated in Fig. 1.3, the DAB converter consists of two full-bridges (8 switches), a high frequency (HF) transformer, an inductor, $L_r$, and two DC-link capacitors [1]. A DAB converter is capable of performing buck, boost, or same voltage operations. It has the benefits of realizing soft-switching i.e. zero voltage switching (ZVS) in switches, bidirectional power flow, and has a

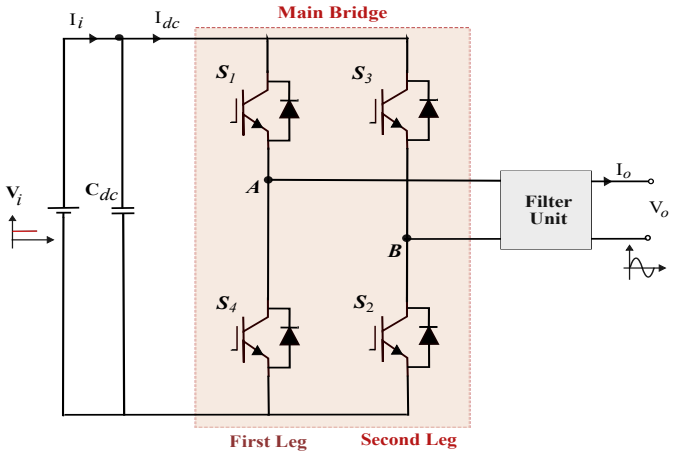



**Figure 1.5:** Circuit diagram of single-phase inverter.

symmetrical structure. The HF transformer offers the necessary galvanic isolation as well as voltage step up or step down. The DAB is a phase-shifted converter, hence the phase shift $\phi$ between the primary and secondary sides is crucial to power transmission and power flow direction.

The SRC is another type of DC-DC converter which uses an additional capacitor, $C_r$ as shown in Fig. 1.4. This capacitor along with the inductor, $L_r$ forms the resonant tank of the circuit. The SRC works most efficiently in the discontinuous conduction mode (DCM) [10]. This circuitry provides an additional feature of zero current switching (ZCS). The switching frequency ($f_s$) in this case is equal or slightly less than the resonant frequency ($f_r$) which is given by

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1.1}$$

The SRC can also work well in the open-loop system. The selection of $L_r$ and $C_r$ plays a vital role in the performance of the converter. The lifetime of various components and the efficiency of the converter is highly affected by the selection of these resonant components [10].

The inverter stage is the last stage of power conversion, as shown in Fig. 1.1 and 1.2. Single-phase inverters play a significant role in many applications as the DC-AC power conversion stage. A fundamental inverter stage shown in Fig. 1.5 consists of a DC-link capacitor at the input, an H-bridge, and an output filter that removes the switching frequency component from the high-frequency inverter output. High performance inverter power conversion systems are distinguished by high efficiency as a result of reduced switching and conduction losses. Through the use of a constant carrier switching frequency signal, the pulse width modulation (PWM) approach is appropriate to have low harmonic levels as well as low THD [11]. The two PWM configurations or schemes are: unipolar and bipolar PWM schemes.

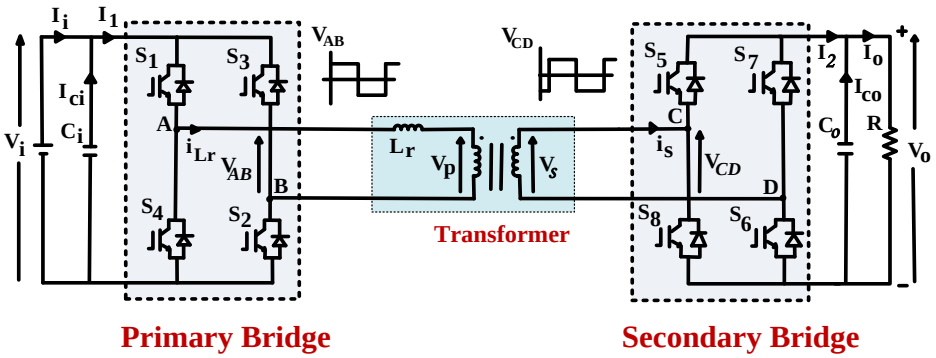



**Figure 1.6:** Circuit configuration of DAB converter.

### 1.1.1 Modulation Schemes for DAB and SRC

The modulation scheme followed in phase-shifted converters are:

1. Single-phase shift (SPS) control
2. Extended-phase shift (EPS) control
3. Dual-phase shift (DPS) control
4. Triple-phase shift (TPS) control

#### 1.1.1.1 SPS modulation

The most commonly used control scheme for the DAB converter shown in Fig. 1.6 is SPS control. According to Fig. 1.7(a), the phase-shift ratio between the switches of the primary bridge and the secondary bridge delivers the necessary power flow. The voltage across the $L_r$ changes as the phase shift ratio varies. This enables modifications to the power flow direction [1]. The SPS control technique may result in the flow of circulating current when the potential of the transformer is at two distinct levels. In this case, the converter cannot attain ZVS across the entire power range [12]. As a result, the efficiency is ultimately decreased when employing the SPS control scheme due to the higher power loss.

#### 1.1.1.2 EPS modulation

EPS is an improved version of SPS control. Both an inner and an outer phase shift are present. The phase shift between the primary bridge's diagonal switches is known as the inner phase shift ($Phi_i$). The voltages of the primary and secondary bridges are separated by an outer phase shift ($\phi$), as shown in Fig. 1.7(b). The inner phase shift decreases the circulating power and increases

the ZVS range, while the outer phase shift adjusts the amplitude and direction of the power flow [1, 12]. This control strategy aids in lowering current stress while enhancing the ZVS range [1].

#### 1.1.1.3 DPS modulation

Similar to the SPS and EPS control, the DPS control system retains an outer phase shift between the two bridges [13]. The DPS control differs from the EPS control in terms of the inner phase shift. Between the diagonal switches of both bridges, the same inner phase shift is offered. The DPS control offers the advantages of lowering the peak current, eliminating reactive power, and lowering output capacitance [1]. The application of the DPS control scheme also improves the efficiency of the converter. The pulse patterns of this scheme are shown in Fig. 1.7(c).

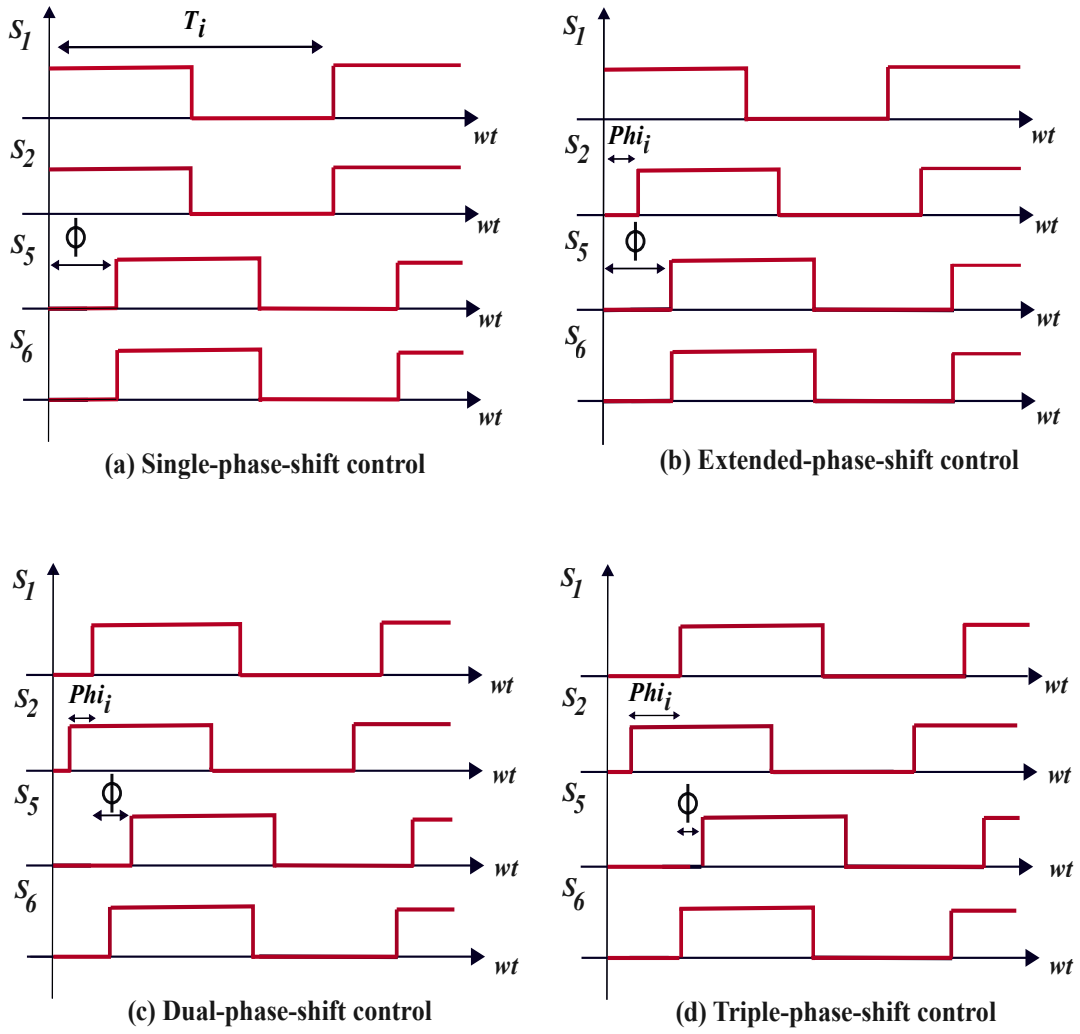



**Figure 1.7:** Different modulation schemes (a) SPS, (b) EPS, (c) DPS, and (d) TPS [1].

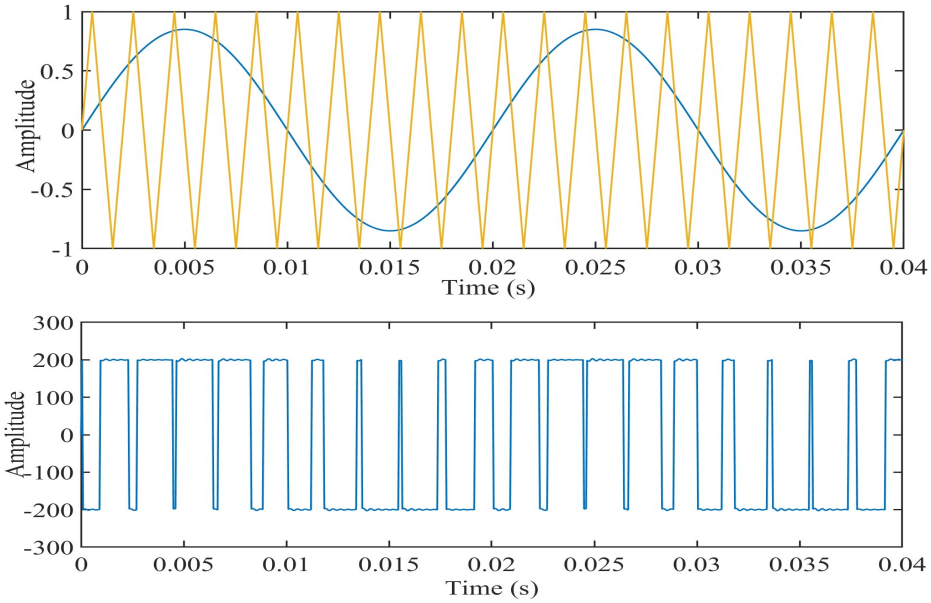



**Figure 1.8:** Bipolar pulse width modulation

#### 1.1.1.4 TPS modulation

In terms of the degree of freedom, the TPS control scheme is different from the DPS scheme. In this, the inner-phase shift between the diagonal switches in both bridges can be different [1]. The implementation of the TPS control is highly challenging because it requires three control degrees. The pulse pattern for TPS control is shown in Fig. 1.7(d).

### 1.1.2 Modulation Schemes for Single-phase Inverter

The modulation schemes used in single-phase inverters are:

1. **Bipolar SPWM:** In order to operate the devices in one leg, this approach compares the modulating signal, $V_m$ with a high-frequency triangle wave, $V_c$. The same pulses that were generated for switch $S_1$ are also provided for switch $S_2$ of leg 2. It is referred to as a bipolar PWM because the output inverter voltage shifts from a negative to a positive DC voltage, i.e., if $V_m \geq V_c$ : $V_{AB} = V_i$ and if $V_m < V_c$ : $V_{AB} = - V_i$ as shown in Fig. 1.5 and 1.8. Considering its ease of implementation, the bipolar SPWM is frequently employed in full-bridge inverters. The bipolar SPWM, however, needs a large filter.

2. **Unipolar SPWM:** This scheme compares the modulating signal $V_m$ with a high-frequency triangle wave to operate the devices in one leg. By comparing the $-V_m$ signal (180 degree shifted signal) with the same high-frequency triangle wave, the devices in the second leg are

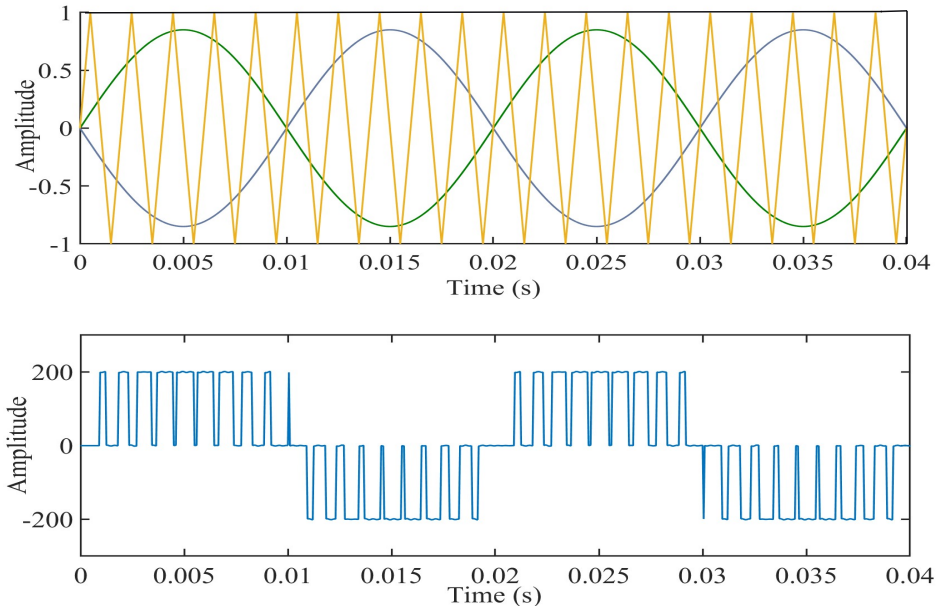



**Figure 1.9:** Unipolar pulse width modulation

operated. The unipolar PWM is capable of achieving three voltage levels: $V_i$, -$V_i$, and zero as shown in Fig. 1.9. According to [11], the unipolar switching approach only requires a small filter. As a result, the unipolar SPWM allows for the selection of the filter and has an improved waveform at the output.

The converters can function well with the above-mentioned schemes for DAB/SRC (SPS, EPS, DPS, and TPS) and single-phase inverters (unipolar and bipolar schemes). However, due to the large number of semiconductor devices employed in these converters, reliability remains a challenge. The issue arises when the converter develops a semiconductor fault and the operation is terminated as a consequence of the failure.

## 1.2 Faults in DC-DC (DAB/SRC) and DC-AC Power Converters: Problem Definition

The usage of power converters is widespread in numerous applications. A DC-DC converter can be used in electric vehicle charging stations, uninterruptible power supplies, data centers, etc., as explained in [2]. Due to the numerous advantages, including soft-switching (ZVS or ZCS), low EMI, superior power density, etc., the DAB and SRC are most frequently used in such applications. The requirements for current and voltage levels vary for each of these applications. For the vast majority of applications, each converter must adhere to strict specifications, which

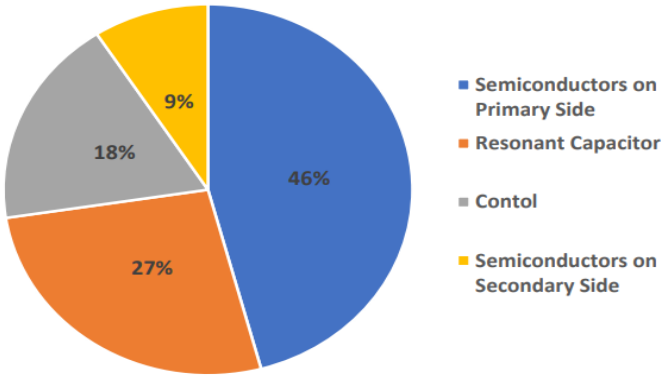



**Figure 1.10:** Most vulnerable devices to failure of the SRC/LLC [2]

typically include cost, reliability, and efficiency. The efficiency and reliability of the converter directly affect operating costs. The cost of maintenance decreases as reliability increases.

According to the survey provided in [2], regardless of the application or power level, the primary side semiconductor is identified as the largest source of converter failure, followed by the resonant capacitor. As demonstrated in Fig. 1.10, these two components account for 73% of all converter failures experienced in the industry. Over half of the damage to the converter is caused by a single defect in the semiconductor on the primary side, which mostly causes the device to short-circuit. The resonant capacitor, on the other hand, opens the circuit when there is a failure, preventing power from reaching the secondary side. Failures on the control platform are ranked third, while failures on the secondary side semiconductor are listed last [2].

The majority of incidents that result in semiconductor failure are linked to auxiliary circuit malfunction (such as gate driver, auxiliary power supply, cooling system, and control unit) or unexpected load behavior. As a result of those occurrences, semiconductors might fail due to overcurrent, overvoltage, or overtemperature [2]. Depending on the failure mechanisms, the semiconductors could enter one of two probable states: open circuit (OC) or short-circuit (SC). The OC fault is not catastrophic as the power transfer will be naturally interrupted. However, a power flow interruption is intolerable in some applications. The primary problem is the SC fault since it can seriously harm the power converter. The SC failure should receive more attention because it is both the most harmful fault type that should be avoided and the one that occurs most frequently in actual applications. Furthermore, a sudden change in the load impedance results in an overvoltage as well as an overcurrent on the capacitor. Typically, the majority of capacitor failures cause an OC situation [2].

For DC-AC conversion, PV inverters are used in PV systems to effectively transform the DC voltage for AC applications or to incorporate the output energy into electrical grids. Leading man-

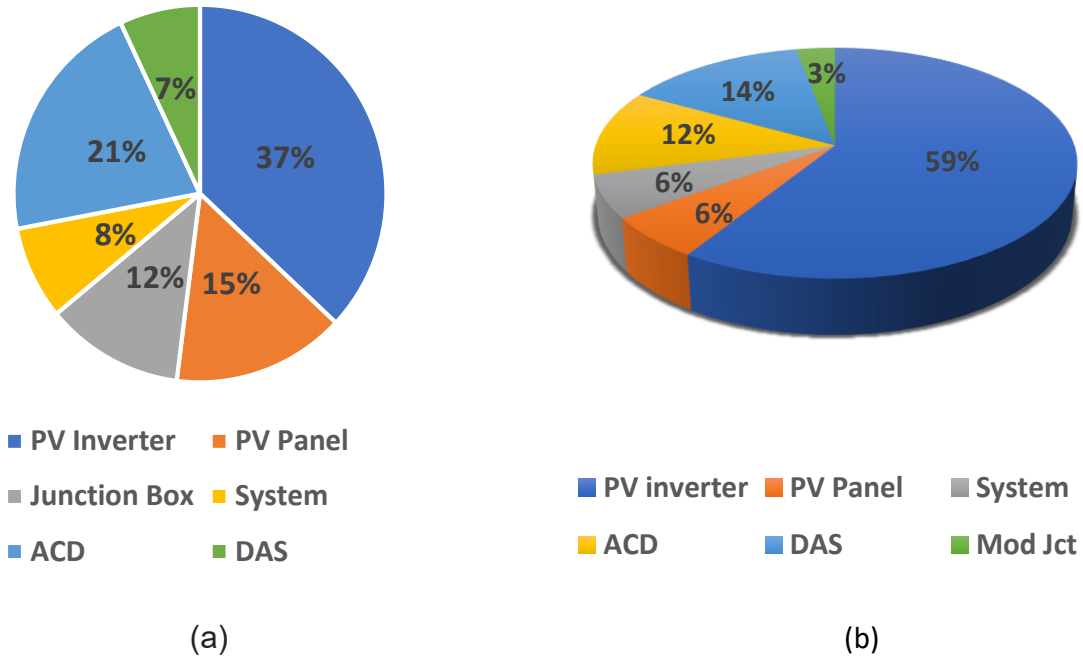



**Figure 1.11:** Unscheduled maintenance (a) events, and (b) associated cost [3].

ufacturers may presently offer a warranty on PV modules of over 20 years. However, in 2012, the average lifespan for PV inverters was roughly five years. Inverters may therefore need to be replaced three to five times over the course of a PV system, requiring additional investment, even if they only make up 10 to 20% of the system's initial cost. A survey on PV inverter failure was conducted in [3]. A total of 156 unscheduled maintenance incidents were noted for the Springerville systems over their operational lifespan from mid-2001 to 2006. The events are organized into many categories, such as data acquisition systems (DASs), inverters, junction boxes, PV arrays, etc., as illustrated in Fig. 1.11(a). The majority of these failures are observed in PV inverters. 1.11(b) gives a breakdown of unplanned incidents by component as a share of overall unplanned repair expenses. The inverters are responsible for the majority of the repair expenses. The field observations between 2001 and 2006 revealed that the PV inverters were in charge of 37% of unscheduled maintenance and 59% of the related expenses.

The reliability of power electronic systems and components is most strongly influenced by temperature. The three main stressors that either directly or indirectly cause failure in power electronic components are temperature, vibration, and humidity as indicated in Fig. 1.12. A highly reliable power electronics system is needed in many industrial applications since power interruptions are not acceptable. In actuality, a power converter failure results in higher operational

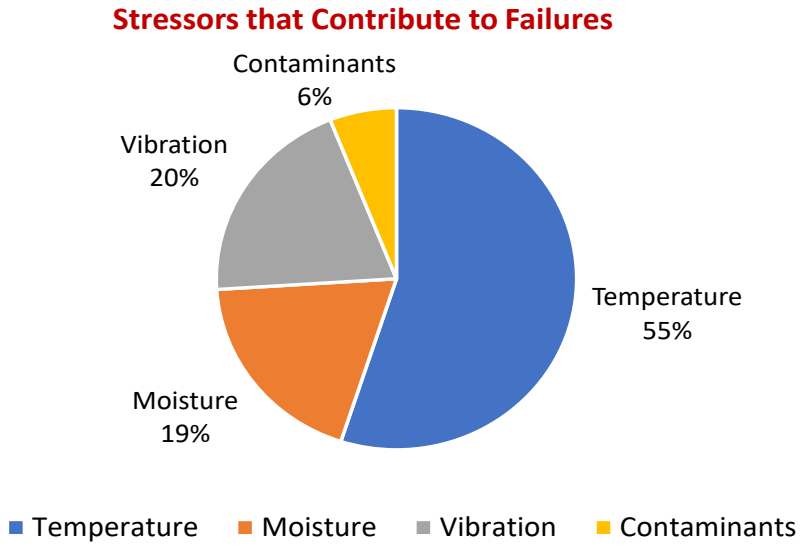



**Figure 1.12:** Factors that cause stress and contribute to failure [4].

costs due to the interruption of service, in addition to higher maintenance costs (to repair or replace the converter). Since power outages are expensive and needs to be avoided. Thus, the power electronic converter should have fault-tolerant feature.

## 1.3 Literature Review on the Fault Tolerance

The fault-tolerant property of power electronic converters has been researched in the literature. There are several fault-tolerant topologies available that target OC/SC or both types of failures. They will be discussed in the following sections.

### 1.3.1 Literature Survey on DC-DC Converter

The availability of the converter increases significantly by preventing the failure on the components and devices. The methods for avoiding failures in the converters are given in Fig. 1.13. Oversizing the most important components is the easiest solution. Although it raises the cost, this is typically done in the industry, especially when the cause of the failure is unknown. This method is ideal for the resonant capacitor in the case of LLC or SRC. Overstressing of the voltage or current caused by unforeseen operations, such as overload, SC, or start-up, is the main cause of the component's failure on a regular basis. The resulting open-circuit behavior of the damaged capacitor prevents power from flowing normally. As a result, oversizing the capacitor is a straightforward and low-cost solution. On the other hand, oversizing semiconductors is rarely used and is not advised. Since the price and the on-state resistance of the semiconductors are directly tied

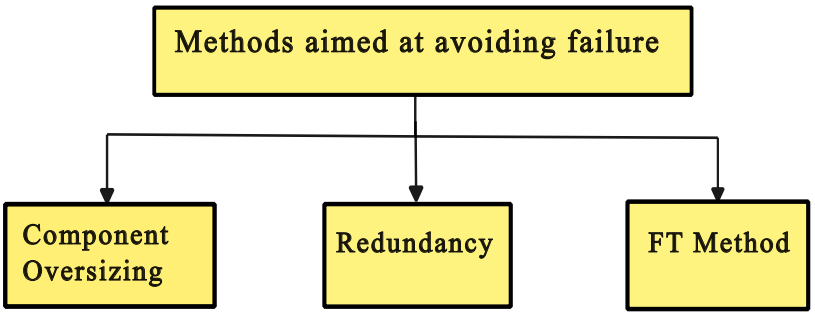



**Figure 1.13:** Methods for avoiding failures in the converter [2].

to the voltage rating of the device. Thus, the price and efficiency of the converter are affected by oversizing the semiconductors in voltage [2].

The most common technique for boosting converter availability is to utilize redundant converters. In many applications where power outages are unacceptable, such as data centers and distribution networks, redundancy has been used [14]. Redundancy can be classified into two types: stand-by and power-sharing. In standby redundancy, the auxiliary converter remains dormant during normal operation and is activated only if the main converter is damaged. In contrast, in power-sharing redundancy, all modules work simultaneously by sharing power, and when one of them fails, the other ones assume total power [2]. The redundancy strategy, regardless of the type, incurs additional costs because more converters are required. The replacement of the entire converter unit for a single device failure is therefore considered to be an expensive solution. If the redundancy is provided in terms of legs, at least one redundant leg is required on each side. In order to isolate the defective switch and connect the redundant legs, fuses and bidirectional switches are therefore needed on both sides, which further increases the price.

The FT feature helps to boost system availability and is a cost-effective option. Several FT approaches have been presented in the literature, and most of them contain substantial amounts of extra hardware, such as semiconductors/leg redundancy, switches/fuses, etc [15, 16, 17]. The incorporation of a redundant leg is the most frequently employed of the existing FT techniques described in the literature [16]. An extra leg is employed in place of the damaged leg in the event of a failure. The fuse is required to be placed in series with the semiconductors to isolate the faulty leg for the SC case. As a result, this method necessitates numerous additional components, significantly raising the cost. Also, the fuses connected in series with the primary devices dissipate power, reducing the converter's efficiency. Another FT technique for the FB DC-DC converter was shown in [18], which is reconfigured into an asymmetrical HB converter. The topology is

valid exclusively for OC failure. Furthermore, this technique also involves the use of fuses in conjunction with the primary devices, which reduces the efficiency of the converter.

A possible FT solution with minimal additional hardware and no effect on the converter's efficiency has been shown in [19]. This topology can be used to address any primary side semiconductor failure because it is resilient to OC or SC. The fundamental principle of this topology is to continue operating the converter as an HB-SRC rather than an FB-SRC, disconnecting the faulty leg. In actuality, the FB converter is converted to an HB converter by using the shorted switch as a circuit path. A reconfigurable rectifier is needed to maintain the output voltage since, following the reconfiguration, the output voltage declines to half of its value. The bidirectional configuration of the same fault-tolerant configuration is shown in [10, 20].

### 1.3.2 Fault-Tolerant Methods in Inverter

In isolated military-secured regions that are challenging to reach for maintenance, the usage of distributed generators, like solar photovoltaic (PV), is essential. In these applications, reliability of the system is prioritised over system cost [21]. However, the fragility of switching devices to failure has a major impact on the reliability of inverters in the PV system. Numerous fault-tolerant topologies that can operate even in the presence of device failure have been developed using additional switching devices. Device redundancy and leg redundancy are the two basic criteria used to categorise the existing fault-tolerant topologies for two-level inverters [16, 22]. Some multilevel inverters, such cascaded H-bridge multilevel inverters have modular redundancy [23, 24]. A decreased output voltage and power are a constraint of topologies based on device redundancy during fault-tolerant operation. In grid-connected PV applications, these topologies are therefore not utilised [25]. These restrictions are overcome by the redundant leg based topologies with the aid of one additional leg. When a device malfunctions, the redundant leg is used to replace the damaged leg, and the original arrangement is then restored [21]. However, these topologies are not economically viable since an additional switching mechanism is needed to switch the redundant leg to achieve the objective of fault tolerance. In [26], along with the redundant leg, it also makes use of four more TRIACs, $T_1$ through $T_4$ that additionally increase the cost. If the redundant leg is used effectively in both the pre-fault and post-fault conditions, the cost of employing redundant leg and TRIACs can be justified. Therefore, the best way to use the redundant leg must be investigated further in order to account for its cost in the system.

## 1.4 Motivation and Objectives

### 1.4.1 Motivation

According to the literature review in Section 1.3, semiconductor devices are more prone to failure than any other component in the circuit. By avoiding device and component failure, the availability of the converter is greatly increased. Oversizing the most crucial components, redundancy, and the FT method are the three techniques for preventing converter failures. Oversizing the capacitor is a low-cost solution. Contrarily, it is not advisable to oversize semiconductors. Utilizing redundant converters is the most popular method for increasing power converter availability. Regardless of the type, the redundancy technique results in higher costs since more converters are required. As a result, it is seen as a costly solution. In the event of a failure, an additional leg is used in place of the damaged one. In addition to this, it is necessary to connect the fuse in series with the semiconductors in order to isolate the faulty leg for SC fault cases. The FT method increases system availability and is a practical choice. Several FT techniques have been published in the literature, and the majority of them include a significant amount of additional hardware, including switches, fuses, and semiconductors/leg redundancy. Thus, a new FT method that uses less extra hardware is required.

The dual active bridge DC-DC converter does not have an inbuilt fault-tolerant capability since it does not possess a self-reliant feature for primary and secondary side faults. When an SC fault occurs on the primary side, a huge DC component can be observed. An excessive amount of DC current drawn from the source is not ideal since it can harm the primary side components if the related protection fails or activate the over current protection, thereby disconnecting the DAB from the source. The secondary side failures in the DAB can be expanded to a similar analysis, and in either instance, the DAB won't be able to continue operating. As a result, an appropriate post-fault correction mechanism is required to block the fault current in the DAB and adjust the topology to assure operation continuity.

SRC is another DC-DC converter that is frequently utilised in a variety of applications. The pre-fault and the post-fault condition for all the single switch and possible combinations of two switch fault needs to be analyzed for the implementation of post-fault correction. The role of the converter's self-reliant characteristic in attaining fault tolerance is not discussed in literature. Furthermore, the secondary side SC failure in bidirectional SRC is not thoroughly investigated in terms of current flow and converter behaviour in post-fault situations.

In single phase inverters, the redundant leg arrangement is commonly employed for fault tolerance. Additional connecting devices, such as TRIACs, are employed in the circuit reconfiguration. The redundant leg circuitry is solely utilised for post-fault correction, and it is not an integral part

of the circuitry in the healthy state. Although the reliability is improved, the redundant leg implementation is expensive since it necessitates an extra leg as well as additional connecting devices in the circuit. In other words, the benefits of using a redundant leg in the converter needs to be maximized to justify the volume, cost and the number of additional components used. As a result, a transition scheme is necessary in which the redundant leg in the pre-fault situation can be employed for a different objective. While in the post-fault condition it can be used for the fault correction. A common circuit design should be developed so that the redundant leg can be used in both pre-fault and post-fault correction within the same configuration.

### 1.4.2 Objective

In consideration of the aforementioned, the main objectives of the research conducted for this thesis are as follows:

1. Analysis and an understanding of converter performance in the event of a fault (pre-fault and post-fault condition without correction).

2. A post-fault correction method for dual active bridge DC-DC converters (DAB does not have built-in fault-tolerant capacity).

3. A post-fault correction approach for series resonant DC-DC converters for single switch fault.

4. Examining the applicability of the developed post-fault correction techniques on two switch faults arising in the converter.

5. Analysis and testing on the self-reliant characteristics of series resonant and dual active bridge converter.

6. Maximizing the usage of the redundant leg in the fault-tolerant single-phase inverter by:

    - designing a transition scheme to switch from the pre-fault condition to the post-fault correction.
    - designing the filter suitable for the pre-fault and the post-fault correction to achieve the desired voltage and current at the output in both the conditions.

## 1.5 Thesis Organization

This thesis studies the fault-tolerant approach for a DC-DC converter and a single-phase inverter appropriate for solid-state transformer and DAB inverter applications for semiconductor switch faults. The fault-tolerant approaches are intended to promote a continuous operation of the converter with rated voltage at the output even after a failure.

Finally, the thesis work is divided into six chapters. The following is a brief overview of each chapter:

### Chapter 1: Introduction

This chapter briefly introduces the different types of faults in the converter. This gives a broad overview of the extent of fault occurrence, unscheduled maintenance events and their cost, the source of stress distribution for failures, and the existing methods for post-fault correction. The motivation and goal of the research conducted for this thesis are finally outlined. It is followed by the organization of the thesis.

### Chapter 2: A New Fault-Tolerant Scheme for Switch Failures in Dual Active Bridge DC-DC Converter

Failures in active devices of the DAB can cause reduced terminal voltages or uncontrollable currents eventually leading to converter disconnection. These consequences cannot be corrected just by disabling the complementary switches of the faulty leg or reconfiguring the full-bridge DAB to a half-bridge DAB topology. In this chapter, a new fault-tolerant approach is proposed that works for both SC or OC failures in the active devices of the DAB DC-DC converter. Parallel combination of a fault-tolerant capacitor and a fast acting fuse, known as fault-tolerant unit, is connected in series with the primary as well as secondary of the transformer. Once the fault is detected, the output voltage is boosted to its pre-fault value through the incorporation of fault-tolerant capacitors along with variation in control parameters, ensuring the continuity of operation. The proposed post-fault reconfiguration scheme is validated experimentally using a 1 kW, 250V DAB prototype.

## Chapter 3: Fault-Tolerant and Self-Reliant Characteristic in Series Resonant Converter for Semiconductor Open/Short Circuit Faults

A single switch primary side failure in SRC results in half of the pre-fault voltage and lesser power at the output. While a secondary side SC fault results in negligible voltage and power leading to discontinuous converter operation. In this work, a post-fault correction is proposed which maintains the continuity of operation and the rated output voltage at the load for different fault conditions in SRC. A fault-tolerant capacitor is used along with the control parameter variation in the post-fault correction for a single switch fault. The analysis of the self-reliant feature and the post-fault correction is discussed and tested on a 1 kW, 250 V SRC prototype for different fault conditions.

## Chapter 4: Analysis of Two Switch Failures in Series Resonant and Dual Active Bridge Converters

A converter can also suffer from two switches undergoing failure either on the same side or alternate side of the converter. For more than one switch fault on any side, the SRC/DAB converter behavior in the post-fault condition is different. The self-reliant feature of the FT converter depends upon different combinations of switch faults which can occur simultaneously or one after the other on the same/different sides of the converter. Thus, the proposed scheme in Chapter 2 and 3 is further analyzed for two switch faults for its applicability. This work presents the analysis and effects of two switch faults in DAB and SRC.

## Chapter 5: A Fault-Tolerant Single-Phase Inverter with Extended Electrolytic Capacitor Lifetime

The single-phase inverters are frequently employed in many different applications. Redundancy in form of switches, legs or modules in inverter functioning is frequently used for a variety of unique goals such as ripple compensation, fault tolerance, etc. Ultimately, the number of redundant components grows as a result of multiple goals being achieved within a unit. In this work, a transition scheme is developed in which a redundant leg in the pre-fault situation ensures 0% to 100% compensation of the SHR in the DC-link current, extending the lifespan of the dc-link capacitor. While using the same leg, the proposed post-fault correction scheme is used to achieve the fault tolerance. The converter operation is safely switched from one mode to another by

following a sequence of events in the preparation stage. The proposed reconfiguration scheme is tested on a single-phase inverter for different SC and OC fault conditions.

## Chapter 6: Conclusion

This chapter concludes by summarising the key findings of the research presented in this thesis and outlining a few potential directions for future study.

# Chapter 2

# A New Fault-Tolerant Scheme for Switch Failures in Dual Active Bridge DC-DC Converter

## 2.1 Introduction

The contemporary evolution of technology in the field of power converters has made extraordinary attempts in handling grids and microgrids [6, 27, 28]. DAB with galvanic isolation is a frequently used DC-DC converter in a variety of applications like smart transformer (or solid-state transformer or SST) [29, 30], battery charger in the electric vehicle, UPS [1], fast-charging station, renewable energy system, traction application [31, 32], etc. DAB is widely used for high voltage/power applications, playing a crucial role in multilevel converters such as power electronic transformer or SST. In telecommunication, renewable energy systems and machine-critical applications, the uninterrupted operation of the converter is extremely important. The accessibility of the network even after sudden failures constitute the fault-tolerant feature of the converter [33, 34].

Failures of semiconductor devices in the power converters are classified OC and SC fault [35, 36, 37]. These faults can occur due to bond wire lift-off or rupture, malfunctioning of the driver unit, failure of the cooling system, control unit and auxiliary circuit failures leading to over current, over voltage and temperature [2]. SC faults are catastrophic in nature and must be isolated immediately when detected, and off-the-shelf gate drives are already equipped with the SC protection. Unlike SC faults, OC faults are not catastrophic and the converter can be operational even after the fault. However, the prolonged current/voltage stress due to OC faults can damage the switches and other connected components in the long term.

Several fault-tolerant schemes for the DAB DC-DC converter have been discussed in the literature [16, 38, 39, 40, 41, 42]. Initially, reliability of the converter was ensured by using a redundant leg with multiple fuses to isolate the faulty leg [16]. Using redundancy for the fault-tolerant operation requires additional components to disconnect the faulty device and connect the redundant component in the circuit. A separate fault isolation unit is also needed to isolate the damaged switch [16]. This was later improved through hardware reduction in [38, 39, 40] as the use of an extra leg would increase the cost of the system. The concept of using a redundant winding is also explained in [38] where fuses connected in series are used to isolate the fault, reducing the efficiency while providing fault-tolerant feature for limited faults. In [38], the use of plenty of fuses, winding, and relays increases the cost of the overall system. The fault-tolerant method used in [38] provides correction for primary side faults only. A fault-tolerant method for primary and secondary side open circuit faults in the converter is discussed in [39]. It gives an analysis on different OC fault conditions in the converter. Also, this method is able to achieve the fault-tolerance for a certain load carrying capacity (lesser than the rated power) only. The switch short-circuit fault correction for DAB is missing in [39]. Another fault-tolerant method consisting of dual loop control in series resonant dual active bridge converter is explained in [40]. The inner loop controls the envelope of high frequency current while the outer loop regulate the DC voltage. The effects on converter operation and the diagnosis of open-circuit failure in DAB is discussed in [41]. In this, the inductor current and voltages at different points are analyzed for the fault detection and location. Another OC fault diagnosis strategy is given in [42]. This OC fault detection method is carried out by using average values of the voltage to identify the faulty devices.

SC faults are catastrophic and can damage all cascaded components if not rectified on time [19, 20]. The SC fault-tolerant methods using a voltage doubler configuration are discussed in [10, 19, 20]. When an OC/SC fault occurs on the primary side, it is converted to a half-bridge whereas the secondary side is reconfigured to a voltage doubler configuration. This fault-tolerant method for unidirectional power flow is discussed in [19] which uses 1 switch and 1 DC capacitor as extra components. It is applicable for primary side fault correction only. While the bidirectional version is presented in [20]. Additional components used in [20] are 4 switches and 2 DC capacitors to achieve the primary and secondary side fault tolerance in SRC. These methods which are used for DC-DC converters in literature [10, 19, 20] are not suitable for their application in DAB converter. Although the fault-tolerant methods for OC faults are discussed in [16, 38, 39, 40], the fault-tolerant feature for SC faults on primary as well as secondary side (with and without correction) of DAB is unexplored in literature. Hence this work focuses typically on the analysis and combined fault-tolerant method for SC as well as OC failure in the single unit of dual active bridge converter. The objective of continuous converter operation and the rated output voltage is retained by post

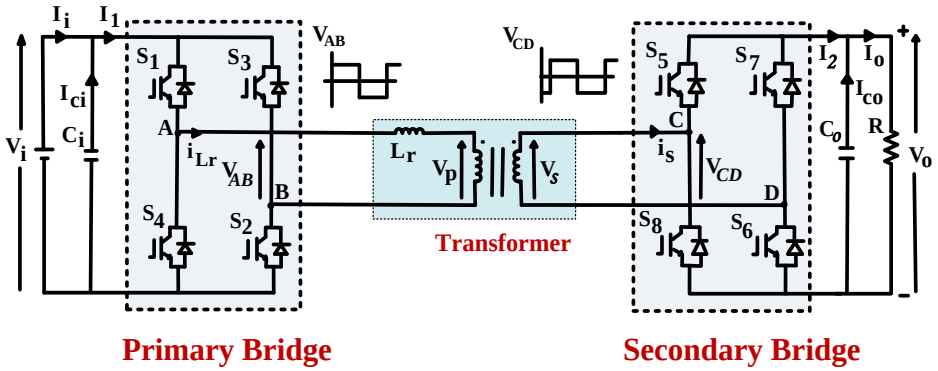



**Figure 2.1:** Circuit configuration of DAB converter.

fault reconfiguration consisting of fault-tolerant capacitor ($C_f$) with appropriate control of duty and phase shift. Also, the proposed work emphasizes on fulfilling the objective with minimum hardware compared to other reconfiguration methods in literature [16, 19, 20, 38, 39, 40, 41, 42].

## 2.2 Dual Active Bridge DC-DC Converter

The circuit configuration of DAB DC-DC converter is illustrated in Fig. 2.1. The DAB consists of a primary bridge formed by the active devices $S_1$ to $S_4$ and a secondary bridge formed using the active devices $S_5$ to $S_8$. Transformer connected between the primary and secondary bridges provides necessary voltage gain between the input, $V_i$ and the output, $V_o$. Each active device of the DAB is operated at a fixed 50% duty cycle to generate the two pole-to-pole voltage i.e., $V_{AB}$ and $V_{CD}$. Power transfer, $P$ between the two bridges is regulated by controlling the phase shift/delay, $\phi$ between $V_{AB}$ and $V_{CD}$ as [1],

$$P = \frac{nV_iV_o\phi(\pi-\phi)}{2\pi^2 f_s L_r} \tag{2.1}$$

where $f_s$ is the switching frequency (in Hertz), $L_r$ (external series inductor of DAB) and $n$ is the turns ratio of the transformer [43].

Semiconductor devices on the primary and secondary sides are the major sources of failure in the power converters [36]. Therefore, operation of the DAB is studied considering various active device failures in the next section.

### 2.2.1 Operation of the DAB with Faults

The short-circuit failures in active devices are known to cause catastrophic consequences, such as SC of the DC terminals either on source-side or load-side depending on the location of the failure,

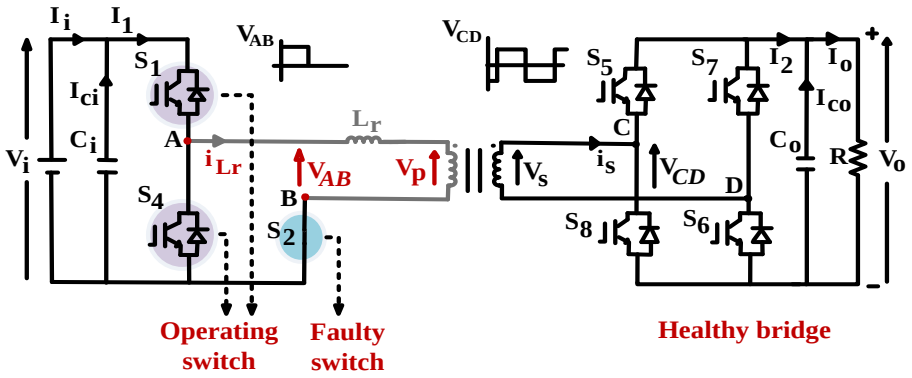



**Figure 2.2:** Circuit operation during SC failure in $S_2$ of the DAB.

**Table 2.1:** Conducting switches under various short-circuit fault cases

| Faulty Location | $V_{AB}$ | Conducting switches |
|---|---|---|
| (i) $S_1$ (ii) $S_2$ | [$V_i$, 0] | (i) $S_1$, $S_2$, $S_3$, $S_5$- $S_8$ (ii) $S_1$, $S_2$, $S_4$, $S_5$- $S_8$ |
| (iii) $S_3$ (iv) $S_4$ | [0, -$V_i$] | (iii) $S_1$, $S_3$, $S_4$, $S_5$- $S_8$ (iv) $S_2$, $S_3$, $S_4$, $S_5$- $S_8$ |
| (v) $S_5$ (vi) $S_6$ | [$V_i$, -$V_i$] | (v) $S_1$- $S_4$, $S_5$, $S_6$, $S_7$ (vi) $S_1$- $S_4$, $S_5$, $S_6$, $S_8$ |
| (vii) $S_7$ (viii) $S_8$ | [$V_i$, -$V_i$] | (vii) $S_1$- $S_4$, $S_5$, $S_7$, $S_8$ (viii) $S_1$- $S_4$, $S_6$, $S_7$, $S_8$ |

and eventually damaging all the connected components. Despite the failures, the continuous operation of the converter is ensured in two ways, (i) operation through redundancy, and (ii) topology reduction. In the former case, either leg-wise or bridge-wise redundancy is provided to replace the faulty leg/bridge during the post-fault operation [2, 16]. Considering the power density and cost constraints in applications such as solid-state transformer (SST), the topology reduction during post-fault operation of DAB is investigated.

The circuit condition for a SC failure in $S_2$ of the DAB is shown in Fig. 2.2. With an installed SC protection mechanism such as desaturation detection circuit in the gate driver, the gating signals to the active devices in the faulty leg can be blocked once a SC fault is detected. When the gating signal to $S_3$ is blocked, the primary bridge of the DAB acts as a half-bridge (HB) and could synthesize either $V_i$ or 0 across the transformer primary as listed in Table 2.1.

The fourier series expression of the fundamental component of $V_{AB}$ in the post-fault condition is given as,

$$V_{AB} = V_i D_1 + \frac{2V_i}{2\pi}[sin(2\pi D_1)cos(\omega t) + (1 - cos(2\pi D_1))sin(\omega t)] \tag{2.2}$$

where $D_1$ is the duty cycle of the active devices on the primary side (with respect to switch $S_1$), $\omega$ is the angular frequency, and $T_s$ is the duration of one cycle.

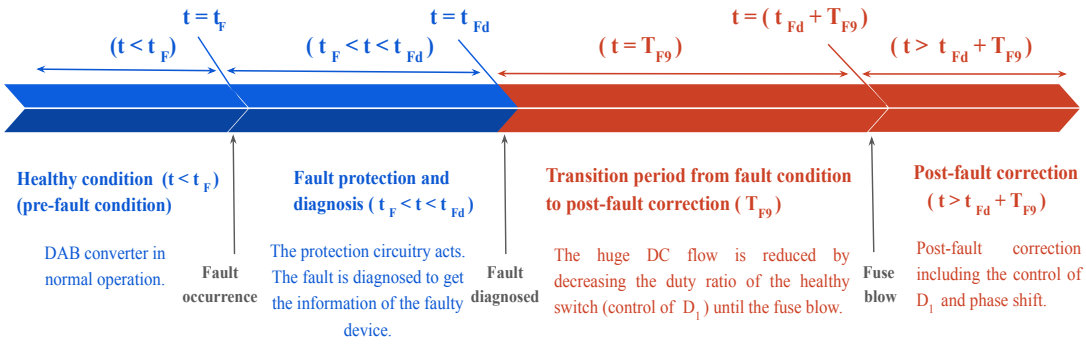



**Figure 2.3:** Timeline diagram of the proposed post-fault correction.

For $D_1$= 0.5, the DC component in $V_{AB}$ is 0.5 $V_i$ as seen from (2.2). Say, $R_{AB}$ is the total resistance offered by $L_r$ (external series inductor of DAB, if connected) and the transformer primary winding, the DC component in the primary current, $I_{Lr\_dc}$ is given as,

$$I_{Lr\_dc} = \frac{V_i D_1}{R_{AB}}. \tag{2.3}$$

A tremendous amount of DC current drawn from the source (as given by (2.3)) is not desirable, as it can damage the components on the primary side if the associated protection fails or trigger the over current protection effectively isolating the DAB from source. A similar analysis can be extended to the secondary side failures in the DAB and in either cases, the DAB will not be able to continue its operation.

From the above analysis, it can be understood that merely blocking the gating signals of the active devices in the faulty leg does not prevent the fault current to grow in the corresponding bridge of the DAB and trigger cascading failures. Thus, a suitable post-fault correction mechanism is needed to block the fault current in the DAB and modify the topology to ensure the continuity of the operation.

## 2.3 Proposed fault-tolerant DAB

The implementation of the proposed post-fault correction scheme for DAB is shown in Fig. 2.3. To guarantee a satisfactory performance of the DAB during the post-fault stage, two components are included in the proposed scheme: (i) fault-tolerant units as hardware modification, and (ii) post-fault correction unit as control modification. As illustrated in the Fig. 2.4, a parallel combination of fault-tolerant capacitor, $C_{f1}$ and fast acting fuse, $F_9$ is used as a fault-tolerant unit in the primary of the DAB. A similar fault-tolerant unit (parallel combination of $C_{f2}$ and $F_{10}$) is connected in series

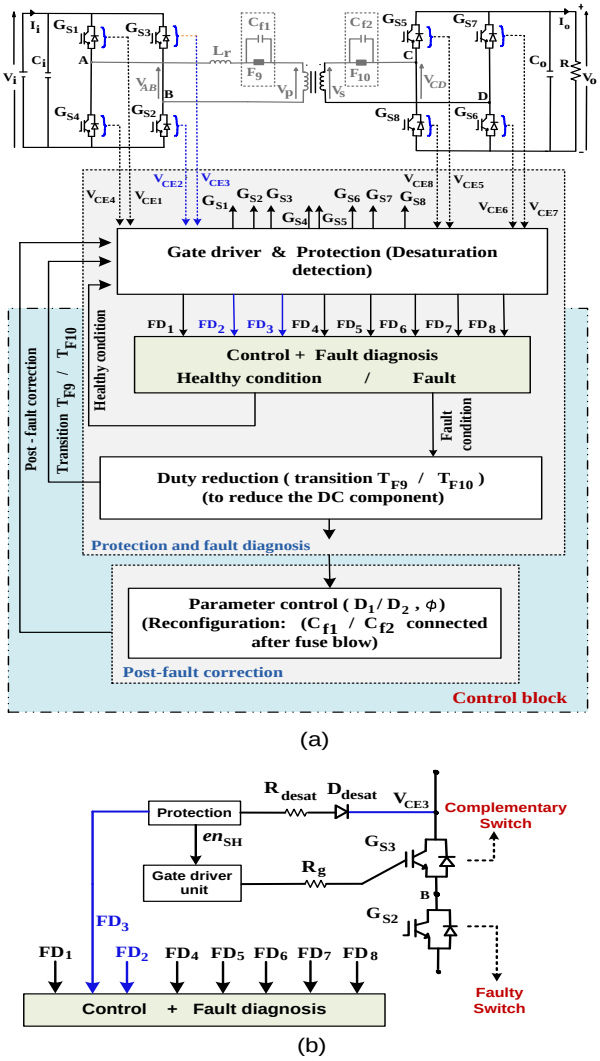
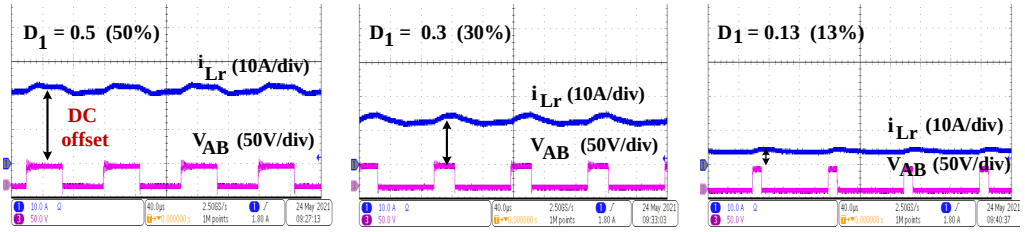



**Figure 2.4:** (a) Implementation of the proposed post-fault correction scheme for DAB, and (b) fault detection algorithm.

with the secondary of the transformer. Before executing the post-fault correction, a successful implementation of the fault detection and diagnosis scheme is important. Several fault diagnosis methods are available in literature [19], [37], [38], [41, 42], [44].

The existing methods like desaturation detection, current mirror method, protection by gate voltage limiting, etc can be used for detecting the switch failure [19, 44]. Here, the conventional desaturation detection is used to detect the SC failures in the active devices [19, 44]. Once the fault is detected, the post-fault correction unit is introduced to modify the control parameters, $D_1/D_2$ and $\phi$ to limit the fault current as mentioned in Fig. 2.4(a).

The sequence of events during the operation of the DAB with the proposed scheme is shown in Fig. 2.3. Before $t_F$, the DAB is operating in healthy conditions. Fault initiated at $t = t_F$ is




(a) (b) (c)

**Figure 2.5:** Variation of DC offset in inductor current at duty ratio (a) 50 %, (b) 30 %, and (c) 13 %.

detected and located at $t = t_{Fd}$, and the fault detection time is algorithm specific. When a SC fault occurs in any of the active device, the voltage across the complementary switch increases from a low saturation value to the DC voltage when the corresponding gate signal is still high. This unexpected behaviour triggers the corresponding fault detection flags, $FD$ (indicated in Fig. 2.4(b)), consequently deactivating the gating signal for the switch in the leg. Once the fault is located at $t_{Fd}$, the post-fault correction unit reduces the $D_1/D_2$ such that RMS current is sufficiently high to open $F_9/F_{10}$ but not high enough to create the cascading failures.

### 2.3.1 Short-Circuit Faults

The proposed fault-tolerant operation of the DAB is addressed separately for primary-side SC faults and secondary-side SC faults.

#### 2.3.1.1 Primary-Side Failures

A SC fault in $S_2$ is considered for this analysis. With the failure in $S_2$, abnormal increase in the voltage across $S_3$ even if the $G_{S3}$ is high triggers the corresponding fault flag $FD_2$ and $FD_3$. As a result, the controller deactivates the gating signals to $S_2$ and $S_3$, effectively forming a half-bridge (HB) on the primary side of the DAB as shown in Fig. 2.2. The HB formation on the primary-side results in a DC in the primary circuit. This current magnitude is proportional to the DC component in $V_{AB}$ which can be controlled by changing $D_1$. Therefore, when a SC fault is located at t = $t_{Fd}$, the duty cycle of $S_1$ is reduced to limit the DC offsets in $V_{AB}$ and $i_{Lr}$ as shown in Fig. 2.5. The reduced duty cycle is applied until fuse $F_9$ blows at t = $t_{Fd} + T_{F9}$. Here, $F_9$ allows the bidirectional current flow and does not hamper with the healthy operation of the DAB converter. The following are to be considered while selecting a suitable fuse:

- A fast-acting fuse needs to be employed to ensure a quick and seamless transition from faulty operation to the post-fault stage [44, 45]. Fast acting fuses have been researched for fault-tolerant DC-DC converters and inverters for isolation of the faulty leg [2, 16, 38].

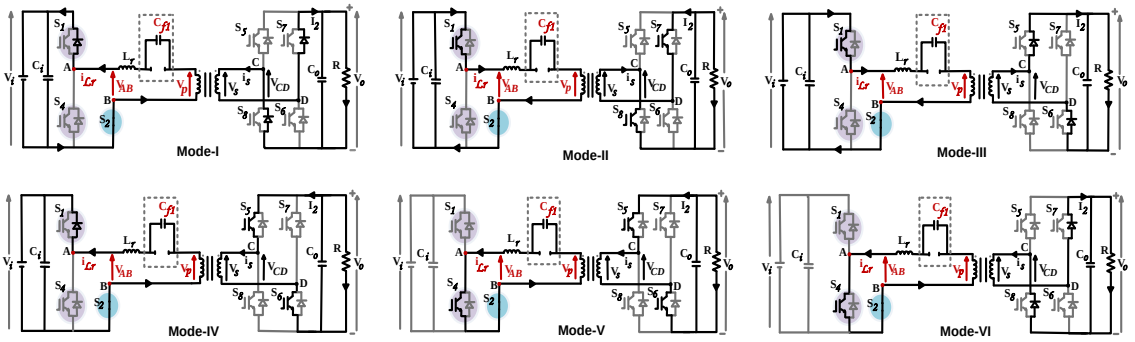



**Figure 2.6:** Mode analysis of current flow in post-fault correction of $S_2$ short-circuit fault in DAB.

- The fuse must be designed to carry 2 times the rated current to avoid the malfunctioning of the proposed topology during different operating conditions.

During $T_{F9}$, i.e., the transition between fault operation and the post-fault correction stage, the modified duty $D_{1(transition)}$ is applied to the HB such that the DC offset in $i_{Lr}$ is within the limits. The $D_{1(transition)}$ is calculated as,

$$D_{1(transition)} = \frac{i_{Lr(transition)} R_{AB}}{V_i}. \tag{2.4}$$

Here, $i_{Lr(transition)}$ is the current maintained during the transition period. This current can be regulated by adjusting the duty ratio $D_{1(transition)}$. The value of $i_{Lr(transition)}$ is completely a designer's choice thus, it can be adjusted according to the prototype. The required value of $D_{1(transition)}$ is selected from (2.4) to disconnect the fuse $F_9$ and implement the post-fault correction. At $t = t_{FD} + T_{F9}$, $C_{f1}$ automatically gets connected in series with the transformer as shown in Fig. 2.6. The role of $C_{f1}$ is to block an unacceptable DC component in $i_{Lr}$ and support the boosting of voltage at the output.

The modes of current flow during the post-fault stage are shown in Fig. 2.6 and 2.7. Fig. 2.7(a)-(c) shows the pulse pattern of switches during various conditions namely, healthy condition, transition $T_{F9}$, and the post-fault correction. The duty of primary side switches in healthy condition is 50%, $D_{1(transition)}$ during the transition $T_{F9}$ and $D_{1(correction)}$ during the post-fault correction. In the proposed correction, when the $S_1$ is operated, $V_{AB} = V_i$ (mode I-IV). While in mode-V-VI, the switch $S_4$ is operated with $V_{AB}$= 0.

Mode I: diode $d_1$ and switch $S_2$ conducts the negative flow of the current to ensure the zero-voltage switching (ZVS) during switch turn-on. Diodes $d_7$ and $d_8$ conduct on the secondary side.

Mode II: When the current becomes positive, the $S_1$ and $S_2$ connects supply to the transformer primary. In this mode, the capacitor $C_{f1}$ starts charging from a minimum value.

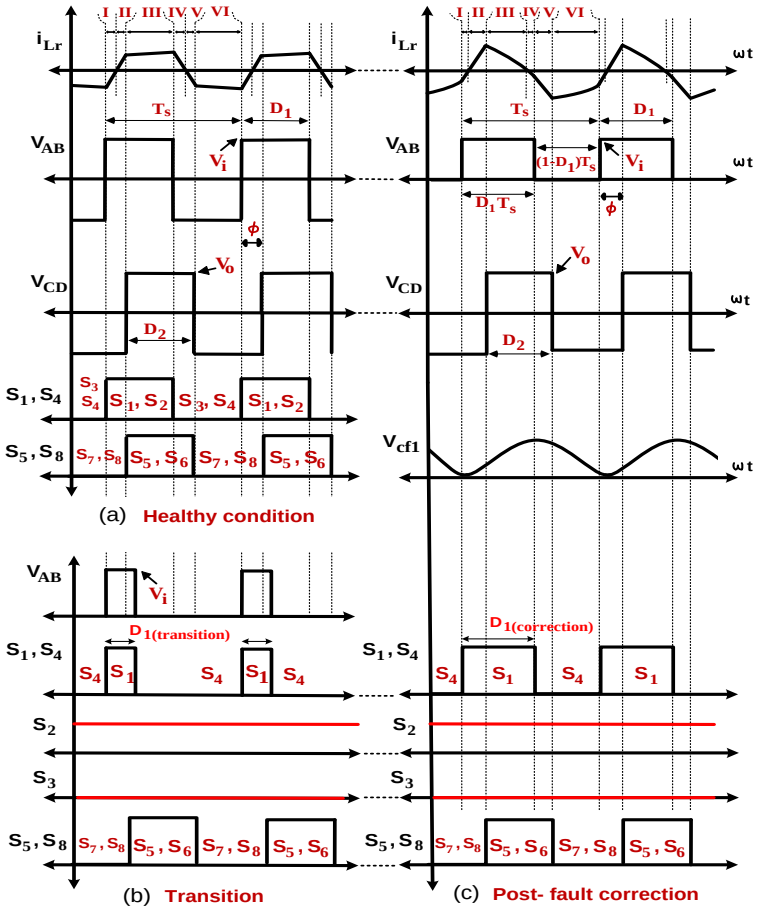



**Figure 2.7:** Voltage and current profiles in various modes under (a) healthy condition, (b) transition $T_{F9}$, and (c) post fault correction for $S_2$ short-circuit fault in DAB.

Mode III: This mode is followed after a phase shift $\phi$ between the two bridges. Pulses are changed such that $d_5$ and $d_6$ conducts the positive current flow allowing $C_{f1}$ to charge up to the peak value.

Mode IV: Diode $d_1$ and switch $S_2$ conducts the negative current for a small duration with $V_{AB}$= $V_i$ while the switch $S_5$ and $S_6$ conducts on the secondary side.

Mode V: When the switch $S_4$ is operated, the supply is disconnected from the transformer primary. Thus, the capacitor $C_{f1}$ discharges.

Mode VI: When the pulses are changed to $S_7$ and $S_8$, the diodes $d_7$ and $d_8$ conducts on the secondary side. While $C_{f1}$ discharges on the primary side through the switch $S_4$.

The power transferred between the primary and the secondary bridge as per [43] is calculated by,

$$P_{CD} = \mathfrak{Re}(V_{CD} i_{Lr}^*) = \mathfrak{Re}(\frac{V_{CD}(V_{AB} - V_{CD})^*}{Z^*}) \tag{2.5}$$

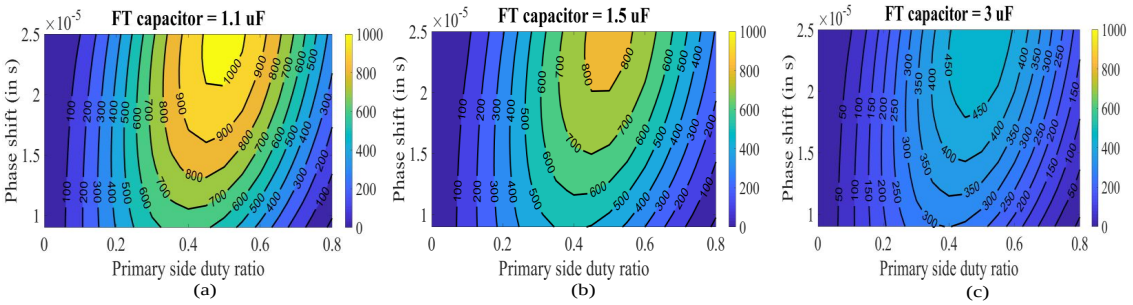



**Figure 2.8:** Power flow between the two bridges with a variation in duty ratio and the phase shift at (a) $C_{f1}$ = 1.1 $\mu$F, (b) $C_{f1}$ = 1.5 $\mu$F, and (c) $C_{f1}$ = 3 $\mu$F for $S_2$ SC fault correction.

where Z is the impedance given by,

$$Z = j(\frac{\omega^2 L_r C_{f1} - 1}{\omega C_{f1}}). \tag{2.6}$$

The fourier series expression of the fundamental component of $V_{AB}$ (from Fig. 2.7(c)) is given by,

$$V_{AB} = V_i D_1 + \frac{V_i}{T_s}\frac{(1 - e^{-j\omega D_1 T_s})}{j\omega} e^{j\omega t}. \tag{2.7}$$

Here, the magnitude of $V_{AB}$ is given by the $|V_{AB}|$ or abs($V_{AB}$). Also, the fundamental component of $V_{CD}$ for a full-bridge (FB) on the secondary side is given by,

$$V_{CD} = \frac{V_o}{2\pi}[-(2sin(\omega\phi_s) - 2sin(f)) + j(-2cos(\omega\phi_s) + 2cos(f))]e^{j\omega t} \tag{2.8}$$

where $f = \frac{\omega T_s}{2} + \omega\phi_s$. Here, $\phi_s$ is the phase delay (in seconds) between the two bridges. Using (2.7) and (2.8) in (2.5), the power transferred between the two bridges is calculated as,

$$\begin{aligned} P_{CD} = \frac{M}{2}[\frac{V_o}{2\pi}(2sin(\omega\phi_s) - 2sin(f))][\frac{V_i}{2\pi}(1 - cos(2\pi D_1)) + \frac{V_o}{2\pi}(-2cos(\omega\phi_s) + 2cos(f))] - \\ \frac{M}{2}[\frac{V_o}{2\pi}(-2cos(\omega\phi_s) + 2cos(f))][\frac{V_i}{2\pi}(sin(2\pi D_1)) + \frac{V_o}{2\pi}(2sin(\omega\phi_s) - 2sin(f))] \end{aligned} \tag{2.9}$$

where M= $\frac{\omega C_{f1}}{\omega^2 L_r C_{f1} - 1}$. Here, the power transferred between the two bridges is a function of $D_1$, $\phi_s$ and $C_{f1}$ for a fixed value of $L_r$ as seen in (2.9).

The current rating of the components and the maximum power transferred between the bridges is decided by the selection of $C_{f1}$ as shown in Fig. 2.8 and 2.9. Several factors that affect the selection of $C_{f1}$ are,

1. Maximum power flow:- The pre-fault power flow in the post-fault correction is maintained only when $C_{f1}$ is designed keeping the resonant frequency ($f_r$) of the tank circuit very close

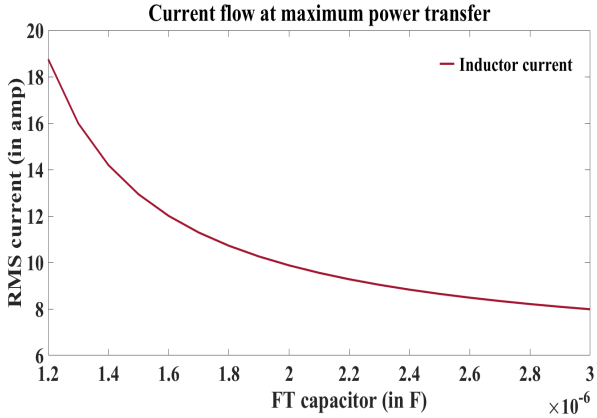



**Figure 2.9:** Current flow through the windings for different values of $C_{f1}$ in the post-fault correction.

to the $f_s$ as shown in Fig. 2.8(a). In this case, the current flow through the components is very high as shown in Fig. 2.9. Thus, the switches and other components needs to be designed for three (or more) times of the pre-fault current value. On operating away from the $f_r$, the maximum power transferred to the load reduces as shown in Fig. 2.8(b) thus, the current flow through the components is lesser (Fig. 2.9). When the $f_r$ is far away from $f_s$, the maximum power flow reduces further as shown in Fig. 2.8(c) which is undesirable. Thus, the $C_{f1}$ is selected such that the current flow through the windings is twice the pre-fault value, without a large reduction in power transferred to the load.

2. Peak value of the capacitor voltage:- When $D_1$ increases, $C_{f1}$ should be capable of blocking the increased value of the DC component ($V_i D_1$). Also, $C_{f1}$ is selected such that the peak voltage across the capacitor should not largely exceed the rated voltage. For a smaller value of capacitor (at $f_r$ closer to $f_s$), the peak voltage across $C_{f1}$ increases beyond the rated input voltage. Thus, the desired voltage (rated voltage) across the capacitor is given by,

$$V_{cf1} = V_i D_1 + \frac{V_i}{2} sin(\omega t - 90^\circ - \frac{\phi}{4}). \tag{2.10}$$

In the proposed post-fault correction, the component ratings are selected by considering the constraints like current flow through the windings, peak value of the capacitor voltage, and maximum power transferred to the load. The values of $C_{f1}$ and $\phi$ are selected such that the maximum $i_{Lr}$ is twice the rated value (on formation of the half-bridge). Since the power flow increases with the increase in $\phi$ (upto 90°), the circulating current through the windings also increases for $\phi$ very closer to 90° as shown in Fig. 2.8(b). Thus, $\phi$ is selected as 75° (lesser than 90°) and $D_1$ is selected as 0.53 (closer to $D_1$ = 0.5) according to the maximum power area shown in Fig. 2.8(b).

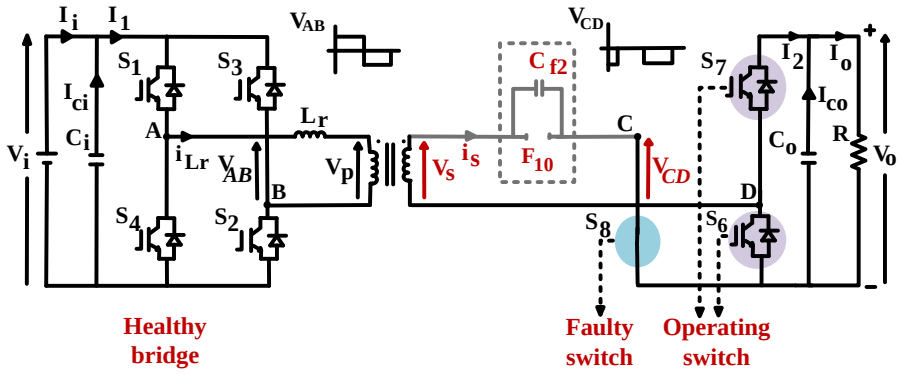



**Figure 2.10:** Reconfiguration for secondary side SC fault in $S_8$ of the DAB.

The power obtained at ($D_1$, $\phi$)= (0.53, 75°) is approximately 80% of the pre-fault power as shown in Fig. 2.8(b).

#### 2.3.1.2 Secondary-Side Failures

An SC fault in $S_8$ results in opening of the switch $S_5$ (by the protection circuitry). The half-bridge formed on the secondary side results in the flow of DC component in operating switches. This would saturate the transformer core in long term and affects the charging-discharging of the output side DC-link capacitor ($C_o$). As $C_o$ cannot charge sufficiently during $S_7$ and $S_8$ conduction due to the presence of DC component in $i_s$ hence it is unable to sustain the load current in $S_6$ and $S_8$ conduction. This consequently results in a very small or negligible voltage across CD terminals ($V_{CD}$) and load.

To implement the post-fault correction, a fuse $F_{10}$ is used to connect another fault-tolerant capacitor ($C_{f2}$) as shown in Fig. 2.10. The DC component in $i_s$ is proportional to the DC component in $V_{CD}$ thus for $S_8$ SC fault correction, the duty of switch $S_7$ is reduced during the transition period $T_{F10}$ as similar to $T_{F9}$ duration shown in Fig. 2.3. At t > $t_{FD}$ + $T_{F10}$, the fuse $F_{10}$ blows and $C_{f2}$ is connected in the circuit to block the DC component in $i_s$ with secondary side half-bridge. The fourier series expression of the fundamental voltage of $V_{CD}$ ($V_{CD}$= 0 for $D_2T_s$ duration and $V_{CD}$= -$V_o$ for $(1-D_2)T_s$ duration) in the post-fault correction is given as,

$$\begin{aligned} V_{CD} = -V_o(1-D_2) - \frac{2V_o}{2\pi}[sin\phi - sin(\phi+2\pi D_2)]cos\omega t \\ - \frac{2V_o}{2\pi}[(1-cos\phi) + (cos(\phi+2\pi D_2)-1)]sin\omega t \end{aligned} \tag{2.11}$$

where $D_2$ is the secondary side duty ratio (with respect to switch $S_5$). In the post-fault correction, $V_{CD}$ is shifted by $\phi$ duration from $\omega t = 0$. Hence keeping $V_{CD}$ = $-V_o$ at $\omega t = 0$, the relation given

in (2.11) reduces to,

$$D_2\pi = [1 - cos(2\pi D_2)]sin\phi - sin(2\pi D_2)cos\phi. \tag{2.12}$$

There are multiple solutions that can satisfy (2.12) by fixing either $\phi$ or $D_2$. The various solutions are ($D_2$, $\phi$)= (0.59, 60°), (0.40, 59°), (0.47, 54°), etc can also be used to provide the rated voltage at the output. Among all these solutions, that set of $D_2$ and $\phi$ is selected which is close to the pre-fault condition values. Thus, (0.47, 54°) is a suitable solution for (2.12).

$$D_2 = 0.47, \phi = 54^\circ \tag{2.13}$$

With the control parameters defined in (2.13), the proposed correction is able to attain the rated voltage at the output. Since the DC offset in $i_s$ affects the charging-discharging of $C_o$. The FT capacitor $C_{f2}$ removes the DC offset in $i_s$ and allow $C_o$ to charge and sustain the pre-fault load current. Here, the maximum power transfer can be calculated by (2.5) in which,

$$V_{AB} = -\frac{j2V_i}{\pi}e^{j\omega t} \tag{2.14}$$

is a FB primary side voltage. Here, the magnitude of $V_{AB}$ is given by the $|V_{AB}|$ or abs($V_{AB}$). The $V_{CD}$ is a HB secondary side voltage (shifted by $\phi$) given by,

$$V_{CD} = -V_o(1 - D_2) + \frac{V_o}{2\pi}[sin(\omega\phi_s + 2\pi D_2) - sin(\omega\phi_s) - j(cos(\omega\phi_s) - cos(\omega\phi_s + 2\pi D_2))]e^{j\omega t}. \tag{2.15}$$

Here, the magnitude of $V_{CD}$ is given by the $|V_{CD}|$ or abs($V_{CD}$).

### 2.3.2 Open Circuit Faults

When an (OC) fault occurs on the primary side, a DC shift is observed in $i_{Lr}$. Hence the proposed topology is also applicable for correcting open-circuit faults in DAB. In the proposed work, the free wheeling diodes remain healthy i.e., only the switch open-circuit faults are considered.

On occurrence of a fault, the complementary switch of the faulty leg is shorted after the fault is diagnosed at t = $t_{Fd}$ (converting the FB to HB). $F_9$ blows off to include $C_{f1}$ in the circuit. The same set of $\phi$ and $D_1$ are used as specified in Section 2.3.1. The effect of an OC failure on the secondary side includes a DC component in the $i_s$. Hence to remove this DC offset, the secondary side FB is modified to HB. Ultimately $F_{10}$ blows off in the $T_{F10}$ period to include $C_{f2}$ in the circuit. The same set of $\phi$ and $D_2$ are used as considered in Section 2.3.1.

### 2.3.3 Design of Fault-Tolerant Capacitor $C_{f1}$ and $C_{f2}$

In the proposed method, rating of $C_{f1}$ is selected by considering the supply voltage and current through the inductor. In healthy condition of the converter, the rated power is transferred at rated $i_{Lr}$ while in post-fault conditions, the power transfer happens at twice of the rated $i_{Lr}$ due to the formation of half-bridge on the primary side [19, 20] such that,

$$i_{Lr(post,fault)} = 2i_{Lr(pre-fault)} = i_{cf1} = C_{f1}\frac{\mathrm{d}V_{cf1}}{\mathrm{d}t}. \tag{2.16}$$

Using (2.10) in (2.16), the value of $C_{f1}$ is obtained in (2.17) as,

$$C_{f1} = \frac{i_{Lr(post,fault)}}{2\pi f_s \frac{V_i}{2} sin(\omega t - \frac{\phi}{4})}. \tag{2.17}$$

At $\omega t = \phi$, keeping the value of $i_{Lr(post,fault)}$ and $f_s$ in (2.17), the estimated value of $C_{f1}$ for the designed prototype is 1.5 $\mu$F.

The calculation of $C_{f2}$ in the post-fault correction of secondary side faults is similar to the design of $C_{f1}$ as,

$$C_{f2} = \frac{i_{Lr(post,fault)}}{2\pi f_s \frac{V_o}{2} sin(\omega t - \frac{3\phi}{4})}. \tag{2.18}$$

At $\omega t = 0$, keeping the value of $i_{Lr(post,fault)}$ and $f_s$ in (2.18) with 1:1 turns ratio, the estimated value of $C_{f2}$ for the designed prototype is 1.4 $\mu$F.

## 2.4 Experimental Results and Discussion

To substantiate the realization of the proposed topology, a prototype of DAB converter shown in Fig. 2.11 (with SPS control) for a power rating of 1 kW and turns ratio 1:1 is developed and tested experimentally. The specifications of the prototype are given in Table 2.2. For the primary and

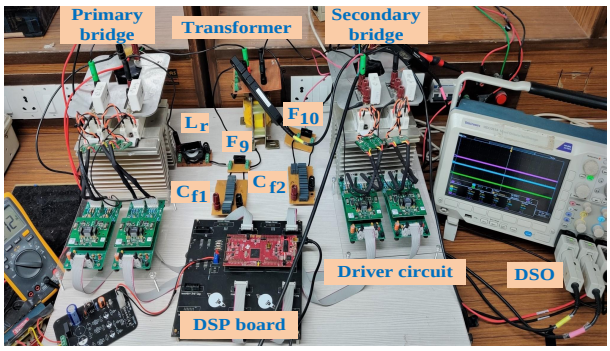
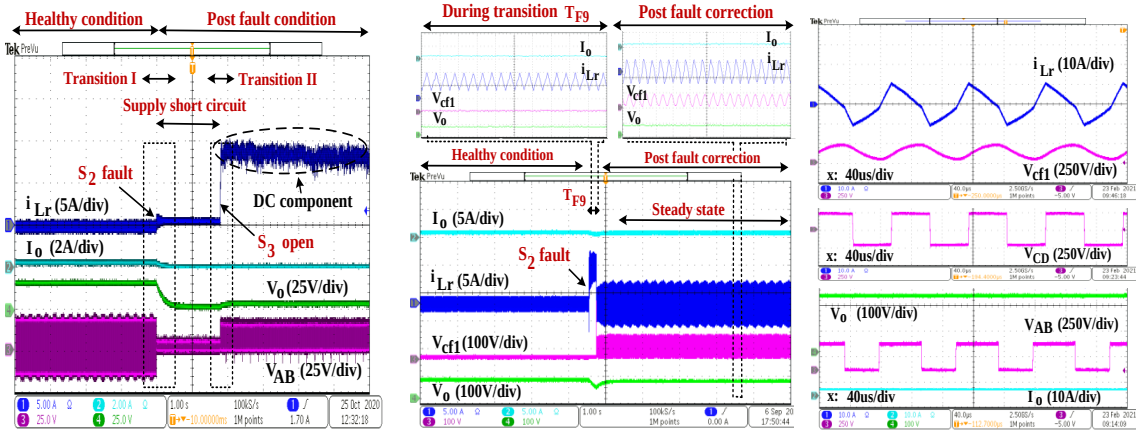



**Figure 2.11:** Hardware prototype of a 1 kW dual active bridge converter




(a) (b) (c)

**Figure 2.12:** Experimental results of $S_2$ SC fault (a) transition results from healthy to supply short-circuit at 20 V (without the overcurrent protection), (b) transition results showing $T_{F9}$ duration from healthy to post-fault reconfiguration for reduced load, and (c) showing steady-state results of the proposed correction at rated input voltage with reduced load.

**Table 2.2:** Parameters of the DAB prototype

| Parameters | Value | Parameters | Value |
|---|---|---|---|
| Input voltage ($V_i$) | 250 V | Switching frequency ($f_s$) | 10 kHz |
| Output voltage ($V_o$) | 250 V | Inductor ($L_r$) | 288 $\mu$H |
| Output power ($P_o$) | 1 kW | Fault tolerant capacitor ($C_{f1}$) | 1.5 $\mu$F |
| Winding ratio (n) | 1:1 | Fault-tolerant capacitor ($C_{f2}$) | 1.4 $\mu$F |

secondary bridge, an IGBT switch is selected as the main switch. All the fault cases and healthy operation of the converter are implemented via DSP board with sufficient deadband [46]. To verify the proposed post-fault correction, the prototype is analyzed in the transient as well as steady-state operation. The effect of control parameter variation to accomplish the objective of rated voltage is shown in the Fig. 2.12-2.14. The transient analysis is shown at 30 % of the rated voltage ($V_i$ = 250 V) while the steady-state correction is shown at the rated input voltage.

### 2.4.1 Post-fault Correction for SC Faults

The prototype is initially tested for primary side faults without correction. The healthy condition and the post-fault condition (with and without correction) for $S_2$ short-circuit fault is shown in Fig. 2.12. Transition I and transition II in Fig. 2.12(a) indicate the changeover from healthy condition to short-circuit condition and short-circuit condition to opening of the complementary switch in the device respectively. During transition I, when an SC fault occurs on $S_2$, there is a huge current flow between the DC-link and faulty leg reducing $i_{Lr}$, $V_o$ and $I_o$ to a negligible value. When the

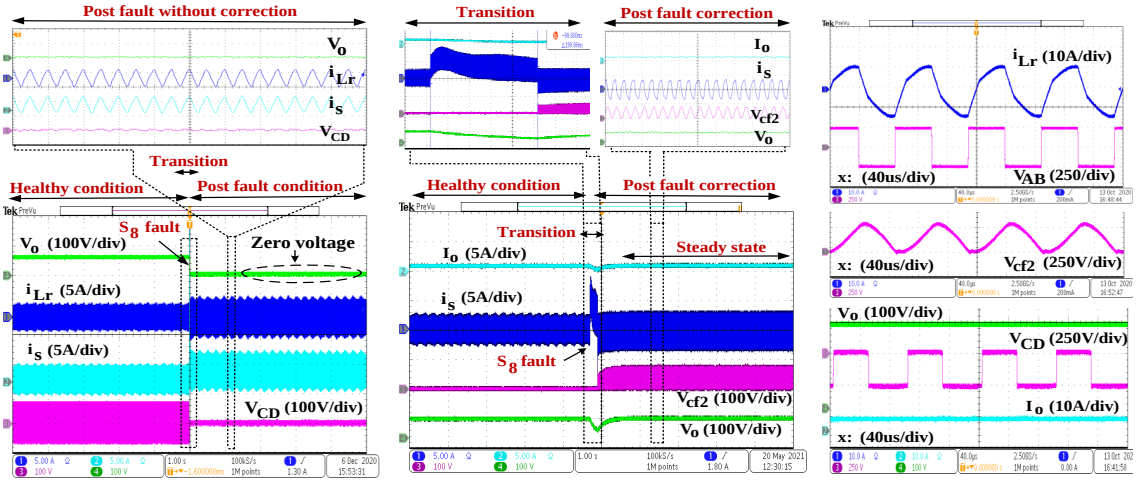



**Figure 2.13:** Experimental results of $S_8$ SC fault showing (a) transition results from healthy to the post-fault condition without the proposed reconfiguration, (b) transition results of the post-fault condition with proposed reconfiguration at 1 kW, and (c) steady-state results of the proposed correction at the rated input voltage.

fault is detected and located, to break off the flow of short-circuit current, the complementary switch ($S_3$) is opened as indicated in transition II. After opening $S_3$ (following transition II), there is a sudden flow of a huge amount of DC current even at very small input voltage through the inductor and transformer at the same duty ratio of healthy condition ($D_1$= 0.5). Hence keeping the safety constraint, results for this case are taken at $V_{in}$ = 20 V at which, more than 5A of DC flow is observed. This immense DC flow should be blocked in the post-fault conditions as discussed in Section 2.3. The transition results during the correction of primary side SC faults are shown in Fig. 2.12(b) at reduced load (0.80 kW) and 30% of the rated voltage. For a 1 kW converter, the current $i_{Lr}$ in the healthy condition will be more than the current shown in Fig. 2.12(b) (shown at 0.8 kW). The $T_{F9}$ duration (in Fig. 2.12(b)) is shown with the duty ratio adjusted using (2.4). From Fig. 2.12(b), it is seen that the converter maintains its continuity of operation with the pre-fault voltage $V_o$ obtained at the load (by including $C_{f1}$ in the circuit) after the transition. The steady-state results obtained at rated input voltage using the reconfiguration scheme are shown in Fig. 2.12(c) at 0.80 kW load. Here, $V_{AB}$ is a half-bridge voltage with rated $V_o$ achieved at the load.

The transition results from healthy to faulty condition (without the reconfiguration) for $S_8$ SC fault are shown in Fig. 2.13(a). The DC component in $i_s$ affects the charging of the DC-link capacitor hence $V_{CD}$, $V_o$ and $I_o$ reduces to a minimum value. A continuous operation is maintained by implementing the post-fault reconfiguration as discussed in Section 2.3. The transition from the healthy to post-fault reconfiguration is shown in Fig. 2.13(b). The steady-state results of the $S_8$ SC fault correction are given in Fig. 2.13(c) at the rated $V_i$. Here, the $V_{CD}$ is HB voltage while

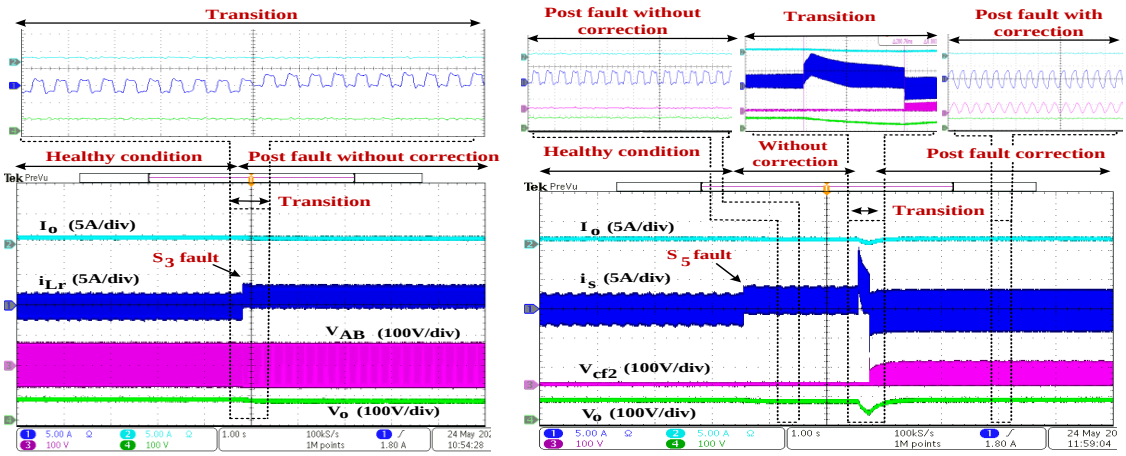



**Figure 2.14:** Experimental results of (a) transition from healthy to post-fault condition without proposed reconfiguration for $S_3$ OC fault (b) transition from healthy to post-fault condition with and without proposed correction for $S_5$ OC fault.

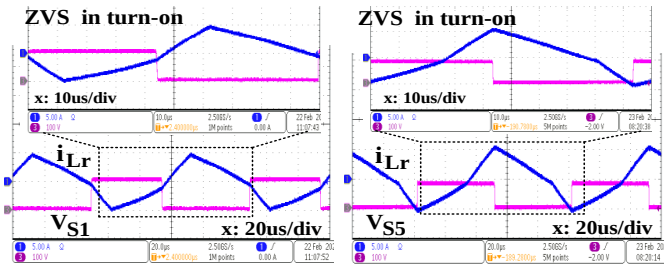



**Figure 2.15:** (a) ZVS in primary side switches, and (b) ZVS in secondary side switches during $S_2$ SC fault correction.

$V_{AB}$ is FB voltage. The charging/discharging of $C_{f2}$ at the specified control parameters (given in (2.13)) ensure that the pre-fault voltage is attained at the load.

### 2.4.2 Post-fault Correction for Open Circuit Faults

The transition from healthy to post-fault condition without reconfiguration/correction for $S_3$ open circuit fault is shown in Fig. 2.14(a). The post-fault correction is implemented to remove the DC shift in $i_{Lr}$ caused due to OC fault on $S_3$. The steady-state results for post-fault correction of $S_3$ open-circuit faults are same as shown in Fig. 2.12(c).

Transition results from healthy to post-fault condition with and without correction for $S_5$ open-circuit fault are shown in Fig. 2.14(b). A DC shift is observed in $i_s$ caused due to the open circuit fault on switch $S_5$. This DC offset is removed in the post-fault correction by including the FT capacitor $C_{f2}$ in the circuit. Here, the post-fault correction results are similar to the $S_8$ short-

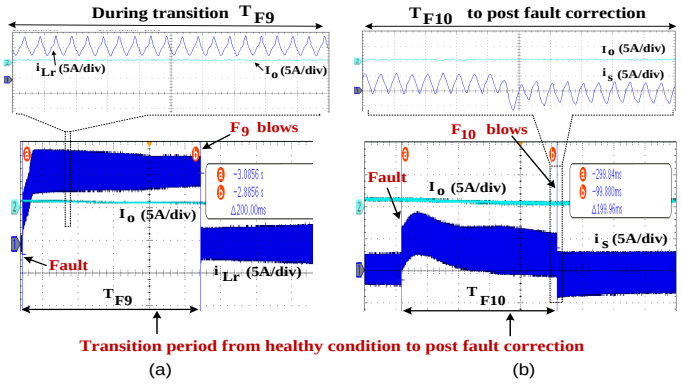



**Figure 2.16:** Experimental results showing transition (a) $T_{F9}$ for primary side fault correction, and (b) $T_{F10}$ for secondary side fault correction for 200 ms duration.

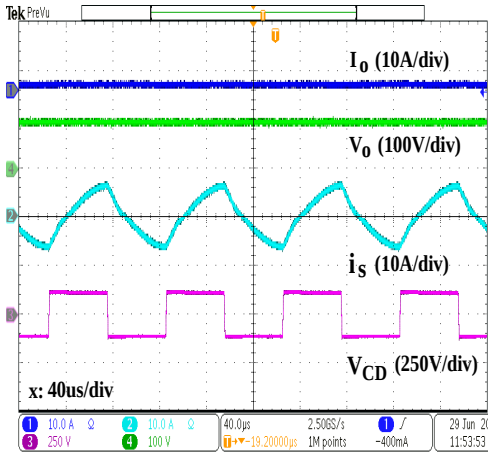



**Figure 2.17:** Experimental results showing the reverse power flow after the proposed correction of $S_3$ OC fault ($V_i$ = 100V).

circuit fault correction. The proposed method is able to sustain the pre-fault voltage and current at the load.

After analyzing all the faults from Fig. 2.12-2.14, it can be concluded that the converter remains operational following a single switch fault. The proposed method is also able to retain the soft-switching in the converter operation in the post-fault correction as shown in Fig. 2.15. The ZVS is achieved during the turn-on operation in primary and secondary side switches as indicated in Fig. 2.15 (a) and (b) (shown for $S_2$ SC fault correction).

The duration $T_{F9}$/$T_{F10}$ depends completely on the fuse selection. In Fig. 2.16(a) and Fig. 2.16(b) (also Fig. 2.12(b) and 2.13(b)), $T_{F9}$ and $T_{F10}$ are analyzed for a larger duration (200 ms) while for a fast acting fuse, this duration ($T_{F9}$/$T_{F10}$) is quite smaller. This indicates that even if the selected fuse is not a fast-acting fuse, the converter will be saved from the harmful effects of the DC flow by regulating the duty cycle. Here, the usage of the duty regulation is a designer's choice.

**Table 2.3:** Comparison of supplementary hardware, fault type and complexity in different topologies

| Feature | Proposed Method (Bidirectional power flow) | [19] (Unidirectional power flow) | [20] (Bidirectional power flow) | [39] |
|---|---|---|---|---|
| (1). Additional hardware | 2 fuses, 2 non-polarized capacitors ($C_f$) | 1 switch, 1 gate driver, 1 DC capacitor | 4 switch, 4 gate drivers, 2 DC capacitor | No additional components |
| (2). Primary side fault | Applicable for primary side OC and SC faults. | Applicable for primary side OC and SC faults. | Applicable for primary side OC and SC faults. | Applicable for primary side OC faults only. |
| (3). Secondary side fault | Applicable for secondary side OC and SC faults. | Not applicable. | Applicable for secondary side OC and SC faults. | Applicable for secondary side OC faults only. |
| (4). Complexity | Moderate complexity | Moderate complexity | Large complexity | Easy implementation |
| (5). Remarks | Applicable for DAB. Switch rating is 2 times the pre-fault current. | Not applicable for DAB. Switch rating is 2 times the pre-fault current. | Not applicable for DAB. Switch rating is 2 times the pre-fault current. | Applicable for a certain load carrying capacity in DAB. |

**Table 2.4:** Supplementary hardware, cost and complexity of the Redundant switch topologies for DAB

| Features | [16] Series redundancy | [16] Parallel redundancy |
|---|---|---|
| (1). Additional hardware | 8 switches, 8 gate drivers, 16 thyristors | 8 switches, 8 fuses, 8 gate drivers, fault isolation scheme |
| (2). Fault Type | Applicable (OC / SC) | Applicable (OC / SC) |
| (3). Conduction losses in healthy operation | Conduction losses are doubled. | Can lessen the overall conduction losses. |
| (4). Cost & Control complexity | Costly & Large complexity | Costly & Large complexity |
| (5). Remarks | Voltage sharing issue needs to be addressed. | Current sharing issue needs to be addressed |

The proposed reconfiguration is also able to achieve the fault-tolerant operation in the reverse power flow. When an OC fault occurs on the primary side while the direction of the power flow is reversed (from the secondary side to the primary side) in a converter, the DC component produced on the formation of HB will be removed by the FT capacitor $C_{f1}$ which gets connected in the main line. The experimental results of the proposed correction for the $S_3$ OC fault in case of the reverse power flow are shown in Fig. 2.17. It is seen that the converter maintains a continuous operation with the pre-fault voltage $V_o$.

The proposed OC fault correction is able to achieve fault tolerance without additional winding which is used in [38]. Also, the primary-side lower power (PLP) method used for OC fault correction presented in [39] is not able to remove the DC offset in $i_{Lr}$, which is undesirable in the converter. This problem is solved with the proposed method which is able to remove the DC shift in the inductor current. In the proposed FT method, the switches ($S_1$ to $S_8$) are selected by considering the double current flow in the post-fault correction as similar to [19, 20].

The proposed topology is implemented for DAB (unlike SRC or CLLC type resonant converter, DAB does not have the inbuilt FT capability). The presented FT method is simple, cost-effective and uses less hardware as shown in Table 2.3 and 2.4 when compared to the existing FT

methods and switch redundant methods in literature.

## 2.5 Conclusion

This work proposes methods to retain a complete semiconductor (switch) fault-tolerant feature in DAB. On occurrence of a fault on the primary or secondary side, the proposed fault-tolerant method connects $C_f$ on faulty side of the converter to obtain a ceaseless operation. Control parameter variation is adopted to obtain the rated voltage at the output. Increasing $\phi$ will boost the power transfer between bridges hence bringing $V_o$ close to the rated value. While the increase or decrease of $D_1$ or $D_2$ completely depends upon the switch undergoing fault.

The major advantage of the proposed method is its application in DAB (which does not have an inbuilt fault-tolerant capability) with reduced number of hardware and simplicity in control. With the proposed topology-

- DAB continues to operate without getting shut down on primary and secondary side switch faults (SC or OC).
- Rated voltage is achieved in the post-fault correction for primary or secondary-side faults. Also, the transition from faulty condition to post-fault correction is smooth and within the defined limits.

The proposed method is tested for different faults on a 1 kW DAB prototype and experimental results indicate the potential and robustness of the FT scheme with rated output voltage.

# Chapter 3

# Fault-Tolerant and Self-Reliant Characteristic in Series Resonant Converter for Semiconductor Open/Short Circuit Faults

## 3.1 Introduction

The technological evolution in grids and microgrids has escalated the growth of the smart transformers which requires resilient and robust converters [6, 29, 47]. Thus, the necessity of an infallible series resonant converter is of utmost significance [17, 48]. A fault-tolerant converter can resist a fault and maintains the continuous operation without getting shutoff. While the self-reliant feature is possessed by a fault-tolerant converter without additional power circuitry in the post-fault correction.

Semiconductor devices are more vulnerable to faults than other available components in a converter [35, 39, 42, 49]. The OC fault can happen as a consequence of bond wire lift-off, cooling system failure, malfunctioning of the driver and control unit, and supplementary circuit failures [2]. A fault-tolerant method reported in literature [18] for open-circuit faults uses redundant winding, relays, and four additional fuses to reconfigure the converter to meet the load requirement. Using a large number of additional components increases the cost of the implementation of the fault-tolerant method. A dual-loop control is implemented in [40] to correct the open-circuit faults on both the sides of the series resonant dual active bridge converter. The outer and the inner loop is used for voltage control and the current envelope control respectively. Here, the fault tolerance is achieved only for OC faults with complex control.

SC faults are mainly caused due to improper gate driver (malfunctioning of the driver unit) or intrinsic failure [16, 37]. These faults results in a huge current flow, destroying all the connected components. The single switch fault-tolerant methods discussed in literature [10, 16, 19, 20, 37, 50, 51, 52] includes extra components like redundant converter or leg in the post-fault reconfiguration [16]. A fault-tolerant method for primary side failure in SRC having diode bridge rectifier is discussed in [19, 37, 50, 51]. An SC fault diagnostic method uses DC-link current and the transformer primary side voltage in [37]. The converter is reconfigured using a boost unit (uses a switch and a diode), introduced between the output rectifier and the filter capacitor. This reconfiguration is only applicable for primary side faults (not applicable for secondary side semiconductor faults). Another fault-tolerant method having unidirectional voltage doubler configuration is shown in [19] for SC and OC fault correction. It uses an additional switch and a split-capacitor configuration on the rectifier side for primary side switch fault correction only. Further improvement in reliability is achieved in [50, 51] towards multiple faults. In [51], the first fault-tolerant ability is obtained by using a redundant circuitry while two additional diodes are added to retain the fault tolerance for second fault. This configuration uses more number of components to provide fault tolerance for primary side faults in a unidirectional power flow converter.

The SC fault correction for bidirectional converter is explored in [10, 20, 52]. A bidirectional converter with voltage doubler configuration is discussed in [20]. Though the fault-tolerant operation is improved, the number of additional components for achieving the fault tolerance increased largely (i.e. four switches and split capacitors on both the sides), increasing the cost and complexity of the converter. A design procedure for the reliability improvement is discussed in [10] for a fault-tolerant SRC. Although, fault-tolerant methods are available in literature [2, 10, 16, 18, 19, 20, 37, 39, 40, 42, 50, 51, 52] but the role of the self-reliant characteristic of the converter in achieving the fault tolerance and the common post-fault correction for a single switch is not discussed. Also, the secondary side SC failure in bidirectional SRC is not deeply analyzed in terms of the current flow and behavior of the converter in the post-fault conditions.

In this chapter, the self-reliant characteristic of the SRC for single switch fault is explored. A post-fault correction is proposed which uses a fault-tolerant (FT) capacitor $C_f$ to achieve a continuous operation of the converter. The objective of the continuous converter operation and the pre-fault voltage at the output is achieved for single switch fault in the converter. Control parameters like phase shift ($\phi$), primary and secondary side duty ratio ($D_1$ and $D_2$) are controlled to obtain the pre-fault output voltage in the post-fault correction.

## 3.2 Self-reliant Feature in SRC

A converter is said to be fault-tolerant when it is able to continue its operation even after sudden failures [34, 52]. While the self-reliant feature refers to the use of existing hardware (no additional power circuit) to achieve fault-tolerance for the respective fault. The additional circuitry used in fault detection is present by default in all the converters for detecting a fault.

The self-reliant characteristic in a converter depends upon- the type of converter, location of the faulty device and the type of fault (OC/SC fault). Here, a series resonant converter shown in Fig. 3.1(a) is analyzed for the self-reliant characteristic. On the occurrence of a short-circuit (SC) fault on the primary side, the complementary switch is opened as a primitive measure to safeguard the supply or load side DC-link, converting the full-bridge (FB) to a half-bridge (HB) [10, 19, 20]. For primary side SC fault cases, the HB formation results in a DC flow in the primary bridge. This unwanted DC component is blocked by the resonant capacitor $C_r$ thus, protecting the switches and devices from getting damaged. Hence the converter possesses a self-reliant feature for primary side SC faults. On formation of a half-bridge, the output voltage reduces to half of the pre-fault value. This voltage reduction at load is unacceptable in converters. Thus, a post-fault correction is highly needed to achieve the pre-fault voltage and the maximum power flow at the output.

Similarly, an undesirable DC shift is also observed in $i_s$ (secondary side current) on the formation of a HB (after an SC fault) on the secondary side of the converter. As a result, the DC-link capacitor ($C_o$) on the load side is unable to charge sufficiently and sustain the required voltage at the load. Since SRC does not a have a resonant capacitor on the secondary side, the DC offset in this case is removed with the help of auxiliary power circuitry added in the post-fault reconfiguration. Here, the converter essentially requires a post-fault correction method to maintain a continuous converter operation. Thus, the SRC does not retain the self-reliant feature for secondary side SC faults. While for an OC fault on any side of the converter, the self-reliant feature is available in SRC (detailed analysis is done in Section 3.3).

## 3.3 Proposed Correction for Single Switch Fault

The basic circuitry of a series resonant converter consists of two full bridges (having $S_1$-$S_8$ switches) separated by a high frequency transformer as shown in Fig. 3.1(a). Phase shift modulation is adopted in the converter with the bidirectional power flow. The converter is operated with the switching frequency ($f_s$) equal or slightly less than the resonant frequency ($f_r$) to get the benefit of the soft-switching on the primary and secondary side semiconductors [1, 10]. The relationship

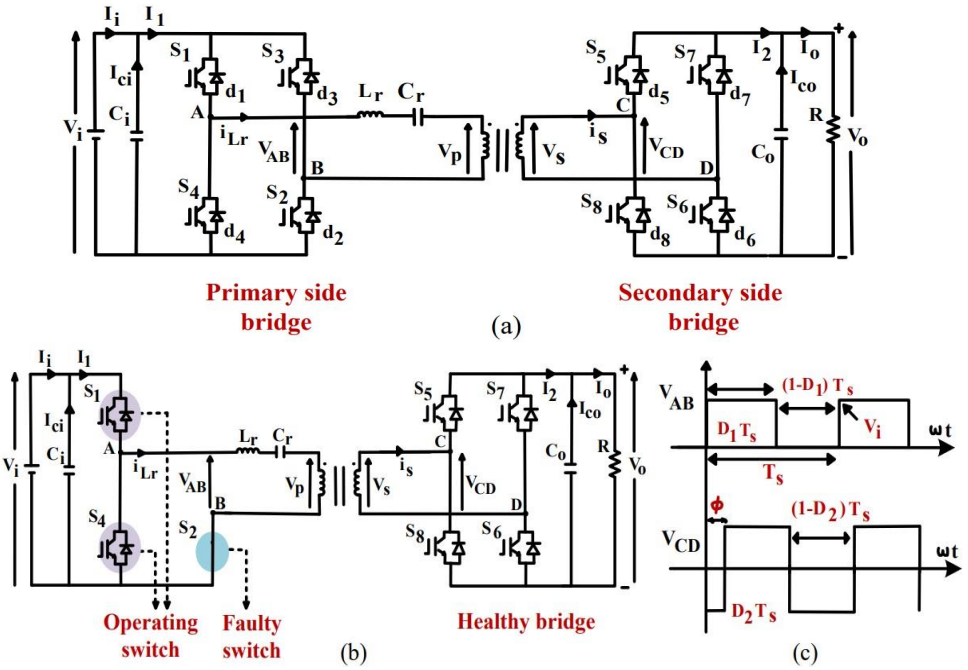



**Figure 3.1:** (a) Circuit configuration of series resonant converter, (b) post-fault circuit reconfiguration for primary side SC faults ($S_2$ fault), and (c) voltage profile of SRC under post-fault correction of $S_2$ SC fault.

between $f_r$, resonant inductor ($L_r$) and capacitor ($C_r$) is given by [19],

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{3.1}$$

To achieve the maximum efficiency, the converter is generally designed at resonant frequency i.e., $f_s = f_r$. The switches are operated at 50% duty cycle in the normal (pre-fault) operation of the converter. The detailed selection of parameters for the healthy operation of the converter is discussed in [10].

### 3.3.1 Short-Circuit Fault on the Primary Side

When a short-circuit fault occurs on the primary side, the FB is converted to HB as shown in Fig. 3.1(b) and (c). The complete series of events in case of an SC fault are given in Fig. 3.2. Consider a short-circuit fault on $S_2$ at $t = t_f$, the switch $S_3$ will be opened by the protection circuitry. Here, $V_{AB}$ is a half-bridge voltage with half of the pre-fault voltage obtained at the load. The resulting DC component in $i_{Lr}$ will be blocked by $C_r$ ensuring the normal current flow.

After the fault occurrence, the fault diagnosis is completed at $t = t_{Fd}$. To obtain the rated output voltage, the post-fault correction is implemented for $t > t_{Fd}$ (path I in Fig. 3.2). The values

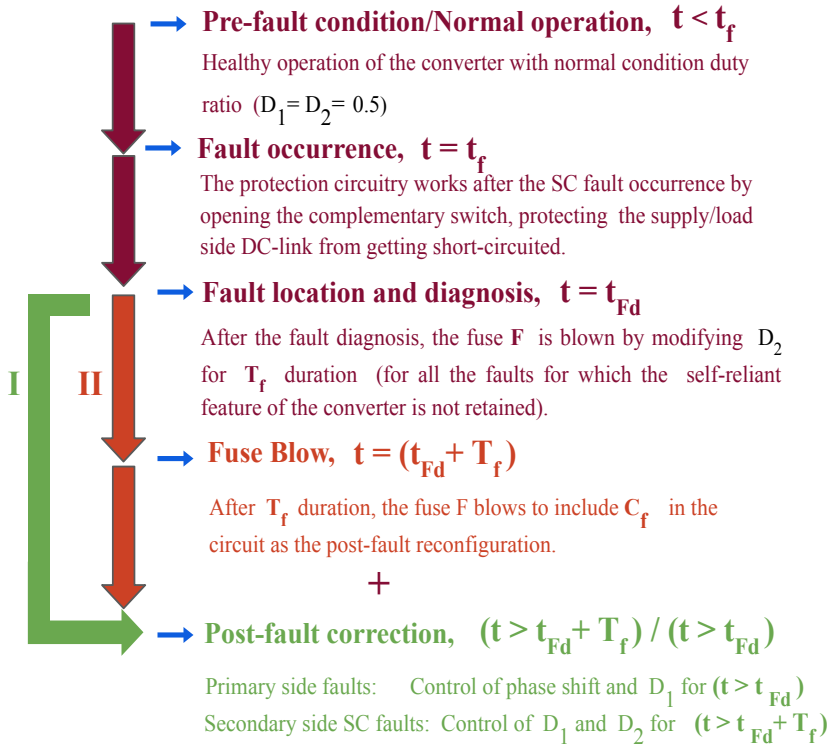



**Figure 3.2:** Series of events on the occurrence of a SC fault in the converter.

of $D_1$ (with respect to switch $S_1$) and $\phi$ (marked in Fig. 3.1(c)) are varied in the correction. Here, $D_2$ variation is not adopted as it adds the DC component on the secondary side. To calculate $D_1$ and $\phi$, the fourier series expression of the fundamental voltage of $V_{AB}$ shown in Fig. 3.1(c) is given by,

$$V_{AB} = V_i D_1 + \frac{2V_i}{T_s} sin\omega t - \frac{2V_i}{T_s}[sin(\omega t - D_1 T_s)] \tag{3.2}$$

where $T_s$ is the duration of one cycle. At $\omega t = \phi$, $V_{AB} = V_i$ (Fig. 3.1(c)). The relation between $D_1$ and $\phi$ in the post-fault condition is given as,

$$(1 - D_1)\pi - sin\phi = sin(D_1 T_s - \phi). \tag{3.3}$$

There are several solutions like ($D_1$, $\phi$)= (0.58, 58°) (0.53, 55°), etc. that can satisfy (3.3). Among all the solutions, (0.53, 55°) is selected as it is close to the healthy condition parameters. From (3.2), it is observed that a change in the duty ratio affects the amount of DC component ($V_i D_1$) in the voltage $V_{AB}$. Although the resonant capacitor is present on the primary side to block this DC component, selecting a large duty variation is not recommended. Thus, $D_1$ is fixed at 0.53 while $\phi$ is selected as 55°. Hence,

$$D_1 = 0.53, \phi = 55°. \tag{3.4}$$

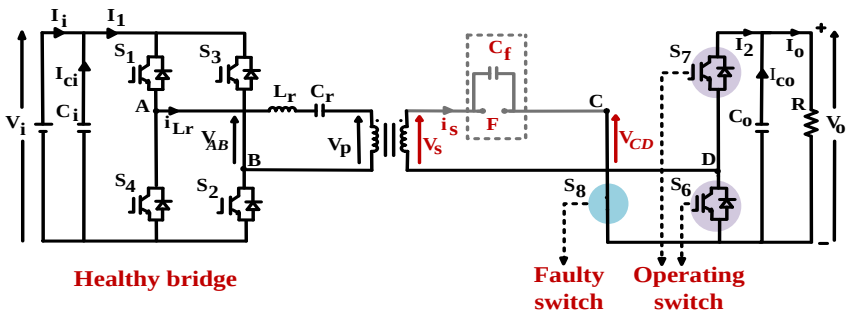



**Figure 3.3:** Post-fault reconfiguration for secondary side SC faults ($S_8$ fault).

Also, applying KVL on the primary side in Fig. 3.1(b) as,

$$V_{AB} = V_{Lr} + V_{Cr} + V_p \tag{3.5}$$

where $V_{Lr}$ and $V_{Cr}$ are the voltages across $L_r$ and $C_r$. Further, higher values of $\phi$ can also be used depending on the designed values of $L_r$ and $C_r$ (as seen from (3.2), (3.3) and (3.5)) in the healthy condition. Here, a large increase in $\phi$ leads to the distortion in voltage and current profile. Thus, a load reduction of 25% is adopted to achieve the rated output voltage ($V_o$) in post-fault correction with control parameters mentioned in (3.4).

The analysis for SC fault on $S_1$ or $S_2$ is similar. However, if $S_3$ or $S_4$ suffer a SC failure, the $\phi$ remains same as given in (3.4) while $D_1$ changes to 0.47. Thus, for all the primary side fault cases, the proposed configuration is able to maintain the continuity of operation and the required voltage at the load.

### 3.3.2 Short-Circuit Fault on the Secondary Side

Consider, $S_8$ has suffered from an SC fault as shown in Fig. 3.3. The protection circuitry works after the fault occurrence at t = $t_f$ by opening the complementary switch $S_5$ (converting FB to HB). Thereafter, the fault is detected at t = $t_{Fd}$ by the fault diagnosis circuitry. The half-bridge formation results in a sudden current peak (with DC offset) in $i_s$. This peak in $i_s$ (during the transition period) is proportional to the DC component in $V_{CD}$ which can be reduced by the duty cycle control of the secondary side semiconductors as shown in Fig. 3.4(a), (b) and (c). On reducing the duty ratio of $S_7$ (or increasing the duty ratio of $S_6$) from the healthy condition duty ratio ($D_2$= 0.5 or 50 %), the sudden peak in $i_s$ decreases. This current peak is helpful in implementing the post-fault correction by blowing the fuse $F$ at $t = t_{Fd}$+$T_f$. The duration $T_f$ is defined as the transition period between faulty condition to the post-fault correction. Here, the duty reduction of $S_7$ is adopted during $T_f$ such that the peak in current $i_s$ is adequate to blow the fuse $F$ but not sufficient to cause

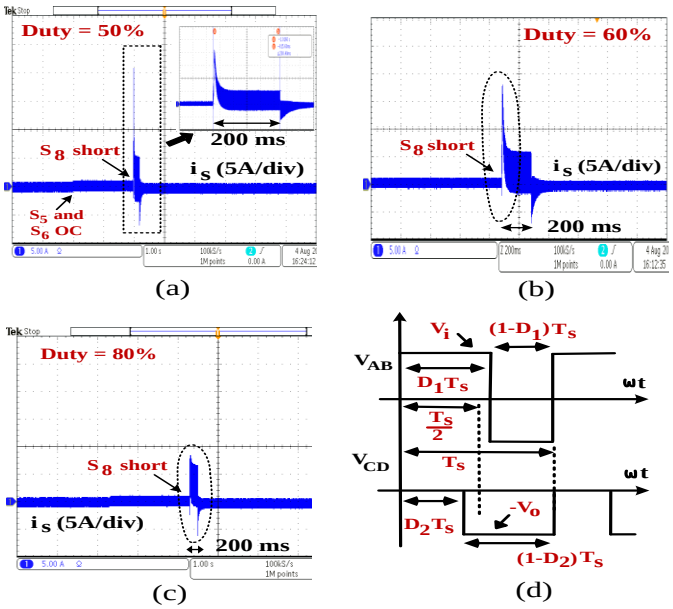



**Figure 3.4:** Transient behavior of the secondary current $i_s$ (on the formation of the half-bridge) with duty cycle $D_2$ (with respect to switch $S_6$) of (a) 50 %, (b) 60 %, (c) 80 % for $S_8$ SC and $S_5$, $S_6$ OC fault (similar behaviour for $S_8$ SC fault), and (d) voltage profile of SRC under post-fault correction of $S_8$ SC fault.

other component failure. The duty cycle $D_{2(T_f)}$ during the period $T_f$ is calculated from the DC component in $V_{CD}$. The fourier series expression of the voltage $V_{CD}$ in the post-fault condition shown in Fig. 3.4(d) is given by,

$$V_{CD} = -V_o(1-D_2) + \frac{2V_o}{T_s} sin(D_2T_s) cos\omega t + \frac{2V_o}{T_s}[(1-cos(D_2T_s)] sin\omega t. \tag{3.6}$$

The DC component in $V_{CD}$ is $V_o(1-D_2)$ as seen in (3.6). Thus, the DC flow in $i_s$ is given by,

$$i_{s(DC)} = \frac{V_{CD_{DCcomp.}}}{R_{CD}} = \frac{V_o(1-D_2)}{R_{CD}}. \tag{3.7}$$

With an increase in the duty of switch $S_6$, the DC flow in $i_s$ reduces as seen in (3.7). Hence the modified duty cycle $D_{2(T_f)}$ in $T_f$ duration is calculated by,

$$D_{2(T_f)} = 1 - \frac{i_{s(DC)}R_{CD}}{V_o}. \tag{3.8}$$

The post-fault reconfiguration is followed after $T_f$ duration by blowing the fuse $F$. Since the circuit in pre-fault condition operates as SRC with fuse $F$ (allows a bidirectional current flow). A fuse of 2 times the rated current flow i.e., $2i_{(rated)}$ is selected for implementing the post-fault reconfiguration.

As seen from (3.8), the calculation of $D_{2(T_f)}$ depends on the $i_{s(DC)}$, $R_{CD}$, and $V_o$. The maximum allowable $i_{s(DC)}$ is limited by the $D_{2(T_f)}$ selection and is a designer's choice. If the selected fuse is a fast-acting fuse, the $D_{2(T_f)}$ is selected such that the current flow is significant to blow the fuse immediately. For this, the duty ratio is selected less than 80%. For a slow-acting fuse, the current should be reduced during the $T_f$ duration such that it does not damage the components until the fuse blow. For this case, the duty ratio is selected more than 80%.

As discussed in Section 3.2, the SRC is not self-reliant for secondary side SC faults. Thus, a fault-tolerant (FT) capacitor $C_f$ connected parallel to the fuse $F$ is used to remove the DC shift in $i_s$ for t $> T_{Fd} + T_f$ (path II in Fig. 3.2). It plays an important role (connected when the fuse $F$ blows) in maintaining the continuity of operation and boosting the voltage at the output. To achieve the rated voltage at the output, control parameters i.e., $D_1$ and $D_2$ variation is adopted in the post-fault correction. Here, $\phi$ as a control parameter is not used (to retain the feature of ZCS in the converter).

#### 3.3.2.1 Control of $D_1$ and $D_2$ in the Post-Fault Correction

To calculate the value of $D_2$ (secondary side duty ratio i.e., with respect to switch $S_5$), substitute $V_{CD}$ = 0 at $\omega t = \frac{\pi}{2}$ (from Fig. 3.4(d)) in (3.6), the following expression is obtained,

$$D_2 - \frac{2}{T_s} cos(D_2 T_s) = 1 - \frac{2}{T_s}. \tag{3.9}$$

$D_2$ = 0.41 (with respect to switch $S_5$ and $S_6$) can satisfy (3.9). Since the duty variation is large, the objective of the rated voltage can be achieved while compromising the ZCS in the converter. Using $D_1$ or $D_2$ alone does not fulfill the requirements of post-fault correction including soft-switching. Thus, the control of both $D_1$ and $D_2$ is adopted.

The fourier series expression of fundamental component of $V_{AB}$ in the post-fault correction shown in Fig. 3.4(d) is given by,

$$V_{AB} = V_i(2D_1 - 1) + \frac{4V_i}{T_s} sin(D_1 T_s) cos\omega t + \frac{4V_i}{T_s}(1 - cos(D_1 T_s)) sin\omega t. \tag{3.10}$$

At $\omega t = \frac{3\pi}{2}$, $V_{AB}$= -$V_i$ as seen in Fig. 3.4(d), (3.10) is reduced to,

$$-1 = 2D_1 - 1 - \frac{4}{T_s}(1 - cos(D_1 T_s)). \tag{3.11}$$

Similarly, at $\omega t = \frac{3\pi}{2}$, $V_{CD}$= -$V_o$ as seen in Fig. 3.4(d), (3.6) is reduced to,

$$-1 = -(1 - D_2) - \frac{2}{T_s}(1 - cos(D_2 T_s)). \tag{3.12}$$

Equating (3.11) and (3.12), the following relationship between $D_1$ and $D_2$ (for $S_8$ SC fault) is obtained as,

$$(2D_1 - D_2) - \frac{2}{T_s} = \frac{2}{T_s}cos(D_2T_s) - \frac{4}{T_s}cos(D_1T_s). \tag{3.13}$$

(3.13) can be satisfied by multiple solutions like ($D_1$, $D_2$) = (0.57, 0.55), (0.54, 0.47), etc. Among all the solutions, (0.54, 0.47) is selected as it is close to the healthy condition parameters. From (3.6) and (3.10), it is observed that a change in the duty ratio affects the amount of DC component in the voltage $V_{AB}$ or $V_{CD}$. Also, selecting a large duty variation affects the soft-switching in the converter. Thus,

$$D_1 = 0.54, D_2 = 0.47. \tag{3.14}$$

The proposed configuration is also applicable for other secondary side semiconductor failures.

#### 3.3.2.2 Designing of FT Capacitor

For designing $C_f$, the current through FT capacitor (here for 1:1 winding ratio) is considered as,

$$2.i_{Lr(pre-fault)} = i_{Lr(post-fault)} = C_f\frac{\mathrm{d}V_{cf}}{\mathrm{d}t}. \tag{3.15}$$

$V_{cf}$ (voltage across $C_f$) can be written as,

$$V_{cf} = V_s - V_{CD} = \frac{V_o}{2} - \frac{V_o}{2}cos(\omega t). \tag{3.16}$$

Substituting (3.16) in (3.15), the expression for $C_f$ is given by,

$$C_f = \frac{i_{Lr(post-fault)}}{2\pi f_s\frac{V_o}{2}sin(\omega t)}. \tag{3.17}$$

Substituting the value of $i_{Lr(post-fault)}$ and $f_s$ (switching frequency) in (3.17), the approximate value of $C_f$ for the designed prototype is estimated as 1.5 $\mu$F. The proposed method is able to achieve the pre-fault voltage and power at the load.

### 3.3.3 OC Fault on the Primary/Secondary Side of SRC

The open-circuit fault on the primary side results in approximately half of the pre-fault voltage at the output. The presence of $C_r$ will provide a benefit of self-reliant operation for primary side OC faults. Also, $i_{Lr}$ is free from the DC shift as $C_r$ will block the DC component in current produced due to the voltage obtained at AB. The post-fault correction is similar to that mentioned in Sections 3.3.1 and 3.3.2. The complementary switch in the faulty leg is shorted after the fault diagnosis.

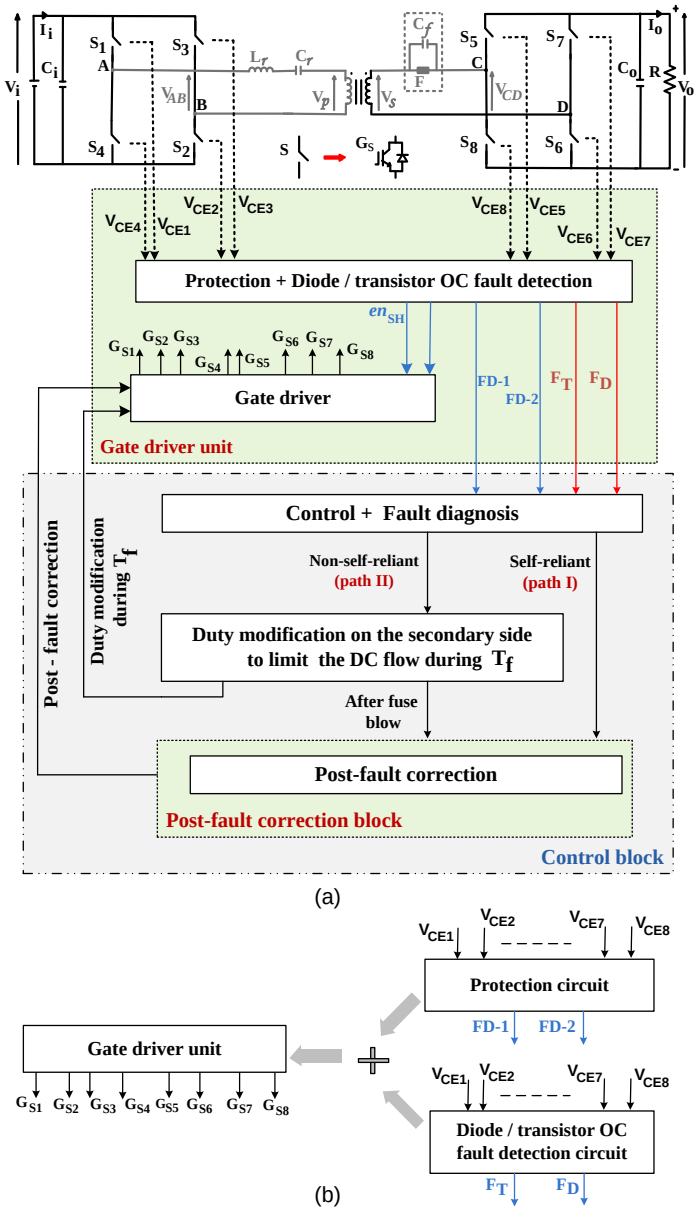



**Figure 3.5:** (a) Fault detection method for semiconductor OC/SC faults, and (b) description of gate driver unit.

Only the transient results vary while the steady-state results are similar in the correction of OC and SC fault.

A switch OC fault on the secondary side of the converter does not result in a significant DC shift in $i_s$ (secondary side current) as the majority of the conduction on secondary side is through the diodes. The post-fault configuration does not need any additional component thus, the converter retain the self-reliant feature for secondary side switch OC faults.

### 3.3.4 Fault detection method

The post-fault correction is always followed after a fault detection scheme. The main objective of the proposed work is to design a common fault-tolerant reconfiguration method which can correct switch OC or SC faults. Thus, the existing methods mentioned in literature can be used for detecting a fault in the proposed work. Various methods discussed in [18, 19, 37, 42, 44, 51, 53, 54] like desaturation detection [19], current mirror method, protection by gate voltage, voltage/current measurement [51], etc are used to detect a SC/OC fault in the SRC. The diode/transistor OC faults are also detected in the [42, 53]. In [53], the voltage across each semiconductor is measured with a detection circuitry included in the gate driver. The measuring circuitry is inexpensive, less complicated and without the use of additional sensors. Another fault detection method for transistor/diode open circuit faults is discussed in [42]. The faulty device is located by using the average values of the voltage without adding the hardware cost [42]. Thus, for the proposed work, the diagnosis of SC/OC fault in semiconductor (switch or diode) can be performed by a combination of two methods mentioned in [19] and [53].

For a SC fault, the desaturation detection is used. As shown in Fig. 3.5, the voltage $V_{CE}$ (collector-emitter voltage) is sensed to detect a fault. The gate driver unit consists of the protection circuitry and the diode/transistor OC fault detection circuitry. Here, the protection circuitry disable the pulses to the driver circuit of the healthy switch (i.e. complementary switch) as soon as $V_{CE}$ across the switch goes from a low value to the DC-link value while the gate signal is still given [19]. The signals FD-1 and FD-2 are further send for the fault diagnosis as shown in Fig. 3.5. After the fault diagnosis, the controller implements the post-fault correction depending on the self-reliant feature of the converter (as indicated by path I and path II in Fig. 3.5). For the OC fault detection, the voltage $V_{CE}$ is used as an indicator of the faulty device as diode or transistor. This method also avoids the use of additional voltage sensors in the measurement. The average value of the voltage is compared with a reference value to detect the faulty device as mentioned in [53].

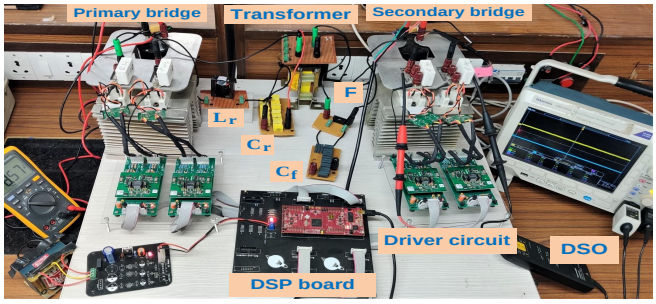



**Figure 3.6:** Hardware prototype for 1 kW series resonant converter.

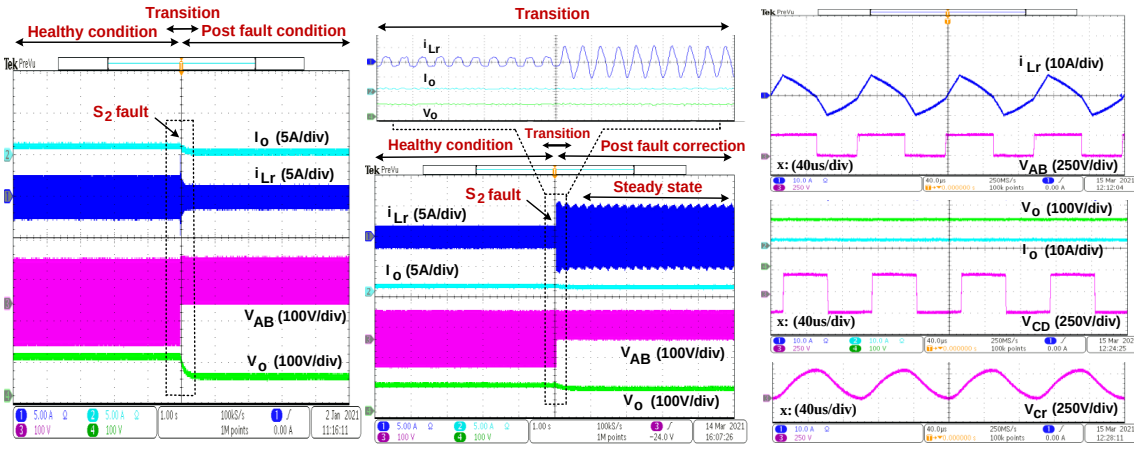



**Figure 3.7:** Experimental results of $S_2$ short circuit fault (a) transition from healthy to post-fault condition without correction, (b) transition from healthy to post-fault condition with correction at 0.75 kW load, and (c) steady-state post-fault correction results at rated input voltage in SRC.

Here, the signal $F_T$ and $F_D$ shown in Fig. 3.5(b) indicates an OC fault on the transistor and diode respectively.

## 3.4 Results and Discussion

To validate the self-reliant characteristic in the converter, a prototype of SRC employing Semikron IGBT switches is developed with single-phase shift (SPS) control as shown in Fig. 3.6. The parameters of the prototype are mentioned in Table 3.1. The switch OC and SC fault cases in the converter are implemented by the digital signal processor (DSP) board similar to [10, 19, 20]. The experimental results shown in Fig. 3.7-3.8 indicates the analysis on the self-reliant operation with the transient and steady-state behaviour during converter faults. The transient analysis (for all the fault cases) is shown at an input voltage of 100 V for safety reasons. While the steady-state post-fault correction for single switch faults is shown at 250 V.

**Table 3.1:** Parameters of the prototype

| Parameters | Value | Parameters | Value |
|---|---|---|---|
| Input voltage ($V_i$) | 250 V | Output voltage ($V_o$) | 250 V |
| Output power ($P_o$) | 1 kW | Winding ratio (n) | 1:1 |
| Switching frequency ($f_s$) | 10 kHz | Resonant inductor ($L_r$) | 270 $\mu$H |
| Resonant capacitor ($C_r$) | 0.9 $\mu$F | FT capacitance ($C_f$) | 1.5 $\mu$F |

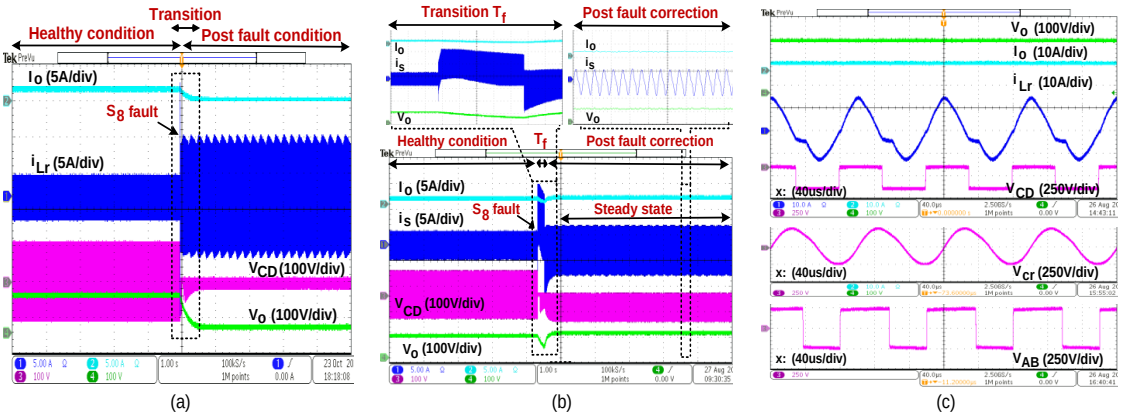



**Figure 3.8:** Experimental results of $S_8$ short-circuit fault (a) transition from healthy to post-fault condition without correction, (b) transition from healthy to post-fault condition with correction, and (c) steady-state post-fault correction results at rated voltage in SRC.

### 3.4.1 Proposed Correction for Single Switch Fault

Initially, the converter was tested for primary side short-circuit fault. The transition from healthy condition to post-fault condition without correction for $S_2$ SC fault is shown in Fig. 3.7(a) where the output voltage ($V_o$) and current ($I_o$) are reduced to half of the pre-fault value on opening of switch $S_3$. Here, $V_{AB}$ is the half-bridge voltage formed on the primary side, indicating the self-reliant operation of the converter towards primary side SC faults. The transition results of post-fault correction for primary side SC faults at reduced load (0.75 kW) is given in Fig. 3.7(b). On the formation of HB, the current in the post-fault correction is double of the pre-fault current to maintain the same power at the output (inherent characteristic of half-bridge SRC as given in [19]). Hence the switches are selected considering the double current flow in the post-fault correction. The steady-state results are shown in Fig. 3.7(c) at the rated input voltage (circuitry shown in Fig. 3.1(b)). The same reconfiguration is also followed for a diode SC fault on the primary side. The steady state results for diode $d_2$ SC fault are similar to switch $S_2$ SC fault as shown in Fig. 3.7(c).

When a short-circuit fault occurs on switch $S_8$ present on the secondary side of the converter, switch $S_5$ is opened by the protection circuitry. The output voltage ($V_o$) and current ($I_o$) reduces to a negligible value as shown in Fig. 3.8(a) with a DC offset in $i_s$. Hence SRC is not self-reliant for secondary side SC faults. Fig. 3.8(b) shows the transition results from healthy to post-fault correction including $T_f$ duration. The steady-state results obtained in the proposed post-fault correction (circuitry shown in Fig. 3.3) at rated input voltage are shown in Fig. 3.8(c). The results indicate the effectiveness of the reconfiguration to achieve the pre-fault voltage at the load. Here, the steady-state results for diode $d_8$ SC fault are similar to switch $S_8$ SC fault. However, when an

**Table 3.2:** Comparison of additional hardware, fault type, cost and power flow in different topologies

| Features | Proposed Method (A basic SRC converter) | [40] Dual loop configuration (A series resonant DAB converter) | [19] Voltage doubler configuration (A basic SRC converter) | [20] Voltage doubler configuration (A basic SRC converter) |
|---|---|---|---|---|
| (1). Additional hardware | 1 fuse 1 non-polarized capacitor ($C_f$) | Implementation of two control loops | 1 split capacitor, 1 switch, 1 Gate driver | 2 split capacitors, 4 switches, 4 Gate drivers |
| (2). Primary side fault | Applicable for both OC and SC faults. | Applicable for only OC faults | Applicable for both OC and SC faults. | Applicable for both OC and SC faults. |
| (3). Secondary side fault | Applicable for both OC and SC faults. | Applicable for only OC faults | Not applicable | Applicable for both OC and SC faults. |
| (4). Cost of the method | Less costly (provides FT feature for SC/OC faults on both the sides) | Less costly | Moderate cost (provides FT feature for primary side faults only) | Costly (number of additional components are large). |
| (5). Power flow | Bidirectional | Bidirectional | Unidirectional | Bidirectional |

OC fault occurs on switch $S_5$, the post-fault condition does not need any additional hardware to maintain the continuity of operation and rated $V_o$.

## 3.5 Conclusion

In this work, the self-reliant characteristic of a series resonant converter along with the post-fault correction for single semiconductor short/open circuit fault is presented. When a fault (SC or OC) occurs on the primary side of SRC, the rated voltage at the output is attained by varying the control parameters. Inductor current is free from undesired DC offset. Hence SRC exhibit self-reliant feature towards SC/OC faults occurring on the primary side of the converter. For the secondary side semiconductor SC faults, an FT capacitor is added to block the DC component in the secondary side current. Thus, SRC is not self-reliant for secondary-side faults (except switch OC faults).

The advantages of the proposed post-fault correction are its application to achieve continuity of operation and overall fault tolerance in a series resonant converter with the reduced number of additional components. The experimental results obtained for a 1 kW series resonant converter for various fault cases indicates the effectiveness of the proposed work.

# Chapter 4

# Analysis of Two-Switch Failures in Series Resonant and Dual Active Bridge Converters

## 4.1 Introduction

DAB and SRC are frequently employed in a variety of applications. The analysis of the converter's self-reliant function becomes essential and useful for analyzing fault behaviour and finalising post-fault correction. In the previously discussed Chapters 2 and 3, the DAB and SRC are analyzed for the single switch fault. However, two switch faults are also possible in converters. Thus, the proposed fault-tolerant scheme is further analyzed for two switch faults for its applicability. The initial failure can occur on either side of the converter. The second fault, on the other hand, can occur on the same or opposite side of the converter. The faults can be OC, SC, or both, occurring simultaneously or one after the other. This chapter examines the pre-fault and post-fault situations in the event of two switch faults on the DAB and SRC.

**Table 4.1:** Possible combinations of two switch OC/SC faults in SRC

| $m \times n$ | n=1 | n=2 | n=3 | n=4 | n=5 | n=6 | n=7 | n=8 |
|---|---|---|---|---|---|---|---|---|
| m=1 | $S_1, S_1$ | $S_1, S_2$ | $S_1, S_3$ | $S_1, S_4$ | $S_1, S_5$ | $S_1, S_6$ | $S_1, S_7$ | $S_1, S_8$ |
| m=2 | $S_2, S_1$ | $S_2, S_2$ | $S_2, S_3$ | $S_2, S_4$ | $S_2, S_5$ | $S_2, S_6$ | $S_2, S_7$ | $S_2, S_8$ |
| m=3 | $S_3, S_1$ | $S_3, S_2$ | $S_3, S_3$ | $S_3, S_4$ | $S_3, S_5$ | $S_3, S_6$ | $S_3, S_7$ | $S_3, S_8$ |
| m=4 | $S_4, S_1$ | $S_4, S_2$ | $S_4, S_3$ | $S_4, S_4$ | $S_4, S_5$ | $S_4, S_6$ | $S_4, S_7$ | $S_4, S_8$ |
| m=5 | $S_5, S_1$ | $S_5, S_2$ | $S_5, S_3$ | $S_5, S_4$ | $S_5, S_5$ | $S_5, S_6$ | $S_5, S_7$ | $S_5, S_8$ |
| m=6 | $S_6, S_1$ | $S_6, S_2$ | $S_6, S_3$ | $S_6, S_4$ | $S_6, S_5$ | $S_6, S_6$ | $S_6, S_7$ | $S_6, S_8$ |
| m=7 | $S_7, S_1$ | $S_7, S_2$ | $S_7, S_3$ | $S_7, S_4$ | $S_7, S_5$ | $S_7, S_6$ | $S_7, S_7$ | $S_7, S_8$ |
| m=8 | $S_8, S_1$ | $S_8, S_2$ | $S_8, S_3$ | $S_8, S_4$ | $S_8, S_5$ | $S_8, S_6$ | $S_8, S_7$ | $S_8, S_8$ |

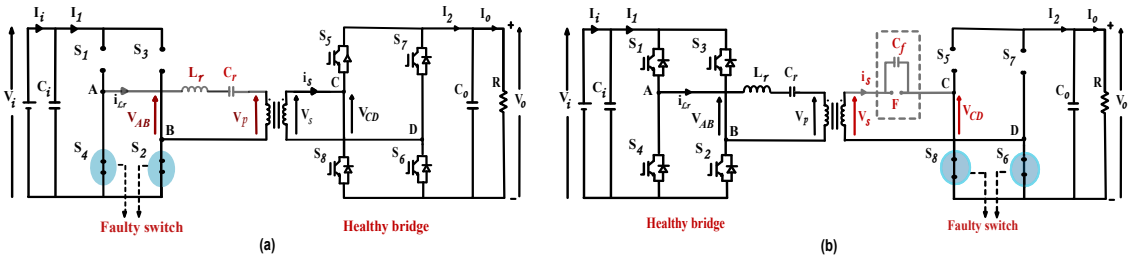



**Figure 4.1:** Two switch short-circuit faults on (a) primary side (m ≤ 4, n ≤ 4), and (b) secondary side (5≤ m & n ≤ 8).

## 4.2 Two switch faults in SRC

A converter can also suffer from two switches undergoing failure. The same concept of using a fault-tolerant capacitor, $C_f$ to remove the DC component from the current as discussed in Section 3.3 is adopted for selected combination of two switch faults, providing a common fault-tolerant feature in the post-fault correction. Here, the self-reliant feature of the FT converter depends upon different combinations of switch faults which can occur simultaneously or one after the other on the same/different sides of the converter. All the possible combinations of two switch faults ($S_m$, $S_n$) are listed in Table 4.1. All two switch fault cases are categorised into three broad categories: primary side faults ( orange color), secondary side faults ( green color), and alternate side faults ( yellow color). Here, the diagonal combinations for $m = n$ highlighted with blue color in the table are invalid cases. All the cases are detailed below.

### 4.2.1 Two switch faults on the primary side (m ≤ 4, n ≤ 4)

The converter is able to withstand a single switch SC or OC fault as discussed in Section 3.3. On the occurrence of a second fault, the supply side gets disconnected from the transformer and load as shown in Fig. 4.1(a). The converter is not self-reliant for two switches undergoing OC or SC fault on the primary side (combinations mentioned in Table 4.1). Thus, the proposed correction cannot be applied to two switch faults on the primary side. The continuous converter operation can only be ensured by providing a redundant leg or converter with additional components used for connecting the redundant circuitry in the post-fault correction.

### 4.2.2 Two switch faults on the secondary side (5≤ m & n ≤ 8)

The converter can handle two switches undergoing fault on the secondary side. Two SC faults cannot be corrected as they will disconnect the transformer's secondary from the load as shown in Fig. 4.1(b). While two switches undergoing OC fault can be corrected with the proposed post-fault

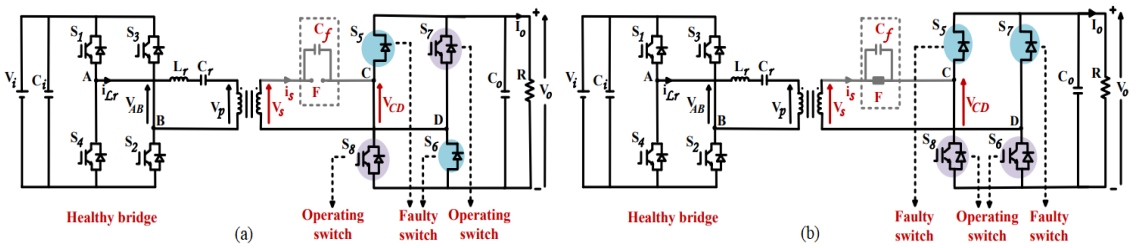



**Figure 4.2:** Two switch open-circuit fault correction on secondary side $(5 \leq m \ \& \ n \leq 8)$ for (a) $S_5$ and $S_6$ fault (diagonal switches), and (b) $S_5$ and $S_7$ fault (adjacent switches).

correction. Here, the self-reliant feature for two switch OC fault on the secondary side depends on the type of fault combinations like diagonal switches, adjacent switches and switches of the same leg.

#### 4.2.2.1 OC fault on the diagonal switches

When a single switch OC fault occurs on the secondary side, additional components are not required in the post-fault correction as mentioned in Section 3.3. When the second OC fault occurs on the diagonal switch, a DC shift is observed in $i_s$. To remove this DC component from current, the same reconfiguration used for a single switch SC fault will work well which includes the addition of $C_f$ in the circuit. Thus, the converter does not possess a self-reliant feature for faults occurring on the diagonal switches. Consider, $S_5$ and $S_6$ has suffered from an OC fault. A DC component is observed in $i_s$ after the second fault. The secondary side FB is converted to HB by shorting the switch $S_8$. The duty cycle during $T_f$ duration is adjusted to decrease the sudden peak observed on the formation of half-bridge as discussed in Section 3.3. Ultimately the fuse $F$ blows off and $C_f$ is connected in the circuit as shown in Fig. 4.2(a). In this case, the HB is again converted to FB by giving healthy pulses to the switch $S_8$ (after $C_f$ is connected in the circuit). The post-fault configuration maintains the continuity in operation and provides the pre-fault voltage at the load. In the post-fault condition, the converter is able to achieve ZCS at both the turn-on and turn-off of the switch.

#### 4.2.2.2 OC fault on the adjacent switches

When two switches undergoing open-circuit fault are adjacent, there is no DC shift observed in $i_s$ (after the second fault) and the converter is able to maintain its operation without a significant dip in the output voltage and power. Hence SRC is self-reliant for OC faults occurring on the adjacent switches. Suppose, $S_5$ and $S_7$ suffered from OC fault, the post-fault condition is similar to the pre-fault condition ($F$ connected) as shown in Fig. 4.2(b). In the post-fault condition, the rated

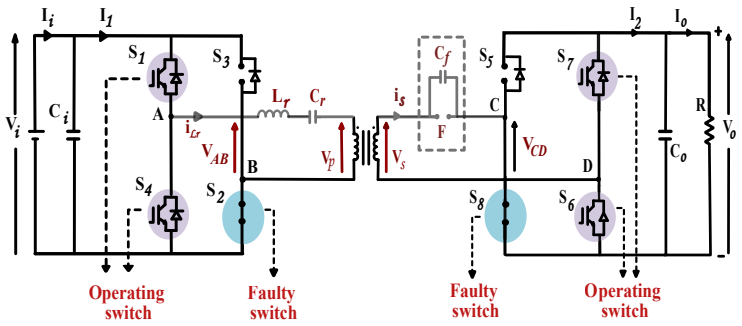



**Figure 4.3:** Two switch OC/SC fault on the alternate side of SRC (1 ≤ m ≤ 4 and 5 ≤ n ≤ 8) or (5 ≤ m ≤ 8 and 1 ≤ n ≤ 4)

output voltage ($V_o$) and power are achieved at the load. Also, the converter is able to achieve ZCS at both turn-on and turn-off.

#### 4.2.2.3 OC fault on switches of the same leg

When two switches undergoing open-circuit fault are switches of the same leg, there is no DC shift observed in $i_s$ (after both switch faults). Suppose, $S_5$ and $S_8$ suffered from OC fault. The converter operates without a significant dip in the output voltage and power. Hence SRC retains the self-reliant characteristic for two switch OC fault occurring on the same leg with no additional component required in the post-fault condition. Also, the converter is able to maintain ZCS at the turn-on and turn-off operation of the switch.

### 4.2.3 Two switch OC/SC fault on the alternate side of SRC (1 ≤ m ≤ 4 and 5 ≤ n ≤ 8) or (5 ≤ m ≤ 8 and 1 ≤ n ≤ 4)

When two switches undergoing fault on the alternate side of the converter (combinations mentioned in Table 4.1), the output voltage obtained is either half or negligible. In this case, the self-reliant feature depends on the type of the fault occurring on the secondary side. For a SC/OC fault on the primary side and an OC fault on the load side, half of the pre-fault voltage is achieved at the load (without post-fault correction) without any DC shift in $i_s$. The post-fault correction for this case is similar to the post-fault correction mentioned in Section 3.3. Whereas for a SC/OC fault on the primary side and SC fault on the secondary side, negligible voltage and power is achieved at the load (without correction) due to a DC component in $i_s$. The post-fault correction for this case is similar to the post-fault correction mentioned in Section 3.3. Hence the correction for alternate side faults uses the addition of $C_f$ in the circuit for some of the fault cases that includes a SC fault on the secondary side.

Consider, $S_2$ on the primary side has suffered from an SC fault. Later $S_8$ has also suffered from an SC fault as shown in Fig. 4.3. Here, switch $S_3$ and $S_5$ are opened by the protection circuitry. The post-fault reconfiguration (after the fault on $S_8$) includes connecting $C_f$ in the circuit (fuse $F$ is open) to remove the DC offset in $i_s$. The converter retains the soft switching in the turn-on and turn-off operation of the switches in the post-fault correction. A load reduction of around 25 % is required to achieve the rated output voltage for two SC faults on the alternate side of the converter.

## 4.3 Two Switch Faults in DAB

A DAB converter, like SRC, might suffer from the two switch failures. As mentioned in the previous section, the SRC has a self-reliant feature for the faults that allows the converter to function without the need for additional hardware. The existence of the resonant converter alters the behaviour of the converters towards faults, as demonstrated in Chapters 2 and 3 of the thesis. As a result, the set of faults for which the self-reliant characteristic is attained differs for DAB and SRC. DAB converter is not self-reliant for single switch OC/SC failure since an unacceptable DC shift in the current is observed when a SC/OC fault occurs on the primary or secondary side. As a result, it is also not self-reliant for two switch faults. All the possible combinations of two switch faults ($S_p$, $S_q$) are listed in Table 4.2. All two switch fault cases are categorised into three broad categories: primary side faults ( orange color), secondary side faults ( red color), and alternate side faults ( yellow color). Here, the diagonal combinations for $p = q$ highlighted with blue color in the table are invalid cases.

### 4.3.1 Two switch faults on the primary side ($p \leq 4, q \leq 4$)

The DAB converter does not have a self-reliant feature for a single switch SC or OC fault on the primary side beacuse of the DC shift produced in the current ($i_{Lr}$), as discussed in Section 2.3. On

**Table 4.2:** Possible combinations of two switch OC/SC faults in DAB

| $p \times q$ | q=1 | q=2 | q=3 | q=4 | q=5 | q=6 | q=7 | q=8 |
|---|---|---|---|---|---|---|---|---|
| p=1 | $S_1, S_1$ | $S_1, S_2$ | $S_1, S_3$ | $S_1, S_4$ | $S_1, S_5$ | $S_1, S_6$ | $S_1, S_7$ | $S_1, S_8$ |
| p=2 | $S_2, S_1$ | $S_2, S_2$ | $S_2, S_3$ | $S_2, S_4$ | $S_2, S_5$ | $S_2, S_6$ | $S_2, S_7$ | $S_2, S_8$ |
| p=3 | $S_3, S_1$ | $S_3, S_2$ | $S_3, S_3$ | $S_3, S_4$ | $S_3, S_5$ | $S_3, S_6$ | $S_3, S_7$ | $S_3, S_8$ |
| p=4 | $S_4, S_1$ | $S_4, S_2$ | $S_4, S_3$ | $S_4, S_4$ | $S_4, S_5$ | $S_4, S_6$ | $S_4, S_7$ | $S_4, S_8$ |
| p=5 | $S_5, S_1$ | $S_5, S_2$ | $S_5, S_3$ | $S_5, S_4$ | $S_5, S_5$ | $S_5, S_6$ | $S_5, S_7$ | $S_5, S_8$ |
| p=6 | $S_6, S_1$ | $S_6, S_2$ | $S_6, S_3$ | $S_6, S_4$ | $S_6, S_5$ | $S_6, S_6$ | $S_6, S_7$ | $S_6, S_8$ |
| p=7 | $S_7, S_1$ | $S_7, S_2$ | $S_7, S_3$ | $S_7, S_4$ | $S_7, S_5$ | $S_7, S_6$ | $S_7, S_7$ | $S_7, S_8$ |
| p=8 | $S_8, S_1$ | $S_8, S_2$ | $S_8, S_3$ | $S_8, S_4$ | $S_8, S_5$ | $S_8, S_6$ | $S_8, S_7$ | $S_8, S_8$ |

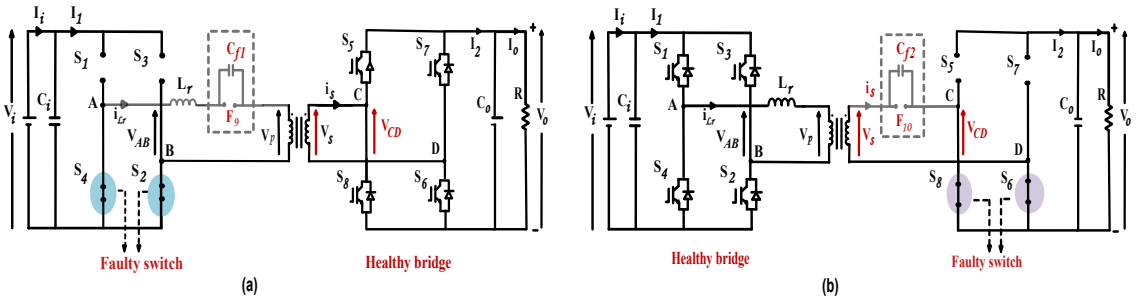



**Figure 4.4:** Two switch short-circuit faults on (a) the primary side $(p \leq 4, q \leq 4)$, and (b) the secondary side $(5 \leq p \,\&\, q \leq 8)$ of DAB.

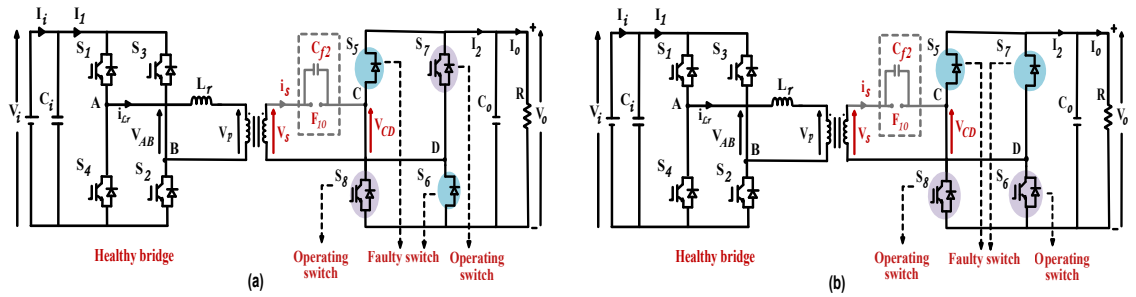



**Figure 4.5:** Two switch open circuit fault correction on secondary side $(5 \leq p \,\&\, q \leq 8)$ for (a) $S_5$ and $S_6$ fault (diagonal switches), and (b) $S_5$ and $S_7$ fault (adjacent switches) of DAB.

the occurrence of a second fault, the supply side gets disconnected from the transformer and load as shown in Fig. 4.4(a). The converter is not self-reliant for two switches undergoing OC or SC fault on the primary side (combinations mentioned in Table 4.2). Thus, the proposed correction cannot be applied to two switch faults on the primary side. The continuous converter operation can only be ensured by providing a redundant leg or converter with additional components for the second fault correction.

### 4.3.2 Two switch faults on the secondary side $(5 \leq p \,\&\, q \leq 8)$

The DAB is not self-reliant in the event of a single switch OC/SC failure on the secondary side due to the presence of the DC offset in $i_s$. A fault-tolerant capacitor is connected on the secondary side for single switch post-fault correction, as shown in Chapter 2. As a result, the converter will be disconnected from the load if the second SC fault occurs as shown in Fig. 4.4(b). The second fault necessitates the use of a redundant leg.

The two switches undergoing OC fault can be corrected with the proposed post-fault correction as shown in Fig. 4.5(a) and (b) as similar to the SRC. However, the DAB converter is not self-reliant for any of the secondary side faults, whether single/two switch OC or SC fault. The first

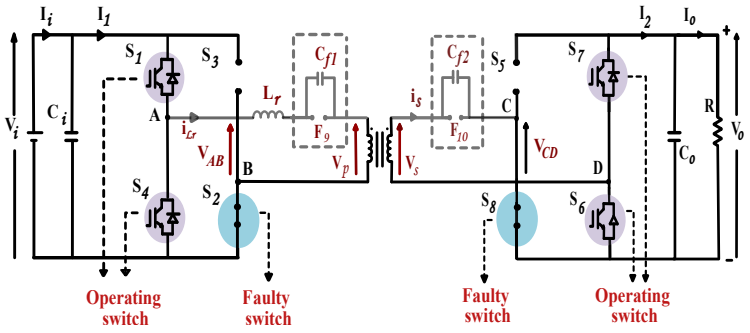



**Figure 4.6:** Two switch OC/SC fault on the alternate side of DAB (1 ≤ m ≤ 4 and 5 ≤ n ≤ 8) or (5 ≤ m ≤ 8 and 1 ≤ n ≤ 4)

fault can be repaired by inserting $C_{f2}$ into the secondary side of the converter, whilst the second OC fault correction on the same side requires variation of the control parameters to obtain the rated voltage on the load. Ultimately, the control parameter variation for two switch OC faults in DAB can be obtained from the two switch OC fault in SRC. Thus, this topic is not covered in this section.

### 4.3.3 Two switch OC/SC fault on the alternate side of DAB (1 ≤ p ≤ 4 and 5 ≤ q ≤ 8) or (5 ≤ p ≤ 8 and 1 ≤ q ≤ 4)

The overall proposed method is tested for the ruggedness of the DAB converter by adding $C_{f1}$ and $C_{f2}$ both for two switch SC or OC fault correction on the alternate side as shown in Fig. 4.6. At any point of time, for two switch fault correction, only one switch on the primary side and one switch on the secondary side can be reconfigured using the proposed approach.

For two switch faults on the alternate side of the converter, consider $S_2$ and $S_8$ SC fault. Switch $S_3$ and $S_5$ are opened by the protection circuitry. The half-bridge will be formed on both the primary and the secondary side of the converter. Thus, $V_{AB}$ and $V_{CD}$ are HB voltages. Here, the post-fault correction is executed by adding $C_{f1}$ and $C_{f2}$ in the circuit as depicted in Fig. 4.6. With the proposed correction, the converter is able to sustain the rated $V_o$ at the output with reduced load.

## 4.4 Experimental Results

To validate the self-reliant characteristic in the converter, a prototype of DAB and SRC employing Semikron IGBT switches is developed with single-phase shift (SPS) control as shown in Fig. 2.11 and Fig. 3.6. The parameters of the prototype are mentioned in Table 2.2 and 3.1. The transient

analysis (for all the fault cases) and the steady-state analysis (for two switch fault combinations) is shown at an input voltage of 100 V for safety reasons.

### 4.4.1 Faults on the secondary side of SRC (5≤ m & n ≤ 8)

Two SC faults cannot be repaired as they will separate the secondary side of the transformer from the load as explained in Fig. 4.1. While the proposed post-fault correction can correct two switches experiencing an OC fault.

#### 4.4.1.1 Faults on diagonal switches

Consider, $S_5$ and $S_6$ suffer from an open-circuit fault (circuit shown in Fig. 4.2(a)), a DC shift is observed in $i_s$ (after the second fault) as shown in Fig. 4.7(a). Here, transition I indicates healthy to $S_5$ open-circuit fault while transition II indicates the changeover from $S_5$ OC fault to $S_5$ and $S_6$ OC fault without correction. Hence the converter is not self-reliant for $S_5$ and $S_6$ OC fault (simultaneous or one after the other). To remove the DC shift from $i_s$, switch $S_8$ is shorted and the fuse $F$ blows off. After $C_f$ is added in the circuit, healthy pulses are again given to the switch $S_8$ (shown in Fig. 4.2(a)). The transition from healthy condition to faulty condition (Transition I) and faulty condition to post-fault correction with $T_f$ duration is shown in Fig. 4.7(b). The steady-state results for $S_5$ and $S_6$ OC faults are shown in Fig. 4.7(c). Here, the output voltage and power obtained in post-fault correction is equal to the pre-fault values with ZCS achieved in all the switches.

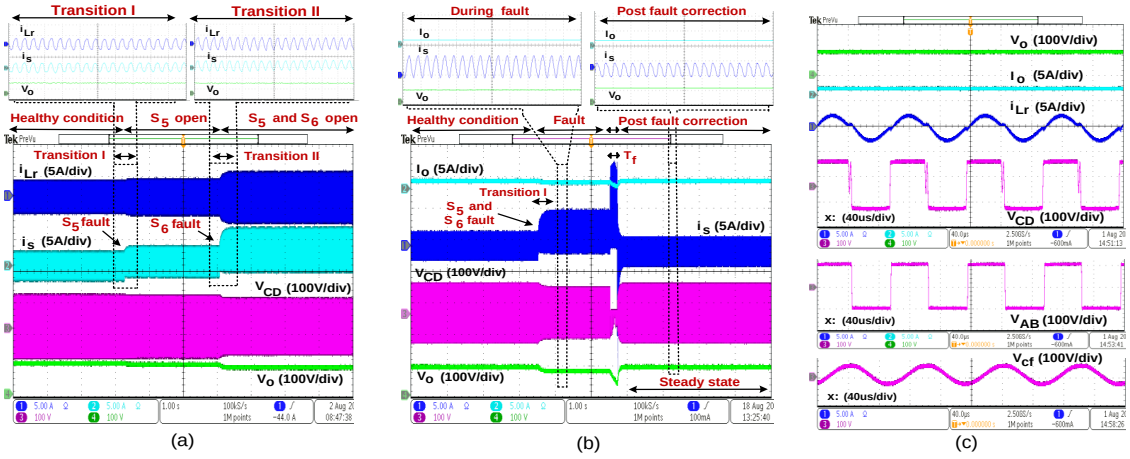



**Figure 4.7:** Experimental results of $S_5$ and $S_6$ open-circuit fault (a) transition from healthy to post-fault condition without correction, (b) transition from healthy to post-fault condition with correction, and (c) steady-state post-fault correction results at $V_i$ = 100 V in SRC.

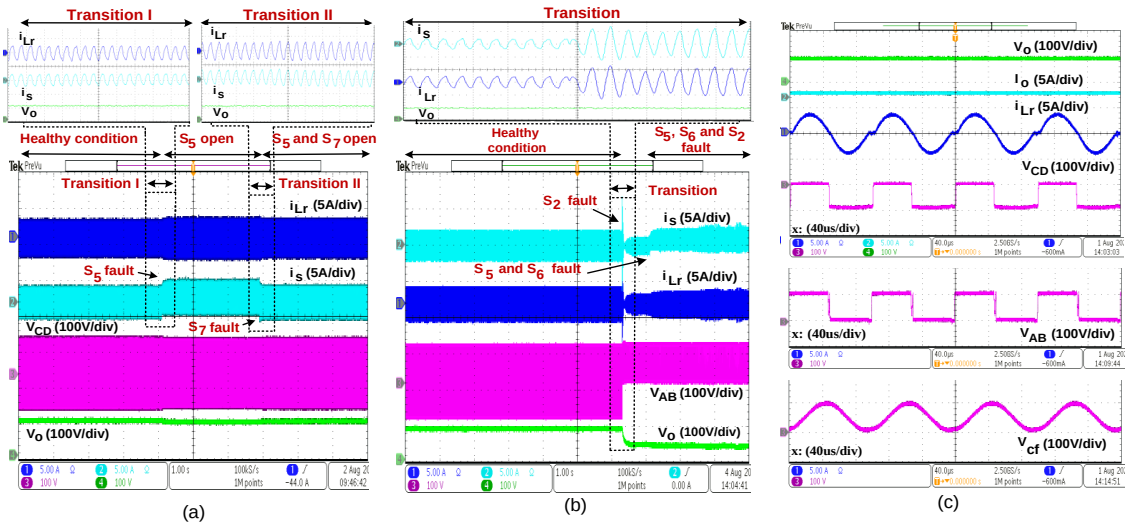



**Figure 4.8:** Experimental results of transition from healthy to post-fault condition without correction for (a) $S_5$ and $S_7$ OC fault, (b) $S_2$ SC fault, $S_5$ and $S_6$ OC fault, and (c) steady-state post-fault correction results of $S_2$ SC fault, $S_5$ and $S_6$ OC fault for reduced load at $V_i$ = 100 V in SRC.

#### 4.4.1.2 Adjacent switch faults

Consider, $S_5$ and $S_7$ both suffer from open-circuit fault. No DC component is observed in $i_s$ or $i_{Lr}$ (after the second fault) as shown in Fig. 4.8(a). The output voltage ($V_o$) and current ($I_o$) in the post-fault condition are similar to the pre-fault values (circuitry shown in Fig. 4.2(b)). Hence the converter possess a self-reliant feature for $S_5$ and $S_7$ OC fault as indicated in Fig. 4.8(a).

### 4.4.2 Two switch OC/SC fault on the alternate side of SRC ($1 \leq m \leq 4$ and $5 \leq n \leq 8$) or ($5 \leq m \leq 8$ and $1 \leq n \leq 4$)

There are various combinations of faults occurring on the alternate side as shown in Table 4.1. Here, it is considered for n=5, 6 & m=2. Consider, $S_2$ (m = 2) suffered from a short-circuit fault, $S_5$ and $S_6$ (n = 5 and 6) from open-circuit faults. The output voltage $V_o$ reduces to half of the pre-fault voltage after the occurrence of $S_2$ SC fault. A DC shift is also observed in $i_s$ (after the occurrence of $S_5$ and $S_6$ OC fault) as shown in Fig. 4.8(b). The steady-state post-fault correction results are shown in Fig. 4.8(c). The $V_{AB}$ and $V_{CD}$ are half- bridge voltages with desired output voltage ($V_o$) achieved at the load.

### 4.4.3 Faults on the secondary side of DAB ($5 \leq p$ & $q \leq 8$)

On occurrence of single OC fault on the secondary side, the proposed fault-tolerant method connects $C_{f2}$ on secondary side of the converter to obtain a ceaseless operation. Control parameter

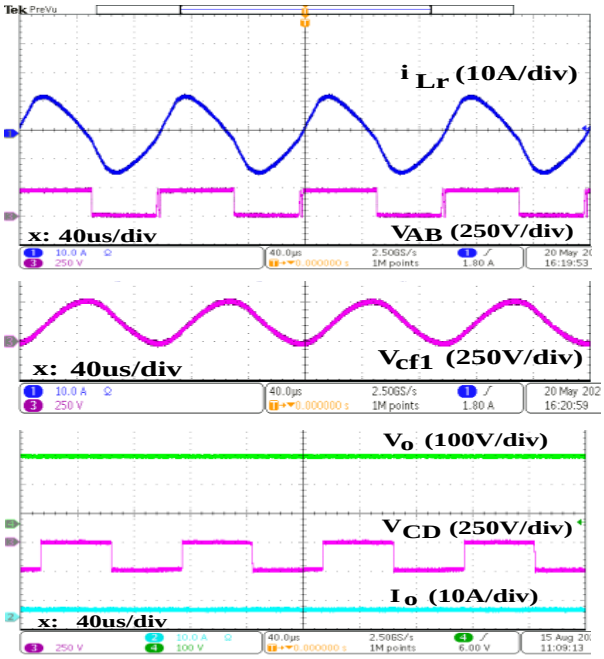



**Figure 4.9:** Steady-state experimental results of $S_2$ and $S_8$ SC fault correction.

variation is adopted to obtain the rated voltage at the output. The DAB converter, similar to SRC, will be able to achieve the rated voltage at the output on the occurrence of a second OC fault (whether on the same leg, an adjacent switch fault, or a diagonal switch fault). The fault-tolerant capacitor is already present in the circuit as a preventative measure for the first failure (as shown in Chapter 2), thus when the second OC fault occurs on the same side, the $i_s$ will also be free from the DC offset. As a result, when the two OC failures on the secondary side of the DAB occur, the continuous converter operation with rated output voltage is achieved.

### 4.4.4 Two switch OC/SC fault on the alternate side of DAB ($1 \leq p \leq 4$ and $5 \leq q \leq 8$) or ($5 \leq p \leq 8$ and $1 \leq q \leq 4$)

The proposed method is tested for the ruggedness of the DAB converter by adding $C_{f1}$ and $C_{f2}$ for two switch SC or OC fault correction. At any point of time, for two switch fault correction, only one switch on the primary side and one switch on the secondary side can be reconfigured using the proposed approach.

For two switch faults on the alternate side of the converter (consider $S_2$ and $S_8$ SC fault as shown in Fig. 4.6), the steady-state results are shown in Fig. 4.9 at rated voltage. The half-bridge will be formed on both the primary and the secondary side of the converter. Thus, $V_{AB}$ and $V_{CD}$ are HB voltages. Here, the post-fault correction is executed by adding $C_{f1}$ and $C_{f2}$ in the circuit. With

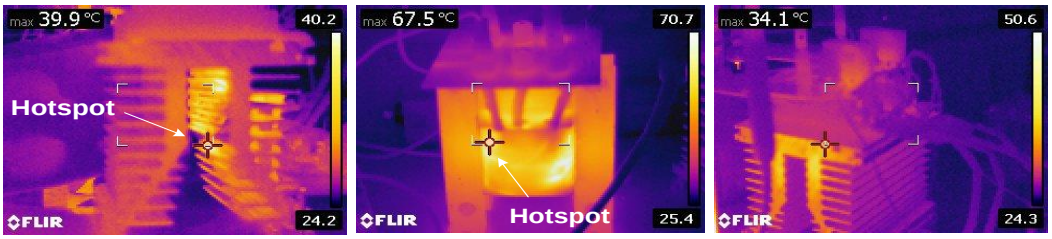



**Figure 4.10:** Thermal picture of the (a) primary side switches with heat sink, (b) transformer, and (c) secondary side switches with heat sink after $S_5$ and $S_6$ OC fault correction.

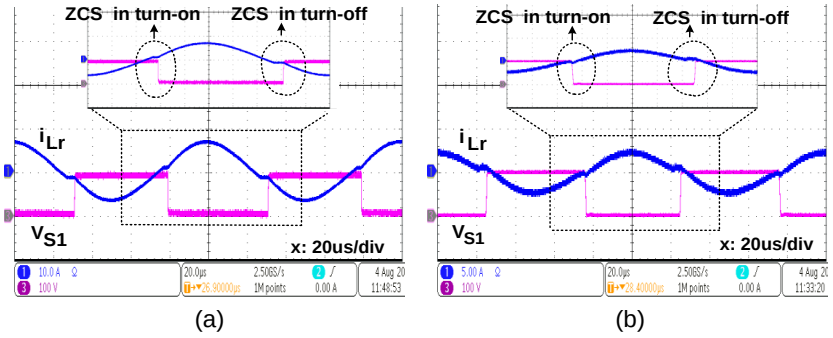



**Figure 4.11:** Soft-switching in primary side switches for (a) $S_8$ SC fault correction (b) $S_5$ and $S_6$ OC fault correction in SRC.

the proposed correction, the converter is able to sustain the rated $V_o$ at the output with reduced load as shown in Fig. 4.9.

### 4.4.5 Thermal stress on the components

For the considered system, the thermal stress on the various components is observed by taking thermal picture using FLIR E40 thermal camera. Here, the thermal scanning of the converter components is shown after the post-fault correction of two switch faults.

The maximum temperature of the components after the correction of $S_5$ and $S_6$ OC fault is depicted in Fig. 4.10(a)-(c) which includes the thermal picture of the primary side switches mounted on the heat sink, the transformer, and the secondary side switches mounted on the heat sink. In Fig. 4.10(a), the maximum temperature of the primary side heat sink is 39.9°C. In Fig 4.10(b), the hotspot temperature on the transformer is 67.5°C. In Fig 4.10(c), the secondary side switches have a maximum temperature of 34.1°C. In this case, both the primary and secondary sides of the converter are full-bridges. The corresponding soft-switching results during switch turn-on and turn-off are shown in Fig. 4.11. Thus, the stress during switching is considered negligible.

**Table 4.3:** A comparison of maximum temperature in various cases

| Cases | Primary side heat sink | Transformer | Secondary side heat sink |
|---|---|---|---|
| Healthy condition | 34.3°C | 49.8°C | 29.1° C |
| $S_5$ and $S_6$ OC fault correction | 39.9°C | 67.5°C | 34.1°C |

A comparison of the maximum temperature in case of healthy condition and the post-fault correction of two switch OC fault on the secondary side is given in Table 4.3. In both the cases, it is observed that the maximum temperature of the transformer is higher as compared to the switches thus, the transformer incorporates the maximum losses in the circuit. Also, the converter components should be designed for two times the pre-fault current value to transfer the maximum power during the half-bridge formation. The detailed design of the transformer for such cases is given in [10].

## 4.5 Conclusion

In this work, the self-reliant characteristic of DAB and SRC along with the post-fault correction for single semiconductor short/open-circuit fault and selected combinations of two switch faults is presented. For two switch fault cases, the fault-tolerant and self-reliant feature in the converter depends upon the combination of switches undergoing failure.

The advantages of the proposed post-fault correction are its application to achieve continuity of operation and overall fault tolerance in SRC and DAB converters with the reduced number of additional components. With the proposed analysis and the post-fault correction schemes:

- Single switch OC/SC fault, two semiconductor faults (OC/SC) on the alternate side of the converter, and two switch OC faults on the secondary side of DAB and SRC are corrected.
- Uses only one extra fuse and one FT capacitor in case of SRC to achieve uninterrupted operation of the converter along with soft-switching and the desired voltage at the load.

For the two switch faults in the DAB converter, a similar analysis is expanded. The experimental results for two switch fault analyses are obtained for a 1 kW SRC and DAB converter for various fault cases to indicate the effectiveness of the proposed work.

# Chapter 5

# A Fault-Tolerant Single-Phase Inverter with Extended Electrolytic Capacitor Lifetime

## 5.1 Introduction

The emerging technologies in the field of solid-state transformer, motor drive applications, uninterruptible power supply (UPS), PV, etc. demands a reliable inverter. A failure of the inverter components can lead to immediate shutdown of the system. In critical applications like military, hospitals and financial markets, system shutdown may lead to huge economic losses [55, 56]. Thus, a fault-tolerant feature is of uttermost importance as it maintains a continuous operation and ensures the reliability of an inverter.

The fault-tolerant method for inverters are widely studied in literature [16, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72]. Redundancy is one such method which improves the reliability of the whole system [16, 21, 73]. Switch level redundancy, leg level redundancy [22], and module level redundancy are widely adopted in literature. Redundant legs are used in parallel connection or series connection with main legs [61, 62]. Redundant parallel leg consists of two schemes: online leg scheme and offline leg scheme. In offline parallel leg scheme, a single redundant leg is connected in parallel and is being shared with rest of the three main legs (for a three-phase inverter). However, this type of topology can tolerate a fault happening only in one phase. Although three redundant legs for a three-phase inverter and two redundant legs for a single-phase inverter can potentially be utilised (one for each phase) for a more reliable operation, this would increase the overall cost of the system. The redundant leg being used is always inactive before fault. Whenever a fault occurs, the faulty leg is replaced by the redundant leg with the

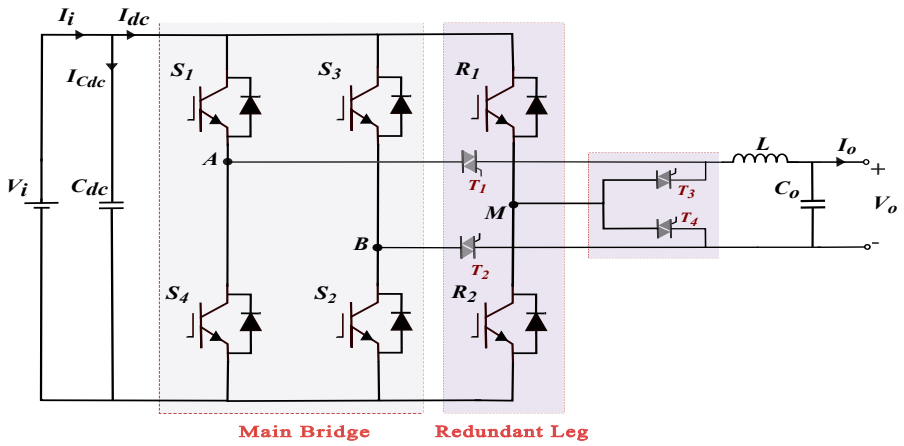



**Figure 5.1:** Circuit configuration of a single-phase inverter with a redundant leg.

help of TRIACs which are used as linking switches [62, 63]. In online leg scheme, even in normal conditions the redundant leg operates. Thus, it improves the overall system behavior by improving the output quality.

Switch level redundancy is generally provided in multilevel inverters or converters. There are three types of switch-level redundancies: redundant switching states [57, 71, 72], DC-bus mid point connection [74] and redundant parallel or series switch installation. A multilevel converter can be realised as a two-level converter with a few redundant switches to achieve fault tolerance. The disadvantage of this method includes the increased conduction losses, degraded performance during post-fault conditions, and doubling of the device blocking voltage for some of the switches. In DC-bus mid-point connection, the faulty leg is connected with the help of additional auxiliary switches to the mid-point of the DC-bus. The DC-bus replaces the faulty leg under faulty condition [74]. When the faulty phase is connected to the mid-point of the DC-link, the output line-to-line voltage in the post-fault condition reduces to half. In addition, oversized DC-bus capacitors are required due to the flow of phase currents through the mid-point point of the DC-bus. In redundant parallel or series switch installation, the extra switches are used as redundant switches in series or parallel with the converter switches. While using redundant switches in series, the conduction loss would increase many folds because of the continuous conduction of the redundant switches even in the healthy condition. Thus, the methods mentioned in literature have large number of components, complexity in control, and limitation in correction of different faults using redundant fault-tolerant methods.

Similar to a three-phase inverter, fault tolerance can also be achieved for a single-phase inverter with redundancy for switch failures. The circuit configuration of a single-phase two-level inverter with redundancy is shown in Fig. 5.1. The fundamental circuit consists of four switches, $S_1$-$S_4$,

which together with the DC-link capacitor, $C_{dc}$, create the traditional full-bridge inverter. The output side filter is made up of an inductor, $L$, and a capacitor, $C_o$. The switches, $R_1$-$R_2$, and the TRIACs, $T_1$-$T_4$, are introduced as a part of the redundant leg circuitry to achieve the fault tolerance in the inverter. When a fault occurs, the switches $R_1$ and $R_2$ provide the necessary fault tolerance by replacing the faulty leg. This turns out to be a very effective way to increase the converter's reliability under the influence of semiconductor faults. However, this approach suffers the following challenges:

- **Maximum utilization of the redundant leg**: The circuit shown in Fig. 5.1 has a redundant leg which is inactive in the pre-fault condition. Thus, the maximum utilization of the redundant leg is not achieved.
- **Cost of the redundant leg circuitry** including switches and the connecting devices is not justified since the redundant leg is used only in the post-fault correction.
- **dV/dt triggering of TRIACs**: The TRIACs $T_3$ and $T_4$ are subjected to a voltage $V_{AB}$ that is PWM in nature. This TRIAC configuration results in a short-circuit across the terminals A and B which is not desirable.

Therefore, a successful post-fault correction for switch failures (constitute 21% of the total faults occurring in the inverter) can only be achieved if the TRIACs do not experience false dV/dt triggering and the cost can be justified if the redundant leg can be used even in the pre-fault condition.

Another key component in converter failure is the DC-link capacitor faults, which was mentioned in Chapter 1. A number of variables, including the operating voltage, ambient temperature during the particular application, and the ripple current, have an impact on the lifetime of the DC-link capacitor. Electrolytic capacitors (E-caps), which have a relatively high capacitance-to-volume ratio and low-cost, are used primarily in the DC bus design of single-phase power electronics systems. As the large capacitance offered by E-caps effectively attenuate the double line frequency ripple power that is an inherent characteristic of single-phase systems [75]. The AC power delivered to the load in case of single-phase inverter is given by

$$P_{ac}(t) = v_{ac}(t) i_{ac}(t). \tag{5.1}$$

where the instantaneous voltage and current on the AC side are:

$$v_{ac} = V_{max} sin(\omega t) \tag{5.2}$$

,and

$$i_{ac} = I_{max} sin(\omega t). \tag{5.3}$$

On simplification, $P_{ac}$ [76] is given by

$$P_{ac} = \frac{V_{max} I_{max}}{2} - \frac{V_{max} I_{max}}{2} cos(2\omega t). \tag{5.4}$$

There are two parts in (5.4), namely the average (DC) component, $P_o$ and the AC (pulsating) component, $P_{ac-pulsation}$. The $P_{ac}$ in terms of $P_o$ and $P_{ac-pulsation}$ is expressed as

$$P_{ac}(t) = P_o + P_{ac-pulsation} = P_o + P_o cos(2\omega t). \tag{5.5}$$

To filter the second harmonic ripple (SHR) current produced due to single-phase power processing, it is inevitable to use electrolytic capacitors to realize a cost-effective and power dense single-phase inverter. Failures in electrolytic capacitors (component with the highest failure rate) are due to design defects, excessive operational temperatures, increased current and voltage stresses, etc [77, 78]. The catastrophic breakdown of the capacitor or the capacitor's long-term degeneration could both be the cause of the capacitor failure. According to [77], using an active ripple reduction circuit in parallel with a DC-link capacitor will lessen the ripple current processed by the capacitor. As a result, the E-cap can be replaced with a long-life film capacitor. In applications like PV inverters or wind turbines, the environmental factors like solar irradiance profile or wind speed profile along with the ambient temperature causes an impact on the ripple current stress on the DC-link. As a result, when determining the minimum capacitance value, various environmental factors must be considered. A minimum value of DC-link capacitance is always required, taking hold-up duration into account. Thus, replacing E-caps with long-lasting film capacitors may not be appropriate for all applications. Hence for several applications, it is crucial to increase the DC-link capacitor's reliability and the lifetime. Consider an example of a 1 kW converter with a voltage rating of 400 V and a 20 ms hold-up period, the required DC-link capacitance is 650 uF approximately. An electrolytic capacitor from the $TDK-EPCOSB$43508 series with 55 $cm^3$ volume can be used as the DC-link capacitor. In contrast, 16 film capacitors ($TDK-EPCOSB$32678) can be used to attain the same capacitance value, capturing a volume of 1600 $cm^3$, which is significantly larger than the electrolytic capacitors. Thus, as a result of the high capacitance value, high energy density, and low cost, electrolytic capacitors are typically used as the DC-link capacitors. However, they have greater equivalent series resistance (ESR), smaller ripple current capacity, and shorter lifespan. These capacitors experience self-heating due to the large ripple current flowing through them, raising the hot-spot temperature, $T_h$, as indicated by

$$T_h = T_o + R_H \sum_{n=1}^{k} [ESR(f_n) I^2_{ripple}(f_n)] \tag{5.6}$$

where $T_o$ is the ambient temperature, $R_H$ is the thermal resistant between hot-spot and ambient, $ESR(f_n)$ is the series resistance at frequency $f_n$, and $I_{ripple}(f_n)$ is the ripple current at $f_n$. The estimated lifetime of the electrolytic capacitor is indicated by

$$L = L_o (\frac{V}{V_c})^{-q} \ 2^{\frac{T_o - T_h}{10}} \tag{5.7}$$

where $L_o$ stands for rated lifespan, $V_c$ for rated voltage, $V$ for applied voltage, and $q$ for voltage stress exponent [77]. According to (5.6) and (5.7), the hot-spot temperature significantly affects the capacitor's lifespan. However, the huge ripple current is what causes the hotspot temperature to increase [76, 79, 80]. Therefore, the current ripple should be decreased in order to lengthen the lifespan and reliability of electrolytic capacitors.

The literature describes a number of steps attempting to reduce the low-frequency ripple, including the use of oversized electrolytic capacitors, the placement of active filters on the input side, ripple transfer port (with redundant components), etc. [81, 82, 83]. In [84], active power decoupling circuits are employed to reduce the capacitance requirement at the DC-link and enable the use of film capacitors, which have a longer operational lifetime compared to electrolytic capacitors. Active power decoupling techniques discussed in the literature are summarized in [81, 82, 83, 85]. The majority of these techniques, however, were implemented on the DC side, which caused the unwanted ripple power to move from the AC to the DC side, producing further losses [81]. A solution to this problem is to restrain the ripple power only on the AC side by means of the extra components. The literature suggests a number of topologies that use a ripple transfer port (with additional leg/switches), and passive components (inductors and capacitors) to minimise the DC-link capacitor voltage ripple [81, 82, 83]. Among these, the circuit architecture that employs an extra leg to prevent ripple current from going through the DC-link capacitor is the most promising.

As a result of the previous discussion, it can be concluded that a single-phase two-level inverter needs two extra legs with the connecting devices to achieve a more reliable operation. One extra leg is necessary for fault tolerance for switch failure, and the second leg is required to lower the SHR and consequently extend the electrolytic capacitor's lifetime. However, this increases the inverter's complexity in terms of the number of additional components. Therefore, in order to increase the converter's reliability toward the two most vulnerable components of the inverter, it is necessary to change the current approaches in terms of the number of components (the number of redundant legs and connecting devices).

This chapter develops a method that focuses on the two main components that are prone to failure, namely the semiconductor failure and the DC-link capacitor failure (gradual degradation or long-term degradation). By considering only one redundant leg as opposed to two, the extra hardware count is reduced. For the pre-fault situation, a control strategy is incorporated to account for the SHR through the DC-link capacitor. This would lengthen the capacitor's lifespan and slow down the gradual degeneration of the capacitor (i.e., due to the capacitor ripple current stress), thus improving the reliability of the device. Given that the capacitors and switches both are also prone to failure, the single-phase inverter's operational aspect must take into account both the pre-fault (before fault) and post-fault (after fault) conditions. Thus, an advanced control strategy should be designed for the pre-fault state that can be appropriately modified after the fault. Also, a transition scheme (from ripple compensation mode to fault-tolerant mode) and a post-fault correction approach are required, which leverages redundancy for both the pre-fault as well as the post-fault conditions (to maximize the benefits of a redundant leg).

## 5.2 Proposed Fault-Tolerant Scheme with Upgraded Capacitor Lifetime (FTUCL)

As discussed in Section 5.1, the reliability is increased by providing fault tolerance for switch failures and by prolonging the lifetime of the DC-link capacitor to avoid its long-term degradation. The proposed transition and correction scheme uses only one redundant leg (with the connecting devices), which reduces the requirement of the two extra legs used to accomplish the same objective. Fig. 5.2 shows the proposed post-fault correction scheme for a single-phase two-level inverter. The additional switches, $R_1$-$R_2$, and TRIACs, $T_1$-$T_2$, are a part of the redundant leg circuitry. $L_1$ and $L_2$ form the inductor of the output filter, while $C_{o1}$ and $C_{o2}$ constitute the output filter capacitor. An additional inductor, $L_M$, and the TRIACs, $T_3$ and $T_4$, are purposefully used in the post-fault correction to retain the normal H-bridge operation after the fault.

In the proposed scheme, the controller is designed to perform three operations: (a) pre-fault operation (or SHR compensation mode), (b) reconfiguration/preparation stage, and (c) post-fault correction (or fault-tolerant mode). The pre-fault operation is performed considering the second harmonic ripple (SHR) compensation. While the post-fault operation considers the fault-tolerant method. The transition from the pre-fault condition to the post-fault correction is accomplished by reconfiguring the inverter in the preparation stage (with the help of TRIACs $T_1$- $T_4$). The detailed discussion on the pre-fault, reconfiguration, and the post-fault operation is given in the following Section.

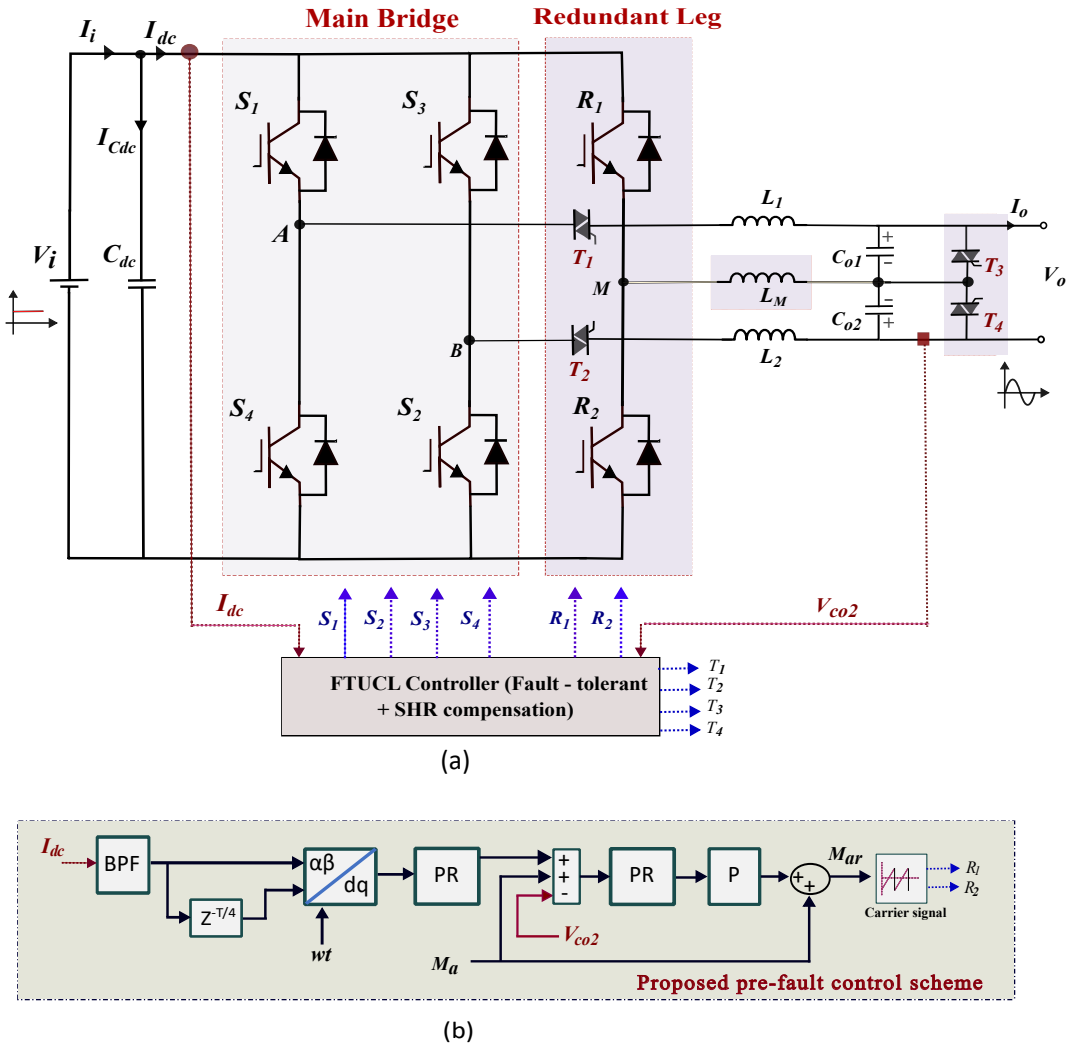



**Figure 5.2:** (a) Circuit configuration of single-phase inverter with the proposed method, and (b) proposed pre-fault control scheme.

### 5.2.1 Pre-Fault Condition

In the pre-fault condition, the redundant leg is controlled to perform the SHR compensation. The ripple compensation method discussed in [81] is extended by connecting an inductor, $L_M$, between redundant leg's pole $M$ and the mid-point of the output filter capacitors, as shown in Fig. 5.2(a). Fig. 5.2(b) illustrates the proposed scheme for SHR compensation. The controller receives the sensed current $I_{dc}$. With the help of a bandpass filter (BPF), the SHR component (i.e., 100 Hz) is extracted from the sensed signal. The transfer function, $G_{BPF}$ is given by

$$G_{BPF} = \frac{Ks}{s^2 + 2Cs + (2\pi 100)^2} \tag{5.8}$$

where $K$ and $C$ are constants. The extracted signal, $i_{2w}$ is delayed to convert the extracted SHR signal from harmonic reference ($2w$) frame to fundamental ($w$) reference frame. A proportional-resonant (PR) controller is used to control the extracted signal in the synchronous reference frame. The outer loop current controller $G_i$ is given by

$$G_i = K_p + \frac{C_1 s}{s^2 + C_2 s + (2\pi 50)^2} \tag{5.9}$$

where $C_1$ and $C_2$ are constants. Harmonic ($2w$) to fundamental ($w$) frame conversion aids in generating the modulated signal for the third leg's pulse generation for ripple compensation, together with the detected voltage signal $V_{co2}$ (controlled using another PR controller) as shown in Fig. 5.2(b). The inner loop voltage controller, $G_v$ is given by

$$G_v = K_{p1} + \frac{C_3 s}{s^2 + C_4 s + (2\pi 50)^2} \tag{5.10}$$

where $C_3$ and $C_4$ are constants. Equations (5.8), (5.9), and (5.10) show the controllers used in the pre-fault condition. The values of the constants used are: $K$=180, $2C$=100 (for BPF), $K_p$=0.5, $C_1$=100, $C_2$=1 (for $G_i$), and $K_{p1}$=0.5, $C_3$=100, $C_4$=10 (for $G_v$). When designing the controller gains, it is crucial to consider the system delays resulting from duty cycle computations and pulsewidth modulation (PWM) of the converter.

As observed in (5.7), the hotspot temperature, which in turn depends on the ripple current, determines the capacitor's lifespan. To analyze this, the power dissipation in the DC-link capacitor, $P_{C_{disspation}}$, as a function of the rms current through the capacitor is considered as [76],

$$P_{C_{disspation}} = I^2_{Cdc_{RMS}} R_{ESR} \tag{5.11}$$

where $R_{ESR}$ is the equivalent series resistance of the DC-link capacitor. $I_{Cdc_{RMS}}$ (rms current through the DC-link capacitor) has two components: (a) low-order harmonic component ($I_{LOHC}$), and (b) switching frequency harmonic component ($I_{SFHC}$), which are given by

$$I_{Cdc_{RMS}} = \sqrt{I^2_{LOHC} + I^2_{SFHC}}. \tag{5.12}$$

According to Fig. 5.2, the low-order harmonic component on the DC side, $I_{dc_{LOHC}}$, is made up of the SHR component ($I_{2w}$) entering the inverter.

$$I_{dc_{LOHC}} = \sqrt{{I_i}^2 + I^2_{2w}} = \sqrt{{I_i}^2 + I^2_{LOHC}} \tag{5.13}$$

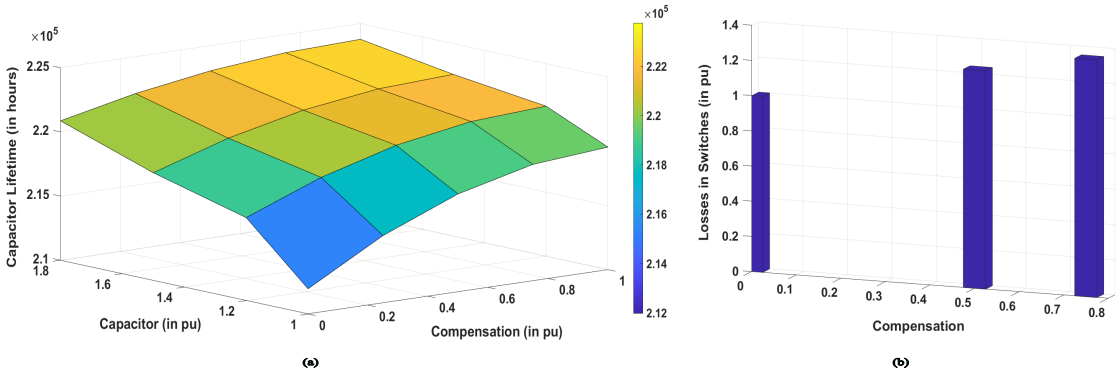



**Figure 5.3:** Graphical presentation of the (a) lifetime of DC-link capacitor with respect to the variation in capacitance and compensation of SHR, and (b) losses in switches with respect to the $I_{2w}$ compensation in the pre-fault condition.

As discussed in Section 5.1, a decrease in $I_{2w}$ will help in increasing the lifetime of the capacitor. On considering $x$ % of $I_{2w}$, the (5.12), can be modified as

$$I_{dc_{xLOHC}} = \sqrt{I_i{}^2 + (xI_{2w})^2} \tag{5.14}$$

The expression of the switching harmonic components is given in [76]. Thus, the total $I_{dc_{xRMS}}$ considering the $x$ % of the SHR is given by

$$I_{dc_{xRMS}} = \sqrt{I_i^2 + (xI_{2w})^2 + I_{SFHC}^2}. \tag{5.15}$$

The computations for $I_{2w}$ can be obtained from [76]. The actual ripple current through the capacitor with $x$ % of SHR is given by

$$I_{Cdc_{xRMS}} = \sqrt{(xI_{2w})^2 + I_{SFHC}^2}. \tag{5.16}$$

The $x$ % indicates the degree of SHR ranging from 0 % to 100 % of the original $I_{2w}$ value. For the examination of the pre-fault scenario, the following cases are considered: (a) 0 % (b) 50 %, and (c) 75 % of the SHR present in the original H-bridge inverter. While the amount of SHR compensated in the $I_{Cdc}$ is (100-$x$) %.

A number of variables, including the operating voltage, ambient temperature during the particular application, and the ripple current, have an impact on the lifetime of an electrolytic capacitor. Taking into account all of these elements, the actual lifespan is provided by [86],

$$L = L_o K_t K_r K_v \tag{5.17}$$

Here, $K_t$ stands for the temperature factor, $K_r$ stands for the ripple current factor, and $K_v$ stands for the operating voltage factor. $L_o$ is the rated lifetime at the nominal ripple current and temperature [86]. In the presented work, the ripple current factor $K_r$ is modified for various SHR compensation values ranging from 0-100 %. $K_r$ for $x$ % of SHR is provided by

$$K_r = K^{(\frac{A\Delta T_o}{10K})}, \qquad A = 1 - (\frac{I_{Cdc_{xRMS}}}{I_{nominal}})^2 \tag{5.18}$$

where $K$ is an empirical safety factor. The SHR compensated current that is passing through the capacitor is represented by $I_{Cdc_{xRMS}}$. When (5.16) is used in (5.18), the relationship between $A$ and $x$ is obtained as

$$A = 1 - \frac{((xI_{2w})^2 + I_{SFHC}^2)}{I_{nominal}^2}. \tag{5.19}$$

The benefits and drawbacks of adding an extra leg for SHR compensation are shown in Fig. 5.3. The capacitor's lifespan grows as the SHR compensation is raised from 'No compensation' to the 'maximum compensation' as shown in Fig. 5.3(a). The effects of oversizing the DC-link capacitor on its lifetime (from 1 pu to 1.8 pu) is also included in Fig. 5.3(a). As observed in Fig. 5.3(b), the losses are lower in the case of 0% compensation than in the other situations because only four active switches are operational in the circuit. The DC-link capacitor, however, has the shortest lifespan. Here, the required lifespan calculations of the DC-link capacitor are obtained using (5.17), (5.18), and (5.19), while the loss calculations are derived from thermal modeling in PLECS.

### 5.2.2 Fault Occurrence

As discussed in Section 5.2.1, the redundant leg contributes to the DC-link capacitor's longer lifespan. Due to semiconductors' high failure rate, the issue arises in the event of a switch fault. When a switch failure occurs, the pre-fault sinusoidal parameters $V_o$ and $I_o$ experience a DC shift. If the pre-fault SHR compensation is active, the $V_{co1}$ will likewise experience an undesirable DC shift. Due to the catastrophic nature of SC faults, the converter must be immediately turned off in order to protect the connected devices. However, for an OC fault, the converter can be shutdown after a few cycles. In many applications, shutting down a converter is highly undesirable. The converter's fault-tolerant feature therefore plays a crucial role in such applications. This requires the controller to reassign the pulses to the switches. Thus, to successfully complete the transition from SHR compensation mode to the fault-tolerant mode, a reconfiguration or preparation stage is required for establishing a post-fault correction mechanism for semiconductor faults.

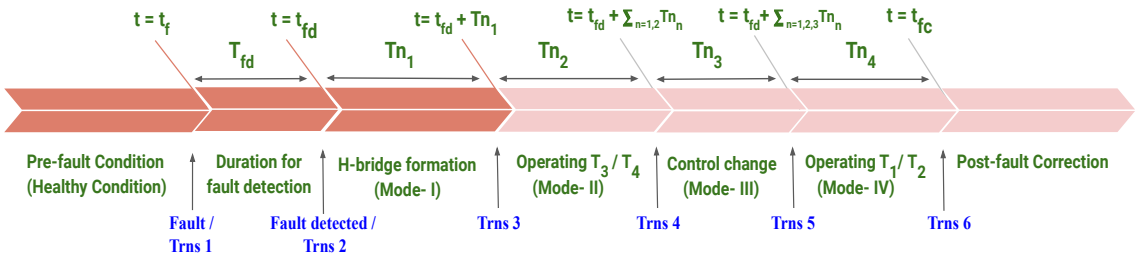



**Figure 5.4:** Timeline diagram of the proposed transition scheme.

### 5.2.3 Reconfiguration / Preparation Stage

The proposed transition from pre-fault to post-fault correction is ensured with the help of TRIACs $T_1$-$T_2$ (connected in series with $L_1$ and $L_2$), and $T_3$-$T_4$ (connected in parallel to $C_{o1}$ and $C_{o2}$). Thus, a preparation stage is required to operate the TRIACs to allow a safe transition.

A complete timeline diagram and the flowchart of the proposed transition scheme is shown in Figs. 5.4 and 5.5, respectively. The transitions (*Trns* 1 to *Trns* 6) represent the converter's gradual reconfiguration from pre-fault to post-fault correction. The converter changes from the healthy condition to the faulty condition when a fault occurs, as shown by the *Trns* 1 in Fig. 5.4. The fault diagnosis is completed in the duration $T_{fd}$. The signal from the fault diagnosis turns on the suggested reconfiguration. Let's assume there is a switch fault. $V_o$ and $I_o$ will have a DC offset when one of the switches is faulty, which is undesirable. The SHR compensation mode is still active, therefore, there will also be a DC offset for the $V_{co1}$/ $V_{co2}$ (depending on the fault location). As a result, the TRIAC installed across the capacitor is unable to function until the capacitor $C_{o1}$/$C_{o2}$, has fully discharged. In order to do this, the redundant leg's pulses at *Trns* 2 must be removed in order to deactivate the SHR compensation mode. Also, the pulses to the complementary switch in the faulty leg are removed as shown in Fig. 5.6(a). This will reduce the voltage across $C_{o1}$/ $C_{o2}$ to zero, making it safe for the TRIAC $T_3$/$T_4$ to operate (depending on the fault location). The TRIAC $T_3$/$T_4$ is successfully turned on at *Trns* 3 shown in Fig. 5.6(b). In order to establish a small zero current period of $I_{t1}$/$I_{t2}$ for securely opening the TRIAC $T_1$/$T_2$, the control pulses of the H-bridge are adjusted at *Trns* 4 (Fig. 5.6(c)). The TRIAC is safely turned off at the imminent zero crossing implemented as *Trns* 5, as shown in Fig. 5.6(d). At this point in mode-IV, the inverter is ready to implement the post-fault correction. The third leg is then given pulses that are equal to those delivered to the faulty leg in the pre-fault condition (after mode-IV). This procedure ensures a secure changeover of the inverter operation from SHR compensation mode to the post-fault correction.

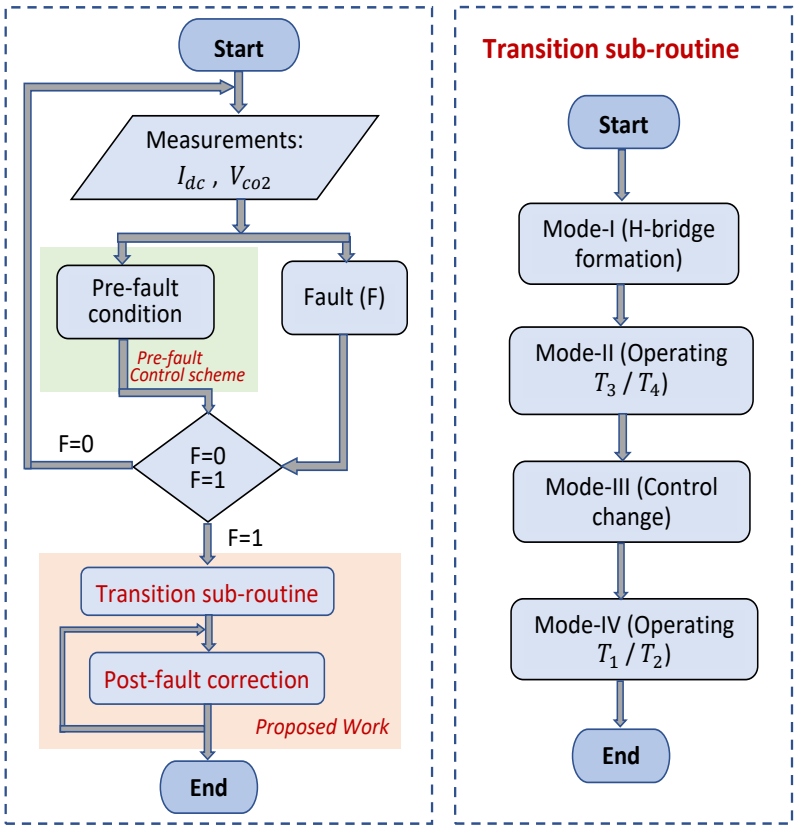



**Figure 5.5:** Flowchart of the proposed scheme with transition subroutine.

**Table 5.1:** Inverter Reconfiguration Under Various Fault Scenarios

| Faulty switch | Operative elements after reconfiguration |
|---|---|
| First leg: $S_1$ or $S_4$ | $S_2$, $S_3$, $R_1$, $R_2$, $L_2$, $L_M$, $C_{o2}$, $T_2$, $T_3$ |
| Second leg: $S_2$ or $S_3$ | $S_1$, $S_4$, $R_1$, $R_2$, $L_1$, $L_M$, $C_{o1}$, $T_1$, $T_4$ |

### 5.2.4 Proposed Post-Fault Correction

To extend the usage of the redundant leg, a post-fault correction method is implemented after the reconfiguration is completed. On occurrence of a fault in switch $S_1$ of leg 1, the controller reconfigures the operation of the inverter. The faulty leg is separated by opening the relevant TRIAC $T_1$, as indicated in Fig. 5.7. After the reconfiguration, a portion of the filter inductor, $L_1$, is eliminated. Hence, only $L_2$ and $L_M$ constitute the filter inductor, while $C_{o2}$ serves as the filter capacitor as illustrated in Fig. 5.7. On the other hand, if a fault appears in leg 2 of the main bridge, the TRIAC $T_2$ will open. In this case, the filter inductor is comprised of $L_1$ and $L_M$, whereas the total filter capacitor is comprised of $C_{o1}$, as shown in Table 5.1. In the post-fault correction, the

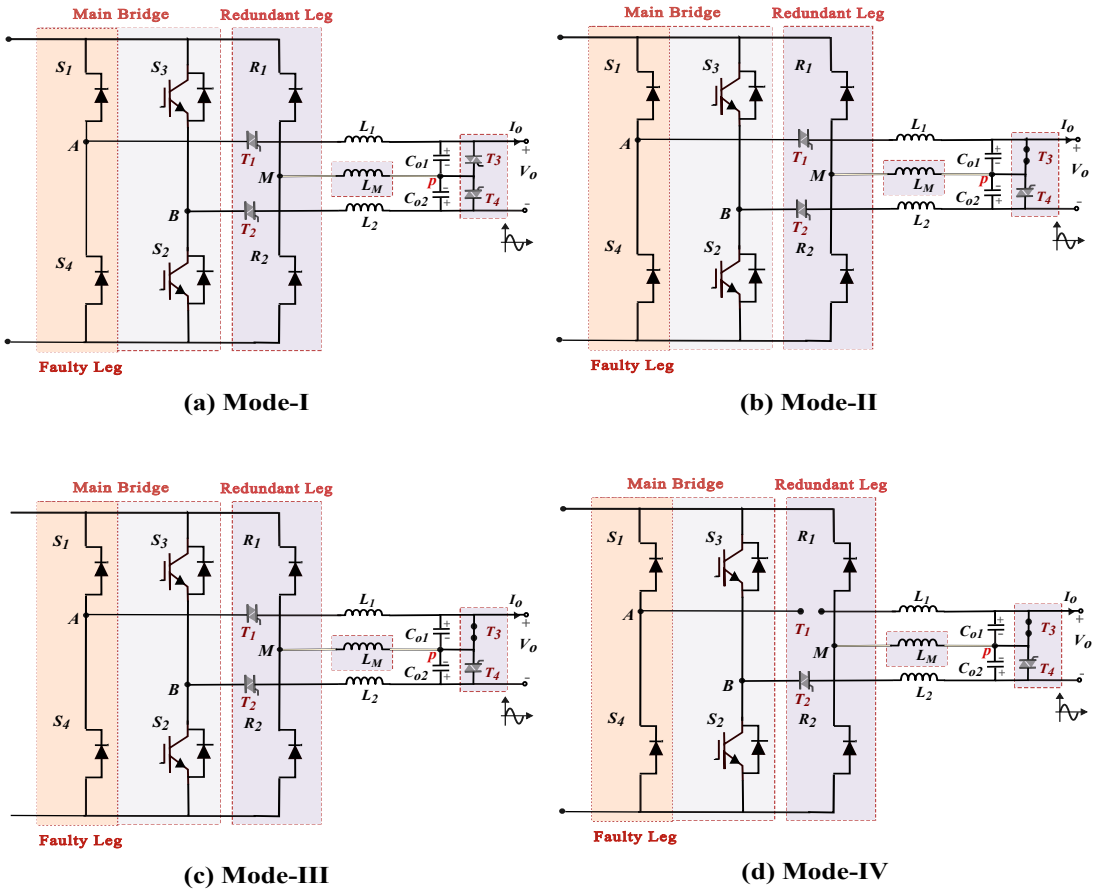



**Figure 5.6:** Circuit configuration during the proposed transition scheme in (a) Mode-I (b) Mode-II (c) Mode-III (the configuration resembles Mode-II, although the two differ in the control modifications), and (d) Mode-IV for OC fault in the $S_1$.

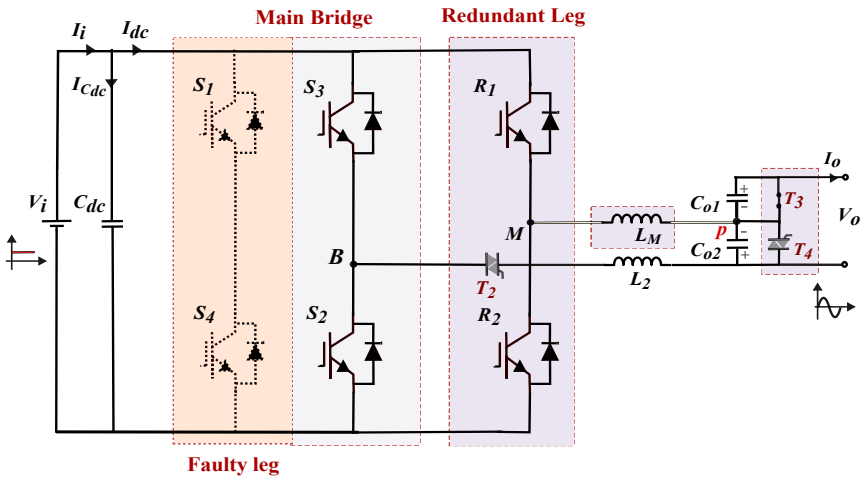



**Figure 5.7:** Circuit configuration during the proposed post-fault correction for a fault in leg 1.

**Table 5.2:** DC-link capacitor values for varying permissible voltage ripple

| % of allowable ripple | Capacitor Value |
|---|---|
| 5% | 212 $\mu$F |
| 4% | 265 $\mu$F |
| 3% | 353 $\mu$F |
| 2% | 530 $\mu$F |

pulses to the redundant leg are given similar to the pulses of the faulty leg given in the pre-fault condition.

The modified filter arrangement in the post-fault correction preserves the inductance value at the main bridge filter's intended value even though the capacitor value is doubled. In terms of usage of semiconductors, there are only four active switches overall as opposed to six. When examining the capacitor's whole lifetime, including its pre-fault and post-fault conditions, the capacitor's lifetime improves as a result.

### 5.2.5 Design of the DC-link Capacitor and Output Side Filter

The design of the DC-link capacitor and the appropriate value of the filter circuit components contribute significantly to the converter's effective functioning. The design of these components is discussed below.

#### 5.2.5.1 DC-link capacitor design

In this study, the DC-link capacitor design is explored in two ways;

1. **Considering the ripple in the DC-link voltage:** The DC-link capacitor design considering the ripple voltage, $\Delta V_r$ is given by,

$$C = \frac{P_o}{2\pi f_o V_i \Delta V_r} \tag{5.20}$$

where, $f_o$ is the mains frequency, $V_i$ is the DC-link voltage, ripple voltage $\Delta V_r = 2rV_{dc}$, and $r$ is the allowed percentage voltage ripple [87]. Table 5.2 shows the calculated values of the DC-link capacitor for various values of the allowed ripple (given in %). The DC-link capacitor values are calculated considering the specifications mentioned in Table 5.4, with the $V_i$ = 150V, $V_o$ = 90 V, and $f_o$ = 50 Hz. Table 5.2 indicates that as the ripple percentage decreases, the capacitance demand increases.

**Table 5.3:** DC-link capacitor values for different hold-up period

| Required Hold-up Time | $V_e$ | Capacitor Value |
|---|---|---|
| 12$ms$ | 120 V | 477 $\mu$F |
| 15$ms$ | 120 V | 597 $\mu$F |
| 20$ms$ | 120 V | 797 $\mu$F |
| 22$ms$ | 120 V | 876 $\mu$F |
| 23.5$ms$ | 120 V | 936 $\mu$F |
| 25$ms$ | 120 V | 995 $\mu$F |
| 20$ms$ | 135 V | 1509 $\mu$F |

2. **Assuming a hold-up duration:** Typically, the inverter functioning in several applications demands for a hold-up duration ranging between 15 and 20 ms. In some cases, the hold-up time requirement is greater than 20 ms.

   The stored energy in the DC-link capacitor, $C_{dc}$ is given by

$$Energy = \frac{C_{dc}(V_i^2 - V_e^2)}{2} \tag{5.21}$$

   As capacitor C discharges into the load, the voltage drops. At a certain point, the voltage becomes sufficiently low for the load to operate, leaving the capacitor with unused energy. The term "$V_e$" is used to describe that low voltage point.

$$C_{dc} = \frac{2P_oT_h}{\eta(V_i^2 - V_e^2)} \tag{5.22}$$

   where $P_o$ is the output power, $T_h$ is the hold-up period, and $\eta$ is the efficiency of the converter. Table 5.3 shows the calculated values of the DC-link capacitor for different hold-up period. The voltage, $V_e$, is assumed to be 120 V (20 % reduction in DC-link voltage) and 135 V (10 % reduction in DC-link voltage). It can be seen that increasing the hold-up period increases the requirement for DC-link capacitance. In addition, as the voltage, $V_e$, rises, the required capacitance value also increases.

   For the designed prototype with specifications mentioned in Table 5.4, the designed value of capacitance is selected considering a hold-up period of 20 ms.

#### 5.2.5.2 Output Side Filter Design

The inductors ($L_1$ and $L_2$) and capacitors ($C_1$ and $C_2$) are used to perform ac filtering. In this case, $L_1$ and $L_2$, as well as $C_1$ and $C_2$, are also equal [81, 83, 88]. Their corresponding sums match the original values of the capacitor and inductor used in a typical H-bridge inverter with the same

**Table 5.4:** Specifications of the Prototype

| Symbol | Parameter | Value |
|---|---|---|
| $V_i$ | Input voltage | 150 V |
| $V_o$ | Output Voltage (RMS) | 90 V |
| $I_o$ | Output Current (RMS) | 1.5 A |
| $f_s$ | Switching frequency | 20 kHz |
| $f_o$ | Fundamental frequency | 50 Hz |
| $L_1, L_2$ | Filter inductors | 100 uH |
| $C_{o1}, C_{o2}$ | Filter capacitors | 30 uF |
| $L_M$ | Redundant leg inductor | 100 uH |

ratings and design criteria. An additional inductor, $L_M$, is used for post-fault correction in order to maintain the same inductance value in the filter to limit the ripple in the inductor current. This inductor is not involved in ac filtering in the pre-fault state.

The selected values of the filter components are: $L_1 = L_2 = L_3 = 100$ uH and $C_{o1} = C_{o2} = 30$uF each. Thus, the total inductor and capacitor participating in filtering is 200 uH and 15 uF. When designing the LC filter for ripple compensation, the following considerations should be made:

1. To obtain ripple compensation, the capacitances $C_{o1}$ and $C_{o2}$ must be high. This means that the capacitance should be chosen so that it can handle the ripple energy.

2. The voltage ripple should also be taken into account while designing the overall filter capacitance. The $C_{o1}$ and $C_{o2}$ hence cannot be very small, such as 1 uF or 2 uF, etc.

3. A very low inductance value will cause increased current ripple. Therefore, the output THD and current ripple should be taken into consideration when designing the inductance.

4. For Leg 1 fault, the filter in the post-fault correction will consist of $L_2$ + $L_M$ (total inductance= 200 uH) as filter inductor and $C_{o2}$ (total capacitance= 30 uF) as the filter capacitor.

5. For Leg 2 fault, the filter consist of $L_1$ + $L_M$ (total inductance= 200 uH) as filter inductor and $C_{o1}$ (total capacitance= 30 uF) as the filter capacitor in the post-fault correction.

NOTE: It should be noted that the identical power circuit (except the use of $L_M$ and the TRIACs) has been used in [81, 83, 88] under different control techniques. Thus, the LC filter architecture stays the same and can be utilised for post-fault correction as well.

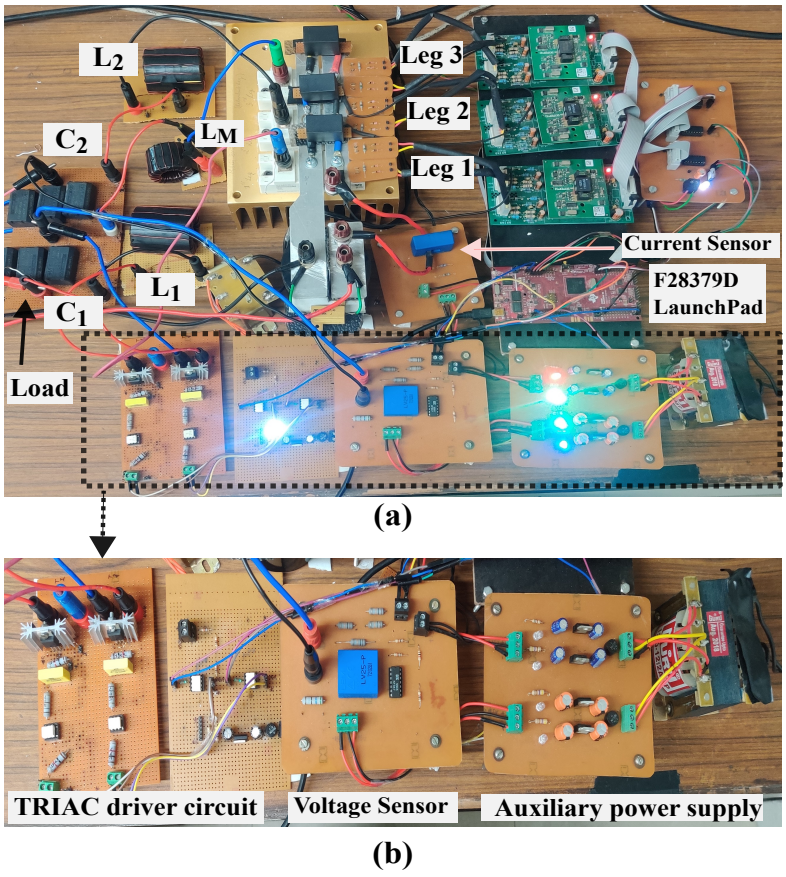



**Figure 5.8:** Laboratory setup of a single-phase fault-tolerant inverter to demonstrate the proposed transition and the correction scheme.

## 5.3 Results and Discussion

A laboratory prototype of the single-phase inverter to demonstrate the proposed transition scheme is shown in Fig. 5.8 with its specifications mentioned in Table 5.4. The proposed scheme is implemented in a digital signal processor (DSP) board F28379D. For the TRIAC circuitry, the selected TRIAC driver IC is the MOC3051 optocoupler. A comparison between pre-fault and post-fault condition is performed. The steady-state results in the pre-fault as well as the post-fault condition are taken at the specified input voltage as shown in Fig. 5.9. To demonstrate the significance and requirement of each mode and *Trns* time, $Tn_1$ to $Tn_4$ (Fig. 5.4), the transition is performed with two distinct transition durations: larger duration (about 1 s) and actual duration (23.5 ms). Fig. 5.10 shows the transition with a longer duration, while Fig. 5.11 depicts the transition with the actual duration.

Fig. 5.9(a) shows experimental results during the healthy condition of the converter without using the ripple reduction technique, i.e., with 0% ripple compensation (SHR). The desired output

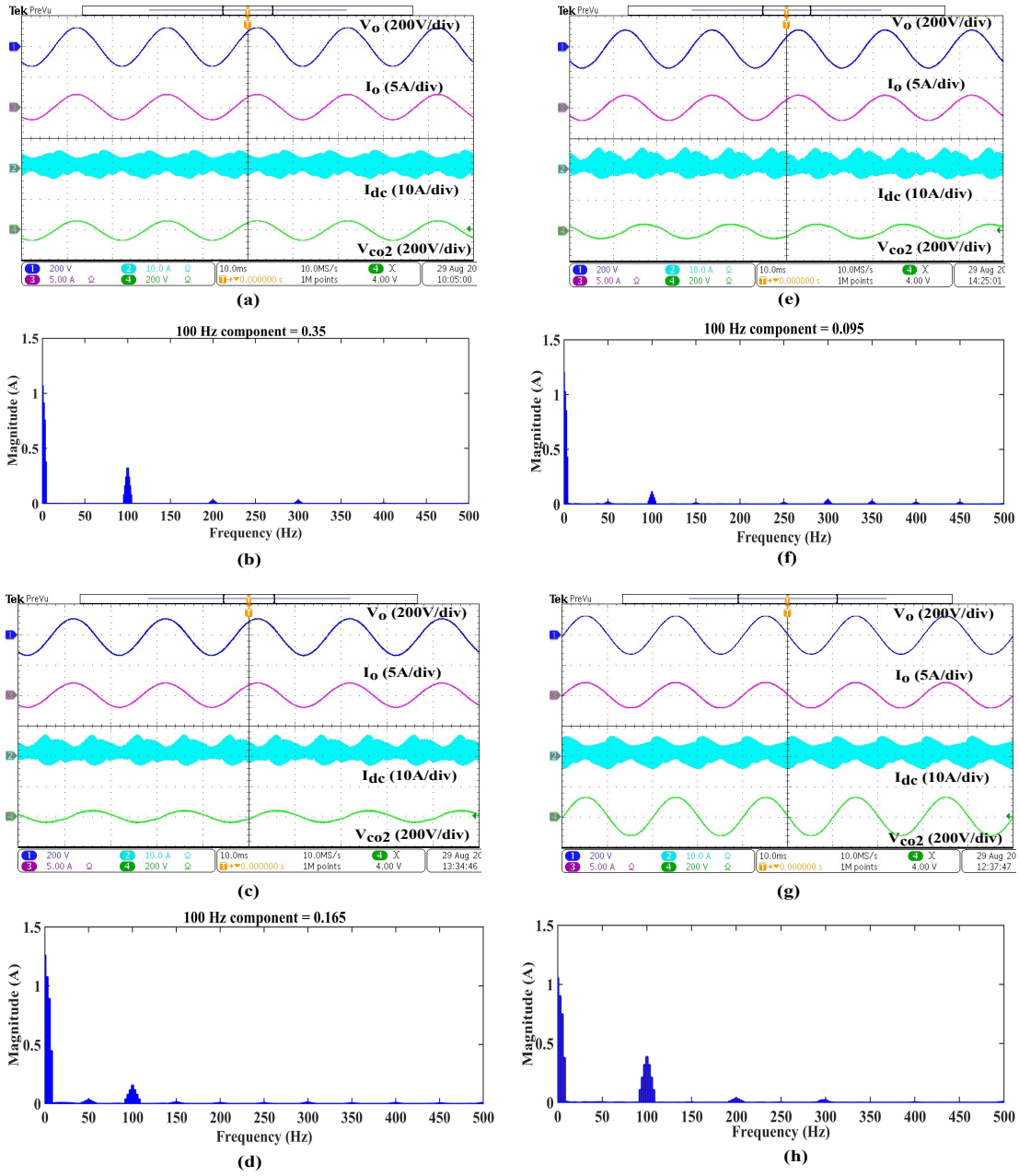



**Figure 5.9:** Experimental results of the pre-fault condition showing (a) $V_o$, $I_o$, $I_{dc}$ and $V_{co2}$ for 0% SHR compensation, (b) FFT of $I_{dc}$ with 0% SHR compensation, (c) $V_o$, $I_o$, $I_{dc}$ and $V_{co2}$ for 50% SHR compensation, (d) FFT of $I_{dc}$ with 50% SHR compensation, (e) $V_o$, $I_o$, $I_{dc}$ and $V_{co2}$ for 75% SHR compensation, (f) FFT of $I_{dc}$ with 75% SHR compensation. (g) $V_o$, $I_o$, $I_{dc}$ and $V_{co2}$ during the proposed post-fault correction, and (h) FFT of $I_{dc}$ during the post-fault correction.

voltage, $V_o$ and current, $I_o$ are obtained. Also, the $I_{dc}$ current shown in Fig. 5.9(a) has a dominating low-order harmonic profile. The corresponding FFT of the current $I_{dc}$ with 0% ripple compensation is shown in Fig. 5.9(b). The presence of the second harmonic component in the $I_{dc}$ is reduced

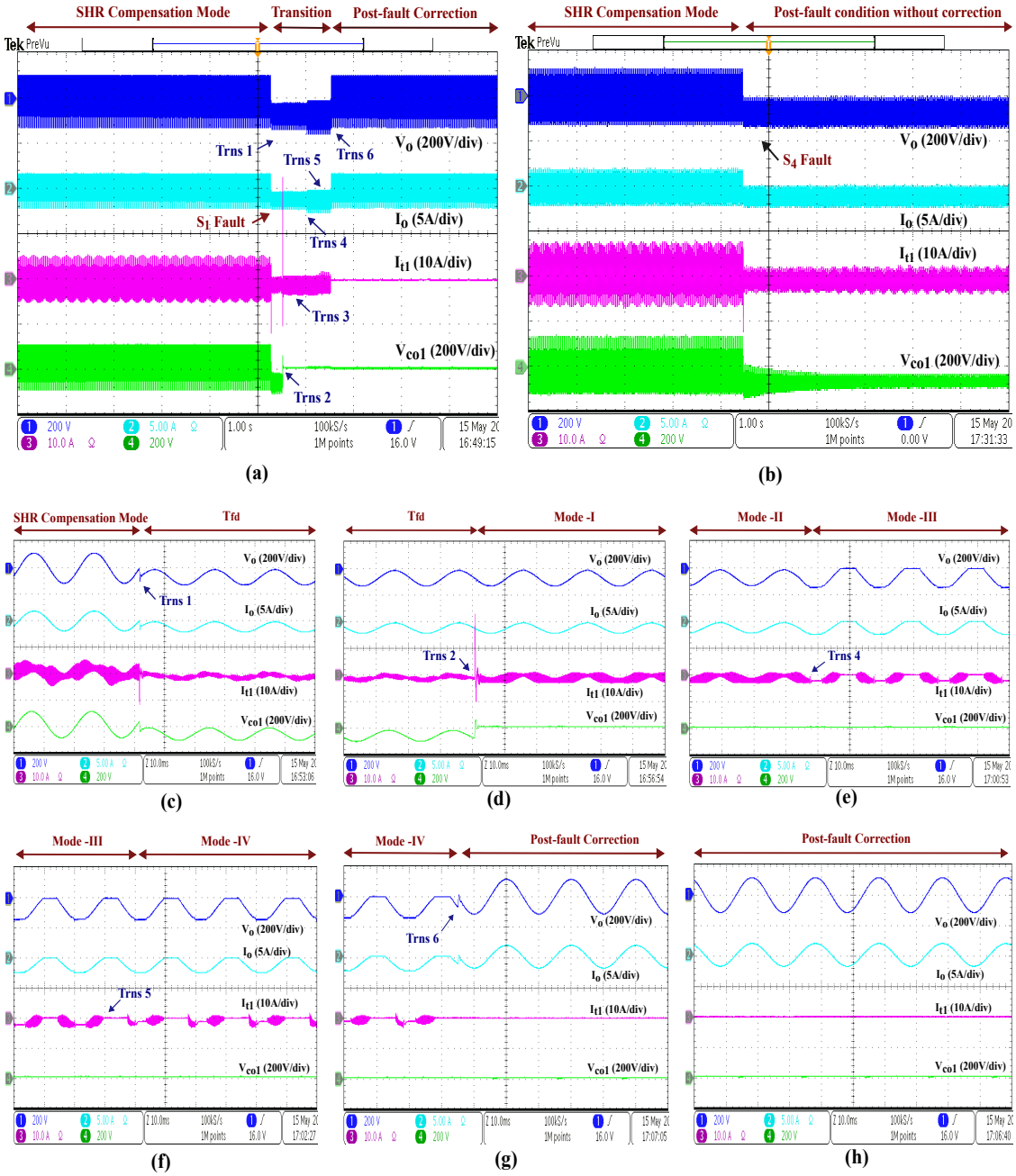



**Figure 5.10:** Experimental results of (a) the proposed transition from the pre-fault to the post-fault correction for $S_1$ open-circuit fault, (b) $S_4$ short-circuit fault (transition showing effects after the protection circuitry) without using the proposed transition and correction scheme, (c) *Trns* 1: transition from healthy to faulty condition, (d) *Trns* 2: transition from faulty condition to mode-I, (e) *Trns* 4: transition from mode-II to mode-III, (f) *Trns* 5: transition from mode-III to mode-IV, (g) *Trns* 6: transition from mode-IV to post-fault correction, and (h) steady-state post-fault correction results for $S_1$ OC fault.

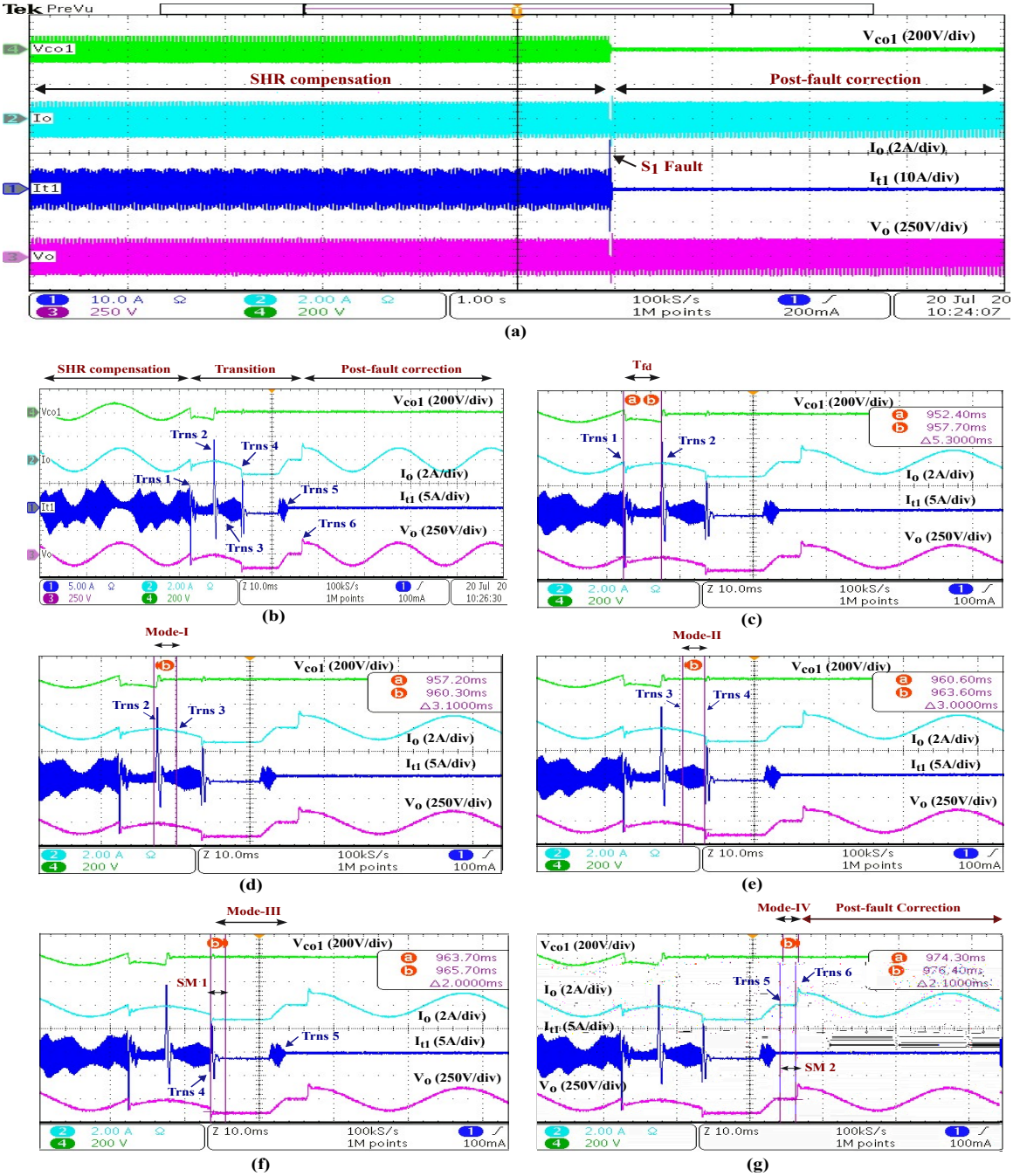



**Figure 5.11:** Experimental results of (a) the proposed transition from the pre-fault to the post-fault correction for $S_1$ OC fault, (b) the complete transition ranging from *Trns 1* to *Trns 6*: completed within 23.5 ms (considering worst case), (c) *Trns* 1 to *Trns* 2: 5 ms for fault detection, (d) *Trns* 2 to *Trns* 3: 3 ms for Mode-I, (e) *Trns* 3 to *Trns* 4: 3 ms for Mode-II, (f) *Trns* 4 to *Trns* 5: consisting of a safety margin (SM 1) of 2 ms and the waiting time for the zero crossing as Mode-III, and (g) *Trns* 5 to *Trns* 6: safety margin (SM 2) of 2.4 ms as Mode-IV.

by switching $R_1$ and $R_2$ as discussed in Section 5.2.1. Experimental results of the pre-fault condition with 50% compensation of the SHR are shown in Fig. 5.9(c). $V_o$ and $I_o$ are similar to those obtained in the 0% ripple compensation case in the pre-fault condition. The FFT for 50% of the SHR compensation is shown in Fig. 5.9(d). To gain more benefit, the SHR compensation can be further increased to 75% of the original value given in Fig. 5.9(b). $V_o$ and $I_o$ shown for this case in Fig. 5.9(e) are identical to the output voltage and current profile shown in Fig. 5.9(a). Also, the FFT obtained in this case is depicted in Fig. 5.9(f). Here, the SHR is compensated by 75% of the original value. This reduces the overall ripple flowing through the DC-link capacitor. Thus, the lifetime of the DC-link capacitor is improved in the pre-fault operation.

The experimental results of the complete transition from the SHR compensation mode to the fault-tolerant method is shown in Fig. 5.10(a) for an OC fault on switch $S_1$. All six of the transitions addressed in Fig. 5.4 are shown in Fig. 5.10(a), (c)-(h). In Fig. 5.10(c), the *Trns* 1 is shown from healthy condition to the faulty condition. The duration $T_{fd}$ is provided for the fault detection. After the fault has been identified and diagnosed, *Trns* 2 is put into action by removing the pulses from the third leg and switch $S_4$. According to Fig. 5.10(d), the mode-I will begin with a zero voltage across the capacitor $C_{o1}$. In mode-II (followed by *Trns* 3), the TRIAC $T_3$ is shorted. As seen in Fig. 5.10(e), after successfully turning on $T_3$, the pulses to the switch $S_3$ are changed to induce a zero current period in $I_{t1}$ via *Trns* 4. The *Trns* 5 (mode-III to mode-IV) is implemented by safely opening the TRIAC $T_1$ as depicted in Fig. 5.10(f). The successful conversion of the converter from faulty condition to the post-fault correction is implemented by *Trns* 6 shown in Fig. 5.10(g) in which the $I_{t1}$ remains zero indicating the complete isolation of the faulty leg. The capacitor $C_{o1}$ is shorted while the capacitor $C_{o2}$ holds the complete load voltage as shown in Figs. 5.9(g) and 5.10(h). Additionally, $V_o$ and $I_o$ return to their pre-fault values. The corresponding FFT of the $I_{dc}$ is also shown in Fig. 5.9(h). Fig. 5.10(b) shows a case of $S_4$ SC fault (effects after $S_4$ is shorted and $S_1$ is opened) without the proposed transition and post-fault correction scheme. Following fault diagnosis, the same transition technique ranging from *Trns* 2 to *Trns* 6 is also applicable for SC failures shown in Fig. 5.10(b).

The actual transition duration is shown in Fig. 5.11(a)–(g). Fig. 5.11(a) depicts a smooth transition from pre-fault to post-fault correction. In the event of an OC fault in switch $S_1$, the transition can be completed in 20 ms or less. The time between *Trns 1* and *Trns* 2 ($T_{fd}$) is kept for fault detection and is considered approximately 5 ms as indicated in Fig. 5.11(c). The time allocated between *Trns* 2 and *Trns* 3 in Fig. 5.11(d) is approximately 3 ms ($Tn_1$), which is the amount of time needed for the capacitor voltage $V_{co1}$ to decrease to zero safely. $Tn_1$ is determined by the amount of energy stored in $V_{co1}$. The time between *Trns* 3 and *Trns* 4 ($Tn_2$) is kept for TRIAC $T_3$ to operate as indicated in Fig. 5.11(e). The duration of the transition is entirely determined by

**Table 5.5:** A Detailed Breakdown of the Transition Period

| Symbol | Parameter | Duration | Details |
|---|---|---|---|
| $T_{fd}$ | Between *Trns* 1, and *Trns 2* | 5 ms | Fault detection. |
| $Tn_1$ | Mode-I | 3 ms | 2 ms for $V_{co1}$ to safely reach zero, and 1 ms as a safety margin. |
| $Tn_2$ | Mode-II | 3 ms | 1.5 ms for TRIAC $T_3$ to operate safely, and 1.5 ms as a safety margin. |
| $Tn_3$ | Mode-III | 10 ms | Safety margin, SM 1 of 2 ms, and the remaining time is the wait for the impending zero crossing after Trns 4. |
| $Tn_4$ | Mode-IV | 2.4 ms | Safety margin, SM 2 of 2.4 ms. |

the point of fault occurrence (in the fundamental cycle) and the distance of the zero crossing after *Trns* 4. In the worst-case scenario (shown in Fig. 5.11) of the fault occurrence in the fundamental cycle, the transition period is represented as 23.5 ms. Two safety margins (SM 1 and SM 2) shown in Fig. 5.11)(f) and (g) with a combined duration of about 4.5 ms are included in the 23.5 ms and can be reduced or eliminated to shorten the transition time further. A detailed breakdown of the transition period is given in Table 5.5.

Experimental results shown in Fig. 5.9 to 5.11 indicates the usefulness of the proposed fault-tolerant scheme with the upgraded capacitor lifetime in a single-phase two-level inverter. The proposed transition strategy is suited to topologies that use an extra leg to compensate for SHR. Let's say, during the working of the topology for SHR compensation in [81], if a fault occurs during its operation, the inverter gets shutdown instantaneously. If the suggested transition scheme is used, the inverter would be able to continue functioning in post-fault operation much like a typical H-bridge inverter without instantly shutting down. Thus, the inverter can accomplish both fault tolerance and SHR compensation using the proposed transition and correction scheme. This effectively utilizes the redundant leg in the pre-fault as well as the post-fault condition by improving the operation of the controller.

## 5.4 Conclusion

The use of a redundant leg is widely adopted in the literature thus, the maximum utilization of the extra leg has been the main focus of this work. This chapter has proposed a transition scheme that switches the converter operation from pre-fault condition (SHR compensation) to post-fault correction (fault-tolerant mode) for open-circuit and short-circuit fault. The pre-fault condition deals with 0-100% compensation of the SHR to extend the lifetime of the capacitor. Whereas

the post-fault correction guarantees the pre-fault condition voltage and current at the output. The proposed method uses TRIACs as connecting devices to exhibit the transition and the correction. The transition scheme is secure and reliable since it switches gradually from faulty condition to post-fault correction. The healthy and faulty conditions (with and without the proposed post-fault correction) have been discussed and experimentally tested on a hardware prototype. The experimental results indicate the usefulness of the proposed transition and the correction scheme on a single-phase inverter.

# Chapter 6

# Critical Overview and Suggestion for Future Work

## 6.1 General

This thesis presents the results of investigations carried on the power electronic converters suitable for SST and two-stage DAB inverter. The most commonly used DC-DC converters are the DAB and SRC. For the majority of applications, every converter must meet certain criteria, including cost, efficiency, and reliability. Operational costs are directly impacted by the converter's reliability and efficiency. In order to encourage the converter's continued operation, the reliability of the converter must be improved. The semiconductors are more prone to failure as compared to any other device. Redundancy in the form of additional switch, leg, module and as a converter is widely adopted in the literature. The cost of the system is increased when redundant legs/modules are used only for the objective of fault tolerance. Therefore, a fault-tolerant approach with a minimal number of additional components is needed. The major contributions of this thesis are as follows:

- Analysis on the converter operation in case of SC and OC faults on power converters used in SST and two-stage DAB inverter.
- Fault-tolerant method for DAB DC-DC converter for the primary side and secondary side faults.
- Self-reliant characteristic and fault-tolerant method for series resonant DC-DC converter for the primary side and secondary side faults.

- Analysis on two switch OC/SC faults occurring simultaneously or one after the other on the SRC and DAB.

- Design and implementation of a fault-tolerant single-phase inverter (giving a complete transition and post fault correction scheme) with extended electrolytic capacitor lifetime.

## 6.2 Summary of Contributions

To encourage prolonged converter operation without shut-down, fault-tolerant techniques are frequently used. The use of redundancy in fault-tolerant methods is a frequent practise. For DC-DC converters like SRC and LLC, regardless of the application or power level, the primary side semiconductor is recognised as the leading cause of converter failure, followed by the resonant capacitor. These two components are responsible for 73% of all converter failures in the industry. A single failure in the semiconductor on the primary side causes catastrophic damage to the converter, causing the device to short-circuit. The resonant capacitor, on the other hand, opens the circuit when there is a failure, preventing power from reaching the secondary side.

For DC-AC power converters, leading manufacturers may presently offer a warranty on PV modules of over 20 years. However, the average lifespan for PV inverters is lesser than this. As a result, inverters may need to be replaced multiple times during the life of a PV system, resulting in additional investment. The detailed discussion on various factors resulting in faults in converters and their remedies are well discussed in **chapter 1**.

A fault-tolerant DAB converter is proposed in **chapter 2**. It involves modifying the whole converter by isolating the faulty switch in order to safeguard the supply and load from short-circuiting. In reaction, a substantial amount of DC component is noticed in the current. Depending on whether the defective switch is on the primary or secondary side, the output voltage drops to half or zero. As a result, post-fault reconfiguration using a fault-tolerant capacitor ($C_f$) with suitable duty and phase shift control achieves the objective of continuous converter operation and the rated output voltage. The major advantage of the proposed method is its application in DAB (which does not have an inbuilt fault-tolerant capability) with reduced number of hardware. With the proposed topology:

- DAB continues to operate without getting shut down on primary and secondary side switch faults (SC or OC).

- Rated voltage is achieved in the post-fault correction for primary or secondary-side faults.

The self-reliant characteristic of the SRC for single and two switch open/short circuit faults is explored in **chapter 3 and 4**. A post-fault correction is proposed which uses a fault-tolerant (FT) capacitor $C_f$ to achieve a continuous operation of the converter. The same capacitor $C_f$ is also utilised for post-fault correction for a selected combination of the two semiconductor defects, offering a common fault-tolerant feature with minimal additional circuitry in the converter. For numerous single/two switch fault combinations in the converter, the goal of continuous converter operation and pre-fault voltage at the output is attained. Control parameters like phase shift ($\phi$), primary and secondary side duty ratio ($D_1$ and $D_2$) are controlled to obtain the pre-fault output voltage in the post-fault correction. For two switch fault cases, the fault-tolerant and self-reliant feature in the converter depends upon the combination of switches undergoing failure. With the proposed analysis and the post-fault correction schemes:

- single switch OC/SC fault, two semiconductor faults (OC/SC) on the alternate side of the converter, and two switch OC faults on the secondary side are corrected.
- only one additional fuse and one FT capacitor is used to achieve continuous operation of the converter, soft-switching, and the desired voltage at the load.

The fault tolerance for the DC-AC converter is given in **chapter 5**. The two primary components that are prone to failure are semiconductor devices and DC-link capacitors. A single-phase two-level inverter needs two extra legs with the connecting devices to achieve a reliable operation in terms of semiconductor fault tolerance and an improvement in the lifetime of the capacitor. However, this increases the inverter's complexity in terms of cost and the number of additional components. Thus, a transition and a post-fault correction scheme is developed to achieve the pre-fault and the post-fault correction objectives. It consists of a single-phase inverter with active power decoupling feature to maximize the lifetime of the electrolytic capacitor during the prefault stage. On occurrence of a fault, the transition scheme securely switches the inverter operation from the pre-fault condition (ripple compensation mode) to the post-fault correction (fault-tolerant mode) in the preparation stage using the same redundant leg. TRIACs are employed as connecting devices to execute the reconfiguration upon the occurrence of a fault in any phase-leg. The transition scheme is secure and reliable since it switches gradually from faulty condition to post-fault correction.

Since semiconductors are more prone to failure as compared to any other component. Thus, the factors needs to be considered while designing the converter to avoid the failures are: thermal design of the converter, turn-on and turn-off resistance of the gate circuit, soft start-up for SRC, SHR compensation for single-phase inverter, etc.

## 6.3 Scope for Future Work

Based on the work provided in the thesis, the following are some suggestions for future work:

1. Continuous functioning is achieved by integrating additional circuitry to achieve fault tolerance. This additional circuitry comprises switches (with gate drivers), connecting devices (such as fuses or TRIACs), sensors, etc. all of which contribute to the control complexity and losses. Thus, a reduction in the additional number of components for fault-tolerant methods, along with a reduction in overall losses and control complexity, can be investigated in the future.

2. The practical simulations considering the device's turn-on and turn-off period, on state resistance, junction temperature, etc. can be considered. The simulations can be executed under a variety of dynamic conditions to complete the accurate investigation of converter and analyze the behaviour of the fault tolerant converter.

3. The DAB and the inverter unit can be connected together to comprehensively test them for different fault conditions. The fault-tolerant methods outlined in the thesis can be examined further for different stages of SST.

4. Methods for implementing both SHR compensation and post-fault correction after the fault can be investigated further in single-phase inverter. It would be interesting to incorporate modifications to the transition and post-fault correction scheme to fulfil both objectives after the fault.

5. The implementation of the fault-tolerant rectifier can be explored further. The same additional circuitry used for fault tolerance can be employed to accomplish multiple objectives.

6. The fault tolerance of the power converters for the two-stage rectifier unit can also be investigated.

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# Appendix A

# Publications

## B.1 Journals

1. P. S. Bhakar and K. Jayaraman, "A New Fault-Tolerant Scheme for Switch Failures in Dual Active Bridge DC-DC Converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7627-7637, Dec. 2022.

2. P. S. Bhakar and J. Kalaiselvi, "Fault-Tolerant and Self-Reliant Characteristic in Series Resonant Converter for Semiconductor Open/Short-Circuit Faults," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 1, pp. 1143-1153, Feb. 2023.

## B.2 Presented conferences

1. P. S. Bhakar and J. Kalaiselvi, "Self-Reliant Feature in DC-DC Converters for Open Circuit Faults," *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Jaipur, India, 2020, pp. 1-6.

2. P. S. Bhakar, S. Jayant and J. Kalaiselvi, "A New Fault-Tolerant Method for Switch Failures in Three-Phase Inverter," *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Jaipur, India, 2022, pp. 1-5.