Modelling, Analysis, and Mitigation of Conducted EMI Noise in Dual Active Bridge Converter

A Thesis Submitted

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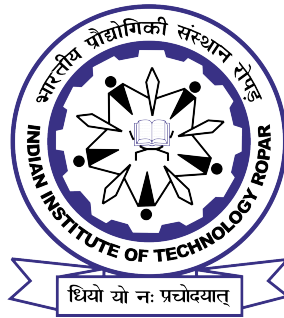
for the Degree of

DOCTOR OF PHILOSOPHY

by

Bellamkonda Dwiza

(2018EEZ0006)

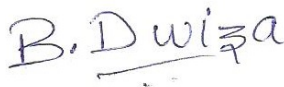**DEPARTMENT OF ELECTRICAL ENGINEERING**

INDIAN INSTITUTE OF TECHNOLOGY ROPAR

December, 2023

I dedicate the thesis to my family.

Declaration of Originality

I hereby declare that the work which is being presented in the thesis entitled **Modelling, Analysis, and Mitigation of Conducted EMI Noise in Dual Active Bridge Converter** has been solely authored by me. It presents the result of my independent investigation/research conducted during the period from July 2018 to December 2023 under the supervision of Dr. J. Kalaiselvi, Assistant Professor, IIT Ropar. To the best of my knowledge, it is an original work, both in terms of research content and narrative, and has not been submitted or accepted elsewhere, in part or in full, for the award of any degree, diploma, fellowship, associateship, or similar title of any university or institution. Further, due credit has been attributed to the relevant state-of-the-art and collaborations with appropriate citations and acknowledgments, in line with established ethical norms and practices. I also declare that any idea/data/fact/source stated in my thesis has not been fabricated/ falsified/ misrepresented. All the principles of academic honesty and integrity have been followed. I fully understand that if the thesis is found to be unoriginal, fabricated, or plagiarized, the Institute reserves the right to withdraw the thesis from its archive and revoke the associated Degree conferred. Additionally, the Institute also reserves the right to appraise all concerned sections of society of the matter for their information and necessary action. If accepted, I hereby consent for my thesis to be available online in the Institute's Open Access repository, inter-library loan, and the title & abstract to be made available to outside organizations.

B. Dwiza

Signature

Name: Bellamkonda Dwiza
Roll No: 2018EEZ0006
Program: PhD
Department: Electrical Engineering
Indian Institute of Technology Ropar
Rupnagar, Punjab 140001

Date: 26/12/2023

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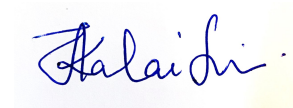
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Certificate

This is to certify that the thesis entitled **Modelling, Analysis, and Mitigation of Conducted EMI Noise in Dual Active Bridge Converter**, submitted by **Bellamkonda Dwiza (2018EEZ0006)** for the award of the degree of **Doctor of Philosophy** of Indian Institute of Technology Ropar, is a record of bonafide research work carried out under my guidance and supervision. To the best of my knowledge and belief, the work presented in this thesis is original and has not been submitted, either in part or full, for the award of any other degree, diploma, fellowship, associateship or similar title of any university or institution.

In my opinion, the thesis has reached the standard fulfilling the requirements of the regulations relating to the Degree.

Signature of the Supervisor
Dr. J. Kalaiselvi
Department of Electrical Engineering
Indian Institute of Technology Ropar
Rupnagar, Punjab 140001
Date: 26/12/2023

Lay Summary

This thesis explores the challenges posed by conducted electromagnetic interference (EMI) in power converters, particularly the dual active bridge (DAB) converter. While advancements in the semiconductor industry have expanded the applications of power converters, the presence of EMI noise remains a critical factor in determining their suitability for use.

The DAB converter, recognized for its bidirectional power transfer, high power density, and galvanic isolation, has become a prominent DC-DC converter. To ensure its seamless operation and prevent disruptions to other converters, this thesis focuses on the analysis and mitigation of conducted EMI noise.

This thesis investigates conducted electromagnetic interference (EMI) noise models of DAB converter. The external-matched impedance approach to estimate conducted EMI noise by examining the transformer's primary-to-secondary winding parasitic capacitance is presented. In addition, the coupled-inductor-based approach to mitigate circulating common-mode (CM) current in the DAB converter, addresses a crucial aspect of interference.

The design of integrated CM chokes for CM and DM EMI filters, aiming to reduce volume occupancy and improve efficiency are developed. Moreover, the integrated chokes for single-stage EMI filters are developed to reduce the EMI filter's overall volume occupancy.

Finally, the thesis concludes with future research directions, making significant strides in addressing EMI challenges in power converters.

Abstract

The conducted electromagnetic interference (EMI) typically refers to the transmission of undesired electromagnetic signals through a conducting medium. The conducted EMI is broadly classified into common mode (CM) and differential mode (DM) noise based on the propagation path. The control schemes opted in a power electronic converter urge the desired switching action for its intended operation. This switching action of the semiconductor devices results in rapid voltage and current fluctuations. These rapid voltage or current fluctuations result in electromagnetic emissions that couple onto nearby conductive paths, thus resulting in conducted EMI.

In isolated DC-DC converters, in addition to the voltage and current transients due to the switching action, the presence of the transformer exacerbates EMI, as it couples noise between primary and secondary sides. Among the isolated DC-DC converters, the dual active bridge (DAB) converter is a cutting-edge power electronics topology renowned for its ability to transfer power with higher efficiency while providing galvanic isolation. The two voltage source converters (VSC) that can accommodate a maximum of eight switches give the DAB converter an impressive power transfer capability compared to other isolated bidirectional DC-DC converters. Moreover, with its advanced control techniques, bidirectional power flow capability, and galvanic isolation, the DAB converter offers engineers a versatile tool for designing next-generation power electronics systems. Thus, it stands as a key player in modern power conversion applications such as renewable energy systems, electric vehicle charging stations, aerospace, and high-voltage DC distribution systems. Despite its impeccable features, the switching action of semiconductor devices, the presence of a transformer, and complex propagation paths for the CM and DM noise, the DAB converter is not exempt from conducted EMI. Hence, understanding the sources and mitigation techniques of the conducted EMI noise in the DAB converter is essential to ensure its reliability and performance in various applications.

Thus, the thesis emphasizes the analysis of conducted EMI noise and its mitigation in the DAB converter. Initially, the work focuses on the detailed analysis of the propagation paths of the CM and DM noise using the CM and DM noise models, respectively. One aspect of the analysis presents an external-matched impedance approach aiming to accurately estimate the conducted EMI noise through the transformer primary-to-secondary winding parasitic capacitance in detail. The other aspect of the analysis focuses on the measurement of the DM noise in the DAB converter that takes a path through the common ground, termed mixed-mode differential mode (MMDM) noise, along with its experimental validation.

In general, the mitigation techniques for common-mode noise typically involve the incorporation of CM filters. Hence, later in the thesis, the circulating CM current that originates due to the DC input CM filters of the DAB converter is thoroughly investigated along with its coupled inductor-based mitigation approach. The detailed comparative analysis of the CM noise performance of the DAB converter with an external inductor and an integrated transformer is presented along with the experimental validation.

Further, the thesis introduces a CM and a DM integrated magnetic structures intended to replace the conventional CM chokes and conventional DM inductors or chokes, to achieve improved physical (size, volume) or electrical characteristics (impedance profile). Finally, to address the size and volume occupancy of the EMI filters, this thesis presents the design of two integrated magnetic choke structures. The experimental performance evaluation of the EMI filters with the presented integrated magnetic choke structures and their corresponding conventional choke structures is conducted on a hardware prototype of the DAB converter.

Thus, the CM and DM noise models of the DAB converter presented in the thesis facilitate a better understanding of the noise propagation paths along with offering insight into the measurement feasibility of the conducted EMI noise through the transformer's primary-to-secondary winding capacitive coupling and the MMDM noise. Additionally, the thesis proves the advantages of employing the integrated magnetics approach, either in the transformer or in the EMI filters, of the DAB converter.

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Abbreviations

EMI   Electromagnetic interference
IEC   International Electrotechnical Commission
CISPR   International Special Committee on Radio Interference
EMC   Electromagnetic compatibility
CM   Common-mode
DM   Differential mode
DAB   Dual active bridge
SPST   Single-phase shift technique
EPST   Enhanced-phase shift technique
DPST   Dual-phase shift technique
TPST   Triple-phase shift technique
LISN   Line impedance stabilization network
MMDM Mixed-mode differential mode
CCMC Circulating common-mode current
CTI   Concentric inductor
CTDMC Concentric toroidal differential mode choke
IC   Integrated choke
PCB   Printed circuit board

Chapter 1

Introduction to Conducted EMI in DAB Converter

1.1 Introduction to EMI

Electromagnetic Interference (EMI) represents an undesirable electromagnetic noise that has the potential to compromise, restrict, or disrupt the optimal functioning of electronic devices or entire systems [1]. Any system handling electromagnetic energy is prone to result in EMI.

The EMI study gained formal recognition quietly in 1933 under a sub-committee of the IEC (International Electrotechnical Commission) in Paris under the name of CISPR (International Special Committee on Radio Interference) [2]. EMI concerns have historically been crucial in military contexts. The swift integration of cutting-edge technologies into power electronic devices has facilitated progress in diverse domains like automotive engineering, microgrid development, and renewable energy systems. Consequently, EMI challenges have become pervasive in power electronic converters across nearly every application. Hence, before deployment in any application, all the power electronic converters, which are designed for the conversion, control, and management of electrical power, undergo testing to ensure their electromagnetic compatibility (EMC). EMC is the ability of a device, unit of equipment, or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to itself or to anything in that environment [3]. The EMC of power equipment is guaranteed through the validation of both the equipment's susceptibility (or immunity) to external influences and its emissions into the surrounding environment.

In practical terms, EMI can manifest in a variety of ways, ranging from subtle performance issues to catastrophic failures. In consumer electronics, for example, EMI may cause audio or video distortion in multimedia devices, disrupt wireless communication signals, or interfere with the operation of sensitive sensors in medical equipment. In industrial settings, EMI can disrupt control systems, leading to production errors, equipment downtime, or safety hazards. In critical infrastructure, such as power grids or telecommunications networks, EMI can compromise the

Table 1.1: EMC standards and its applicability

Sl. No.	Application	Standard	Description
1	Information Technology and Multimedia Equipment	CISPR 32 (EN55032)	Specifies limits and measurement methods for conducted emissions for IT and multimedia equipment
2	Industrial, Scientific, and Medical Equipment (ISM)	CISPR 11	Specifies limits and methods of measurement of radio-frequency emissions from ISM equipment
3	Automotive	CISPR 25	Addresses the measurement of radiated emissions from vehicles, boats, and internal combustion engine-powered devices.
5	Defence	MIL-STD-461	Specifies limits for the control of EMI characteristics of subsystems and equipment.
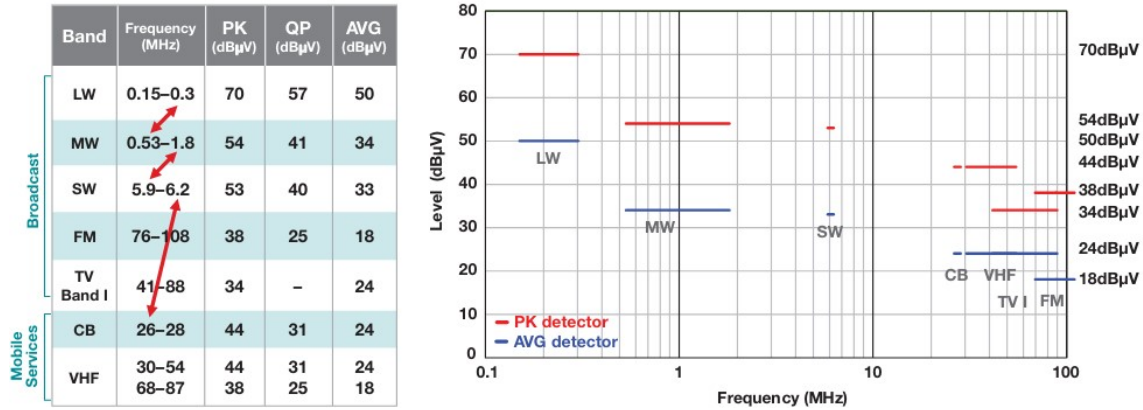
Figure 1.1: CISPR 25 Class 5 conducted emission limits [4].

reliability and resilience of essential services, posing risks to public safety and national security. Hence, to restrict the EMI, the device intended for a specific application undergoes EMC verification. Table 1.1 showcases a selection of standards that the device must adhere to attain EMC compliance. To provide a glimpse of the standard limits, Figure 1.1, given in [4], depicts the CISPR Class 5 conduction emissions limit.

1.1.1   Sources of EMI

Typically, the diverse sources of EMI can be broadly classified into natural and man-made sources, as shown in Figure 1.2 [5]. Solar flares, cosmic rays, storms, and thunder are a few of the natural sources that contribute to EMI in radio, space,
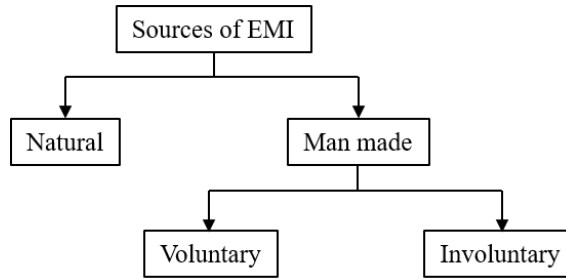
Figure 1.2: Categorization of EMI sources.

aerospace, and telecommunication systems. Due to the unpredictable nature of these natural EMI sources, the systems are designed to nullify the impact of these sources on their performance.

Advancements in technology have led to corresponding progress in electronic circuits, giving rise to EMI, classified as man-made EMI sources. Depending on the intended objectives of electronic advancements, man-made EMI sources are further classified into voluntary and involuntary categories.   Voluntary sources are deliberately designed to produce EMI for specific purposes, such as in wartime scenarios to disrupt enemy activities. In contrast, electronics essential for human civilization, including mobile phones, laptops, medical equipment, power cables, and automobile vehicles, serve as involuntary man-made sources of EMI. The high di/dt loops and high dv/dt nodes in the power stages are usually the involuntary source of noise [1] in the power electronic converters.   Moreover, the ongoing developments in power electronics towards high-power density converters have resulted in components and conductive paths in closer proximity, thereby intensifying the EMI issues. The utilization of integrated circuits, with their densely packed and intricately interconnected components, further exacerbates the EMI, necessitating heightened attention to analyze and mitigate these interference effects for the seamless operation of modern power electronics.

1.1.2   Classification of EMI

EMI manifests itself through the transmission of unwanted signals, either propagating along conductors or radiating into the surrounding air. The former scenario is characterized by electromagnetic energy through the conductive paths and is commonly referred to as conducted EMI noise.   The latter scenario is characterized by electromagnetic energy emanating into the environment, termed radiated EMI noise.

Conducted EMI noise occurs when electromagnetic energy travels along conductive paths, such as wires, cables, or traces on circuit boards. This type of interference is primarily associated with switching events in electronic devices, where rapid changes
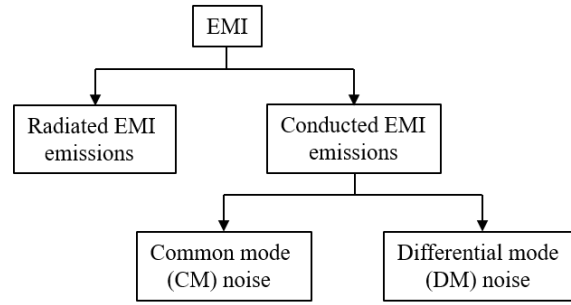
Figure 1.3: Classification of EMI in an electrical circuit.
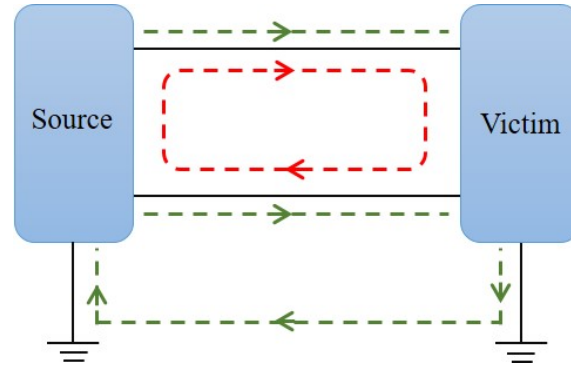
Figure 1.4: CM noise (green) and DM noise (red) propagation paths from an EMI source to the victim.

in voltage and current generate electromagnetic fields that can couple into nearby conductors. Conducted EMI can disrupt the operation of sensitive circuits, leading to malfunctions, data corruption, or even equipment damage.

Radiated EMI noise, on the other hand, occurs when electromagnetic energy emanates into the environment, propagating through free space. Sources of radiated EMI include electronic devices, power lines, and wireless communications systems. This type of interference can affect nearby electronic equipment, particularly if it lacks adequate immunity to external electromagnetic fields.

Thus, the conducted and radiated EMI are the common concerns in electromagnetic compatibility (EMC) testing, where regulatory standards impose limits on the permissible levels of electromagnetic emissions from electronic devices.

As given in Figure 1.3, the conducted emissions are further classified into common-mode (CM) and differential-mode (DM) noise [6] based on their propagation paths. Figure 1.4 illustrates the propagation paths of CM and DM noise emissions from an EMI source to the victim. In Figure 1.4, the source represents a power converter, while the victim denotes any sensitive device connected to the power converter. As depicted in Figure 1.4, the CM noise travels from the source to the victim via the ground, indicated in green; while the DM noise travels through the main power lines, indicated in red. It is to be noted that, the power converter chassis is grounded for safety reasons. Consequently, the high switching

nodes in the power converter activate the converter-to-ground parasitic capacitance, leading to the generation of CM noise. Moreover, inevitable non-idealities in power electronic converters, such as parasitic capacitance and stray inductance in active and passive components like semiconductor switches, inductors, and capacitors, resulting in undesirable high-frequency current and voltage components, consequently generating DM noise.

1.1.3   Conducted EMI in DC-DC converters

Recently, there has been an exponential rise in the dependency on electronic devices in daily life that demands various DC voltage levels to meet the requirements of the specific device. These different voltage levels are obtained by employing the DC-DC converters. In this process, the DC-DC converters have gained popularity in a wide range of applications that deal with lower voltage levels such as portable electronic devices, sensors, and wearables to applications that deal with very high voltage levels such as electric vehicles, microgrids, renewable energy systems, and industrial power distribution networks.

The ideal dc-dc converter exhibits 100 % efficiency; however, in practice, efficiencies of 70 % to 95 % are typically obtained [7]. This is achieved using switched-mode circuits whose elements dissipate negligible power. Based on the topology, DC-DC converters are broadly classified into non-isolated and isolated converters. The non-isolated DC-DC converters include Buck, Boost, Buck-Boost, Zeta, SEPIC, and CUK converters. Due to their simple design, cost, and size, significant research has been performed on non-isolated DC-DC converters [8].

On the other hand, the isolated DC-DC converters ensure a reliable power transfer and provide safety. The flyback, forward, and phase shift converters are among the popular isolated DC-DC converters. The electrical isolation in isolated DC-DC converters can be achieved by a coupled inductor or a transformer [8]. Conventionally, the conducted EMI noise is attenuated by EMI filters. These EMI filters are broadly classified into passive, active, and hybrid EMI filters. Additionally, the suitable modifications in the transformer or the coupled inductor facilitate another feasible approach to reduce the conducted EMI noise in isolated DC-DC converters. The detailed literature study on the conducted EMI noise analysis and mitigation techniques in the isolated DC-DC converter is detailed in Chapter 2. Despite extensive studies on conducted EMI emissions in isolated DC-DC converters like flyback, forward, and phase-shift full bridge converters, the analysis of conducted EMI noise in dual active bridge (DAB) converters is seldom reported. Moreover, the limitations due to operational dissimilarities of the DAB converter with other isolated converter topologies demand a thorough insight into
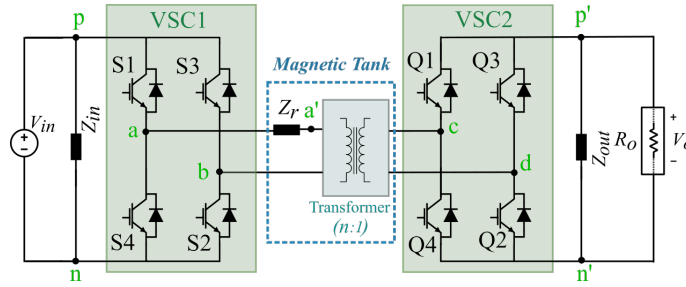
Figure 1.5: Topology of the isolated DAB converter.

the conducted EMI concerns associated with the DAB converter. Further, the DAB converter is discussed along with its operations and potential applications.

1.2 Introduction to DAB Converter

The DAB converter was first proposed in the early 1990s [9]. The DAB converter is highly valued for its inherent features such as bidirectional power transfer capability, high power density, and galvanic isolation [10], [11]. Despite being proposed long ago, it has recently risen to prominence as the leading DC-DC converter, largely attributed to the accessibility of high-voltage and high-current rating semiconductor devices; thus finding the relevance of DAB converter in diverse fields including aerospace [12], [13], [14], electric vehicles [15], [16], micro-grids [17], and shipboard systems [18].

1.2.1 Structure of DAB converter

The DAB converter comprises two voltage source converters (VSCs) interconnected via a magnetic tank, as shown in Figure 1.5. Primarily, VSC1 functions as an inverter by converting DC input to AC, while VSC2 acts as a rectifier by converting AC to DC. The magnetic tank comprises the high-frequency transformer (HFT), which is operated at switching frequencies from a few tens of kHz to a few hundreds of kHz, and an inductor denoted by impedance Z_r, as shown in Figure 1.5. An intriguing aspect of the DAB converter is that, along with the external inductor in the magnetic tank, the leakage inductance of the transformer also contributes to the power transfer.

1.2.2 Phase-shift techniques

Among a variety of control schemes, the phase-shift modulation methods are commonly employed to operate the DAB converter. While control methods may vary for enhanced topologies and their variants, all of these methods can ultimately

be traced back to the following fundamental schemes [19], [20].

Single-phase shift control (SPST)

The SPS is the most widely used control scheme for the DAB converter due to its simplicity and ease of implementation. In this control method, the switches S1 and S2 are governed by the same gate signal, whereas S3 and S4 receive complementary gate signals. This gate signal modulation pattern is similarly applied to the switches of VSC2. However, the switches in the VSC2 experience a phase-shifted gate signal, as a consequence of the employed phase shift modulation scheme. This intentional phase shift in gate signals facilitates power transfer within the DAB converter. The transfer of power becomes feasible due to the phase difference between v_{ab} and v_{cd} node voltages, as shown in Figure 1.6(a). For the square wave v_{ab} and v_{cd} voltage waveforms, the current through the inductor (i_L) is obtained as shown in Figure 1.6(a). For a designed DAB converter, the power flow can be controlled by adjusting the phase shift between the gate signals of the VSC1 and VSC2 switches.

In addition to the ease of implementation, the SPST has acceptable current stress, high efficiency with ZVS particularly at heavy load, and relatively low reactive power when the output-input voltage gain is close to one [9]. However, the considerable mismatch in the v_{ab} and v_{cd} results in higher RMS and peak current between the VSC1 and VSC2. Thus, further techniques are developed to avoid power loss and achieve higher efficiencies in a wide range of voltages.

Enhanced phase-shift Technique (EPST)

Typically, the EPST is the enhanced version of SPST. The EPST provides the feasibility of two phase-shift controllability namely, an inner phase shift and an outer phase shift. The inner phase shift refers to the phase shift between the switches of either the VSC1 or VSC2 and the outer phase shift is the phase shift employed between the VSC1 and VSC2 switches. Thus, the AC voltages of either the VSC1 or VSC2 with the inner phase shift is a quasi-square wave. Figure 1.6(b) shows the v_{ab}, v_{cd}, and i_L waveform for the inner phase shift in the VSC1 switches.

The outer phase shift provides control of power flow direction and magnitude, while the inner phase shift provides the feasibility to reduce the circulating current. Thus, when compared to the SPST, the DAB converter operated with EPST has the advantage of lower circulating current, higher efficiency, and wider ZVS voltage range.

Dual-phase shift Technique (DPST)

Similar to EPST, in DPST there exist both inner and outer phase shifts; however, unlike EPST, in DPST control, the same inner phase shift is employed for both the VSC1 and VSC2 switches. This results in the quasi-square wave v_{ab} and v_{cd}
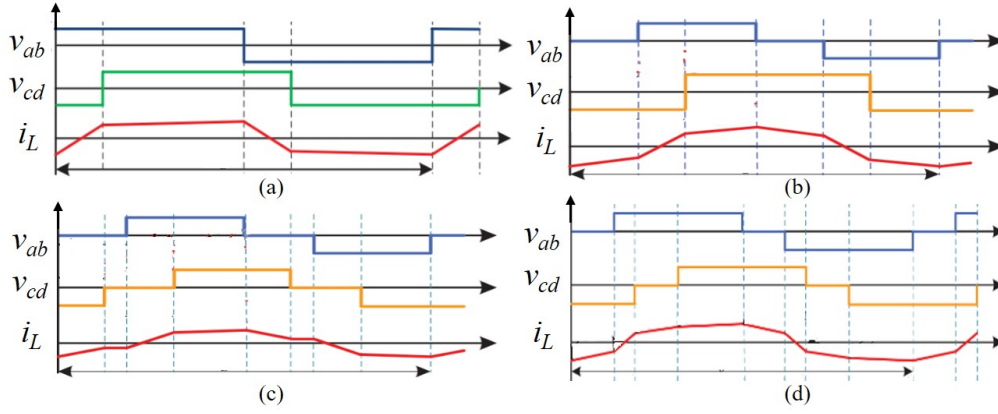
Figure 1.6: v_{ab}, v_{cd}, and i_L waveforms of DAB converter with, (a) SPST, (b) EPST, (c) DPST, and (d) TPST [20].

voltages, as shown in Figure 1.6(c). The corresponding i_L current waveform for the quasi-square v_{ab} and v_{cd} voltages is shown in Figure 1.6(c). When compared to SPST, the DAB converter operated with DPST has lower current stress and steady-state current, improved efficiency, and a wider ZVS operating region. Additionally, the DPST provides the ease of deadband compensation.

Triple-phase shift Technique (TPST)

The TPST control is similar to the DPST, however, the inner phase shift ratios for the VSC1 and VSC2 switches are different. This results in the v_{ab}, v_{cd}, and i_L waveforms as shown in Figure 1.6(d). Thus, the power flow in the DAB converter operated with the TPST has three controllable parameters: two inner phase-shift ratios and an outer phase-shift ratio. Due to the three-degree control freedom with the TPST, it is more difficult to implement TPST compared to SPST, EPST, and DPST. The DAB converter operated with the TPST has minimum current stress, minimum conducting losses, minimum power losses, and maximum ZVS range.

1.2.3   Research Performed on DAB converter

Researchers are actively contributing to various key areas of investigation in the realm of DAB converters. Advanced control strategies and modulation techniques to elevate the overall efficiency of DAB converters, particularly under diverse operating conditions and varying loads were extensively reported [21], [22], [23], [24]. The integration of the hybrid Pulse Width Modulation (PWM) method is under exploration to extend the operational range of DAB converters, ensuring adaptability to wider voltage variations [25], [26], [27]. Moreover, the development of fault-tolerant designs and reliability enhancement techniques is underway to fortify the robust operation of DAB converters [28], [29], [30], [31],

[32]. This is particularly critical in applications where operational downtime is deemed unacceptable [31]. Research is being conducted on the application of DAB converters within smart grid environments [33], [34], [35], [36], [37]. This involves exploring their pivotal role in enhancing grid stability, improving power quality, and facilitating seamless integration with renewable energy sources. The integration of advanced semiconductor technologies, such as wide-bandgap devices like Silicon Carbide (SiC) and Gallium Nitride (GaN), is being explored to enhance the performance and efficiency of DAB converters [38], [39], [40], [41]. Addressing thermal challenges associated with high-power DAB converters involves exploring magnetic integration methods to mitigate DC flux and optimize overall thermal performance [42]. Despite advancements in the above-discussed areas, it is noteworthy that research on conducted EMI issues in DAB systems is relatively under-explored. Addressing this crucial aspect of EMI is paramount to ensure the compatibility and reliability of DAB converters in real-world applications. Hence, the goal of studying conducted EMI in a DAB converter is to understand the common-mode (CM) and differential-mode (DM) noise generation/propagation and to explore the best solutions that reduce the CM and DM noise to achieve the EMC.

1.3   Summary

This chapter provides an in-depth introduction to EMI and its implications in electronic systems, particularly focusing on power electronic converters. The historical context of EMI, its formal recognition by the IEC, and its significance in various domains, including automotive engineering and defense systems, are highlighted. Key sources of EMI, both natural and man-made, are discussed, emphasizing the importance of mitigating EMI to ensure the EMC of electronic equipment. Additionally, relevant EMC standards and their applicability to different applications are presented.

Conducted EMI in DC-DC converters is then discussed, noting the increasing reliance on DC-DC converters in various applications. Further, the chapter elaborates on the structure and operation of the DAB converter along with the most widely employed phase-shift modulation techniques for operating the DAB converter such as SPST, EPST, DPST, and TPST.

Further, the research performed on DAB converters is outlined, focusing on areas such as advanced control strategies, fault-tolerant designs, integration with smart grid environments, and the utilization of wide-bandgap semiconductor technologies. However, it notes the relative lack of research on conducted EMI issues in DAB systems, underscoring the importance of addressing this aspect to ensure their

compatibility and reliability in real-world applications.

Chapter 2

Literature Survey, Motivation, and Objectives

2.1 Literature Survey

In the DAB converter, Figure 2.1 illustrates the CM and DM noise propagation by paths A and B, respectively. The line impedance stabilization network (LISN) at the DC input of the DAB converter, shown in Figure 2.1, stabilizes the line impedances and decouples the conducted EMI of the DAB converter from the external noise of the main supply. It is to be noted that, the transformer and the load are isolated from the ground. Considering the CM and DM noise propagation paths mentioned in Figure 2.1, the CM and DM noise through the power lines of the converter can be measured using a current probe, as shown in Figure 2.2. As discussed in Section 1.1, to achieve EMC of the DAB converter operating in various applications, various national and international organizations and committees provide standard limits such as CISPR 11, CISPR 32, CISPR 25, and so on for the conducted EMI noise [9]. Further, the literature survey on the conducted EMI noise analysis along with the mitigation techniques and the motivations of this thesis are presented.

As indicated in Figure 2.1, the two prominent CM noise propagation paths in the DAB converter are, (i) converter switch node-to-ground parasitics [43], [44], [45],
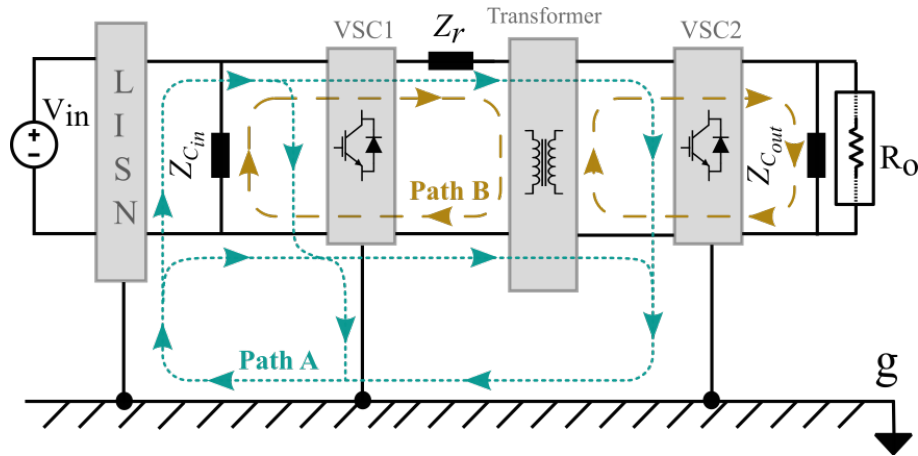
Figure 2.1: CM current (green) and DM current (red) flow is indicated by paths A and B, respectively.
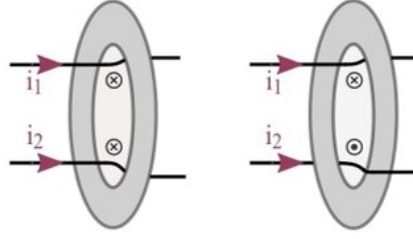
Figure 2.2: Connecting wires arrangement in the current probe to measure the CM and DM currents.

[46], [47] and (ii) transformer intrawinding parasitic capacitance [48], [49], [50], [51],[52],[53]. The high dv/dt on the switch nodes excites the switch node-to-ground parasitics, which are capacitive in nature, thus resulting in CM noise. Hence, reducing the capacitance of the converter-to-ground parasitics significantly reduces the high-frequency currents; thus reducing the CM noise. The printed circuit board (PCB) design of the power converter to reduce this switch node-to-ground parasitic capacitance is reported in [45]. However, the modifications in the converter PCB increase the design complexity and overall cost of the converter. The approach of creating a negative capacitance to reduce the CM noise is discussed in [46] and is validated for various DC-DC converter topologies. However, as the DAB converter consists of more than one converter-to-ground parasitic capacitance, this approach of creating the negative capacitance increases the design complexity of the converter. The concept of complementary current injection to nullify the resultant high-frequency current to the ground is reported in [47], [53]. However, the additional external components for the complementary circuit design increase the design complexity and overall cost of the converter. The compensation circuit that generates the complementary high-frequency current consists of an auxiliary winding and a capacitor. This compensation circuit is validated for the conventional isolated and nonisolated DC-DC converter topologies. Another approach to reducing the converter-to-ground parasitic capacitance with the concept of CM voltage cancellation is reported in [47], [51]. However, the additional compensation circuitry requires one sensing transformer for each half-bridge leg of the converter, thus increasing the cost and size of the converter.

As evident from Figure 2.1, the CM current through the VSC2-to-ground parasitics returns through the transformer of the magnetic tank circuit. Hence, the transformer's primary-to-secondary winding parasitic capacitance plays a significant role in contributing to the CM noise of the DAB converter. Extensive work is reported in regard to the reduction in the CM current through the transformer of the isolated DC-DC converters. Appropriate insertion of the shielding layers between the primary and secondary winding layers significantly reduces the CM noise, as discussed in [48], [49], [50]. In addition, based on the converter topology,

the terminal connections of the transformer reduce the high dv/dt between the transformer windings and thus reduce the CM noise [51], [52]. Moreover, these alterations in transformers with shielding layers or terminal connections demand a thorough understanding of the transformer design and thereby increase the design complexity and cost.

Unlike the extensive work reported for CM noise analysis and mitigation, fewer studies have been performed on DM noise of DC-DC converters. Nevertheless, the presence of two VSCs and a transformer in the DAB converter complicates the DM noise propagation path. For the converter with more than one switch, the impact of the heat sink arrangement on the DM noise is studied in detail in [54]. The study on the DM noise at the dc input side of the isolated dc-dc converters is explored in [55]. Ideally, the source of the DM current is the DM voltages interacting with the power line impedances. However, certain situations result in the DM noise either due to the CM voltage or the CM impedances. This noise transformation phenomenon further subcategories the DM noise into intrinsic and non-intrinsic (i.e., mixed-mode) DM noise. The mixed-mode noise study reported in [56], [57], [58] considers the parasitic capacitor between the switching node on the transformer's primary and the ground. However, the analysis does not consider the transformer's secondary side parasitics. Hence, such detailed analysis of the mixed-mode DM noise in the DAB converter, which consists of multiple converter-to-ground parasitics needs to be thoroughly analyzed.

The above-discussed literature study performed on the CM and DM noise are briefly presented along with their limitations in Table 2.1. Further, the research focusing on the transformer and passive EMI filters is discussed in detail.

The transformer in the DAB converter is subjected to pulsating voltages which energize the parasitic capacitances of the transformer windings and aids the CM and DM noise of the DAB converter. Several methods focused on improving the transformer isolation are explored in the literature [43], [51], [52], [53], [59], [60]. In addition, a detailed analysis of the impact of transformer parasitics on the DM noise of the DAB converter is presented in [61], [62]. With the concept of integrated magnetics, the external discrete inductor is integrated into the transformer, termed integrated transformer, by suitably designing its leakage inductance [63]. Studies revealed that incorporating the integrated magnetics has the benefits of the minimum number of magnetic components, lower losses, and lesser volume, thereby improving the power density of the converter [63], [64], [65]. Although the impact of integrated transformers on the operational performance of the DAB converter is extensively studied, the impact of integrated transformers on the CM noise performance is unexplored.

In general, to effectively mitigate the challenges posed by the CM and DM noise,

Table 2.1: Literature survey on the CM and DM noise along with the limitations

	Impact	Remarks
CM noise		
PCB design modifications	Reduces switch-node-to-ground parasitic capacitance	Requires additional components such as either capacitors or auxiliary winding or sensing transformers, and increases the converter's design complexity and cost
Negative capacitance effect		
Complementary current injection technique		
CM voltage cancellation technique		
Shielding technique	Reduces transformer primary-to-secondary winding capacitance	This demands a thorough understanding of the transformer design and thereby increases its design complexity and cost
Transformer terminal connection modifications	Reduces the high dv/dt transients between the transformer windings	
DM noise		
Heat sink arrangement	Reduces the converter's parasitic capacitance	Limits the improvement of the DM noise profile in the MHz frequency range.
Measurement of MMDM noise in offline switching power supplies	Avoids discrepancies in the CM and DM noise measurement due to the noise transformation phenomenon at the LISN terminals	The analysis cannot be directly extended to the DAB converter due to the presence of more converter-to-ground parasitic capacitance.

either passive [3] or active EMI filtering techniques [66], [67] are employed. Amongst the passive and active EMI filters, the passive EMI filters are widely employed due to their simple design, reliability, and robustness [3]. A typical single-stage EMI filter consists of DM inductors, CM choke, X-capacitor, and Y-capacitor [3]. The X-capacitor is connected between the power lines, while the Y-capacitor is linked between the power lines and the ground. In the context of safety compliance, the selection of Y-capacitors is limited by the maximum allowable leakage current to the ground [3]. Therefore, a CM choke becomes necessary to effectively mitigate the CM noise within the desired standard limit. To meet the attenuation requirement of the DM noise, the DM inductors are generally employed as the high dc-link voltages pose the limitation in choosing the X-capacitor [3], [68]. Due to the presence of CM choke and DM inductors, the passive EMI filters occupy substantial volume, thereby

deteriorating the power density of the converter.

Thus, the integrated magnetics approach is explored to significantly reduce the printed circuit board (PCB) area and volume occupied by the passive EMI filters [69], [70]. The literature reports the design of integrated chokes intended to offer higher DM inductance than the conventional CM choke. Such a design reduces the additional DM inductor's requirement, thereby reducing the area and box volume occupied by the EMI filter [69], [70]. This integrated choke can be designed either by employing a toroidal core [68], [70] or a solenoid [69] into the window area of the conventional toroidal CM choke. However, the integrated choke discussed in [69] introduces the risk of CM choke core saturation, this is because the DM flux through the solenoid flows through the core of CM choke. Moreover, the large core volume requirement for the DM inductor, due to larger DM currents, limits the feasibility of the integrated structure presented in [68], [70]. Integrated choke structures employing EQ cores [71] and stacked arrangements [72] increase the DM inductance of the CM choke at the expense of an increase in the box volume of the CM choke. Additionally, the integrated choke designs with core structural modifications are investigated in [73], [74], [75]. However, these integrated chokes introduce design complexities and higher costs as they are not commercially available. Moreover, the integrated choke structures explored in [76], [77], [78] using ER and I cores increase the risk of magnetic core saturation and reduce the feasibility of using the high permeability nanocrystalline magnetic cores, thus reducing the achievable CM inductance. The single-stage and two-stage integrated EMI choke is presented in [79], to improve the DM performance, is not suitable for the CM choke with a larger window area and has many geometric design constraints. Although the integrated choke structures presented in [77] are suitable for CM choke with a larger window area, the winding structure of the integrated structure does not fully utilize the winding capacity of the ER cores; thereby limiting the maximum achievable DM inductance. Hence, the integrated choke structures for the EMI filters, which address the above-mentioned limitations are to be explored. Besides the above-mentioned two approaches, the possibilities of any other approaches are to be thoroughly investigated.

2.2 Motivation of the Work

From the literature survey it is observed that to ensure the intended operation of the DAB converter, it is crucial to investigate the conducted EMI performance. In general, the detailed analysis of the conducted EMI helps the design engineer in deciding the appropriate EMI filtration technique [63], [80]. Investigating the CM

and DM noise models of the DAB converter eases the propagation path analysis in complex modular systems like solid-state transformers [81]. Moreover, the mixed-mode DM current (MMDM), i.e., the current through the converter-to-ground parasitic capacitance has to be explored to analyze its impact on the DM noise of the DAB converter. In addition, the CM and DM noise through the transformer's parasitics influences the noise performance of the DAB converter. Hence, an appropriate technique to measure the CM and DM noise through the transformer is to be explored.

Additionally, the CM noise reduction techniques discussed in the literature survey incorporate the approach of reducing either the converter-to-ground parasitics or the transformer parasitic capacitance, thereby increasing the design complexity and cost of the converter. Nevertheless employing these techniques reduces the CM noise, but they do not guarantee the elimination of the dc-input side CM filters. As the CM choke in the CM filter is inevitable, the integrated magnetics approach to reduce the CM choke size is to be explored, such that the higher CM inductance is achieved in a lesser box volume. Moreover, the integrated transformer employed to improve the efficiency of the converter is not completely understood in terms of the noise performance of the DAB converter. Hence, the impact of employing the integrated transformer on the CM noise profile, when compared to the presence of its equivalent discrete components, is to be thoroughly explored.

In general, the DC-input CM filters are employed to reduce the DC-side CM noise of the DAB converter. However, incorporating the CM filters there still exists a closed path for the CM current to flow through the transformer parasitic capacitance. Hence, a detailed analysis of the CM noise propagation by employing the DC-input filters is to be performed. The DM inductor or the DM choke occupies a substantial volume in the DM filters. Apart from the conventional winding and core arrangements, the inductor structures that offer higher inductance or occupy a lesser volume are to be explored.

Typically, toroidal core inductors are preferred over other magnetic core structures due to less acoustic noise, low winding losses, and higher inductance [82], [83]. Although the functionalities of the DM inductor differ from the external inductor in the magnetic tank of the DAB converter, the feasibility of extending the integrated magnetic approach of DM inductors to the power inductors should be addressed. Additionally, such a study performed on the power inductors significantly impacts the converter's design and thereby helps improve the converter's power density.

In addition to the integrated magnetics approach to design the CM and DM chokes or inductors, an integrated choke structure that provides both the CM and DM inductance occupying the lower volume is to be investigated. Although various integrated choke structures are explored in literature, the integrated structures that

(a) utilize the commercially available cores, (b) have the flexibility to adjust the air gap thereby eliminating the risk of core saturation, and (c) the winding structure with fully utilizing the core, are to be investigated.

2.3   Objectives of the Work

Based on the above-mentioned motivations, the thesis aims to thoroughly understand the propagation of the conducted EMI noise. Furthermore, it endeavors to offer a viable alternative to traditional magnetic structures in EMI filters, thereby diminishing the spatial footprint occupied by magnetic components within these filters or achieving higher impedances without a change in the spatial footprint. Thus, the objectives of the thesis are summarized as follows.

1. To investigate the conducted EMI noise propagation paths from the CM and DM noise models of the DAB converter.

2. To estimate the CM and DM noise through the transformer's interwinding parasitic capacitance along with the MMDM noise analysis.

3. To analyze the impact of DC-input CM EMI filters on the CM noise propagation in the DAB converter.

4. To explore techniques that facilitate lower CM choke requirement or reduce the volume of CM choke.

5. To devise inductor structures for improved DM inductance.

6. To devise an integrated choke for single-stage passive EMI filters with reduced volume occupancy when compared to the conventional EMI filters.

2.4   Scope of the Thesis and the Organization

The thesis investigates the CM and DM noise in the DAB converter and presents a measurement technique for the conducted EMI noise through the high-frequency transformer of the DAB converter. In addition, the impact of input CM filters on the CM noise propagation path is investigated in detail. The mitigation techniques to reduce the volume occupancy of the discrete CM choke and DM inductor, as well as the integrated choke to reduce the volume occupancy of the EMI filter, are presented. The chapters of the thesis are organized as follows.
In Chapter 3, the detailed CM and DM noise models of the DAB converter are derived by considering the dominant parasitic capacitances. The external-matched

impedance approach is presented to estimate the conducted EMI noise through the transformer's primary-to-secondary winding parasitic capacitance. The generation of the mixed-mode differential mode noise is discussed along with its measurement. In Chapter 4, the coupled-inductor-based approach to mitigate the circulating CM current in the DAB converter, which originates due to the input CM filters is discussed in detail. Additionally, the concentric CM choke intended to reduce the volume occupied by the CM filters is presented in detail. Moreover, the impact of the integrated transformer on the CM noise profile of the DAB converter is discussed in detail.

In Chapter 5, the integrated inductor and DM choke structures to achieve higher DM inductance are presented. The integrated CM choke structures for single-stage passive EMI filters that offer higher DM inductance compared to their equivalent conventional toroidal choke are presented in Chapter 6. The conclusion and future work are summarized in Chapter 7.

2.5   Summary

The chapter provides a comprehensive literature survey, motivation, and objectives for the investigation of conducted EMI noise in DAB converters. It outlines two main paths for CM noise propagation: converter switch node-to-ground parasitics and transformer interwinding parasitic capacitance. The study emphasizes reducing parasitic capacitance to mitigate CM noise, citing various techniques like negative capacitance and complementary current injection.

Furthermore, it highlights the complexity of reducing CM noise and the limited studies on DM noise. The chapter underscores the importance of understanding mixed-mode DM noise and the impact of transformer parasitics. It also discusses passive EMI filtering techniques and the integration of magnetics to reduce filter size and complexity.

Motivated by these challenges, the chapter articulates the thesis objectives, which include investigating EMI noise propagation paths, estimating CM and DM noise through transformer parasitics, analyzing the impact of CM filters, and exploring techniques for reducing CM choke volume. Additionally, it aims to devise integrated choke structures for passive EMI filters.

The scope of the thesis encompasses a detailed investigation of CM and DM noise in DAB converters, along with the mitigation techniques. The chapter concludes by outlining the organization of subsequent chapters, which cover noise model derivation, mitigation techniques, and integrated choke structures.

Chapter 3

Modelling and Analysis of Conducted EMI Noise in DAB Converter

3.1 Introduction

In this chapter, the DAB converter CM and DM equivalent circuits are derived by considering the dominant parasitic components. Following the derived DM equivalent circuit, the analysis and quantification of the MMDM current and the DM current through the transformer are presented. An experimental approach based on an impedance-matched external capacitor, which is employed between the primary and the secondary windings of the DAB transformer, is presented to quantify the DM current through the transformer. The MMDM current and the DM current through the transformer, are validated from the derived DM equivalent circuit.

3.2 Parasitic Consideration for Conducted EMI Noise Analysis

The DAB converter topology is shown in Figure 3.1(a). The voltage source converters VSC1 and VSC2 are mounted on separate heatsinks that stand on the converter case, which is usually grounded for safety concerns, as shown in Figure 3.1(a).

3.2.1 Converter Parasitic Consideration

As shown in Figure 3.1(a), Z_a and Z_b are the leg midpoints (a and b) to ground parasitic impedances of the VSC1; and Z_c and Z_d are the leg midpoints (c and d) to ground parasitic impedance of the VSC2. Further, the positive and negative DC rails-to-ground impedance on the input side are modeled as Z_1 and Z_2, respectively; and Z_3 and Z_4 are the positive and negative DC rails-to-ground impedance on the output side, respectively. The Z_r denotes the impedance of the discrete inductor,
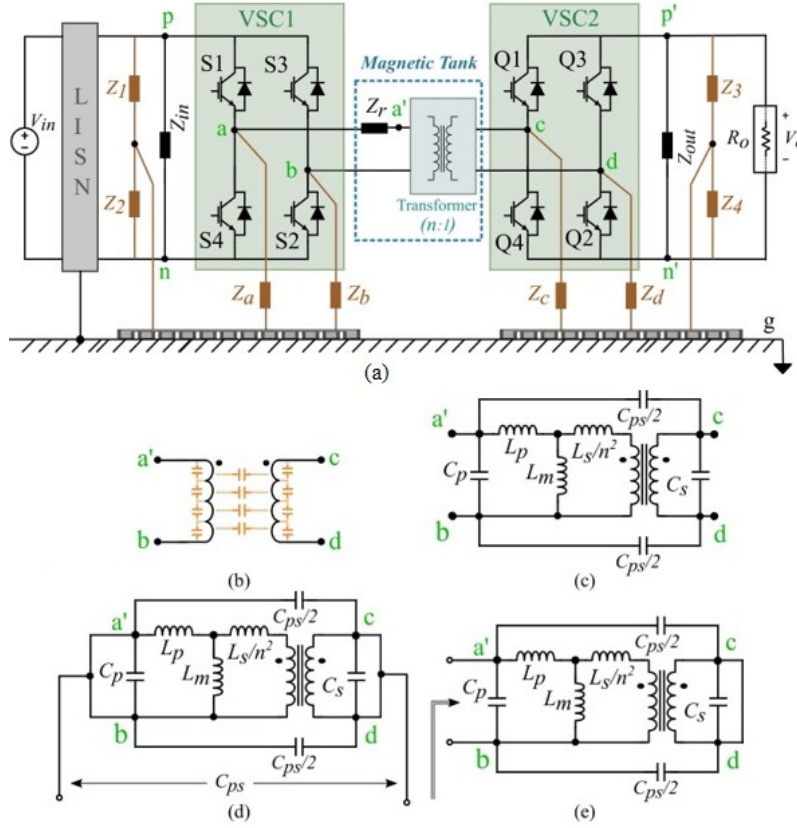
Figure 3.1: (a) DAB converter with dominant parasitics, (b) distributed parasitic capacitance in the transformer, (c) simplified lumped parasitic model of the transformer, (d) measurement of C_{ps}, and (e) measurement of C_p.

L_r. The Z_{in} and Z_{out} are the input and output DC-bus capacitive impedances, respectively.

3.2.2 Modelling of Transformer Parasitics

The transformer parasitics that affect the CM and DM noise are (i) turn-to-turn distributed capacitance of the primary and secondary windings and (ii) distributed capacitance between the primary and secondary windings, as shown in Figure 3.1(b) [51]. The simplified lumped parasitic model of the primary and secondary windings of the transformer is shown in Figure 3.1(c) [9], [62]. In this figure, C_{ps} is the capacitance between the primary and secondary windings of the transformer, whereas C_p and C_s are the turn-to-turn capacitances of the primary and secondary windings, respectively. L_p and L_s are the primary and secondary leakage inductances of the transformer, respectively. While the L_m is the magnetizing inductance.

To estimate C_{ps}, the primary and secondary windings are short-circuited as shown in Figure 3.1(d). Moreover, the parallel combination of L_m and L_s can be approximated to L_s, due to the larger L_m inductance. The capacitance measured across the short-circuited terminals gives the C_{ps} capacitance. To estimate C_p, the transformer
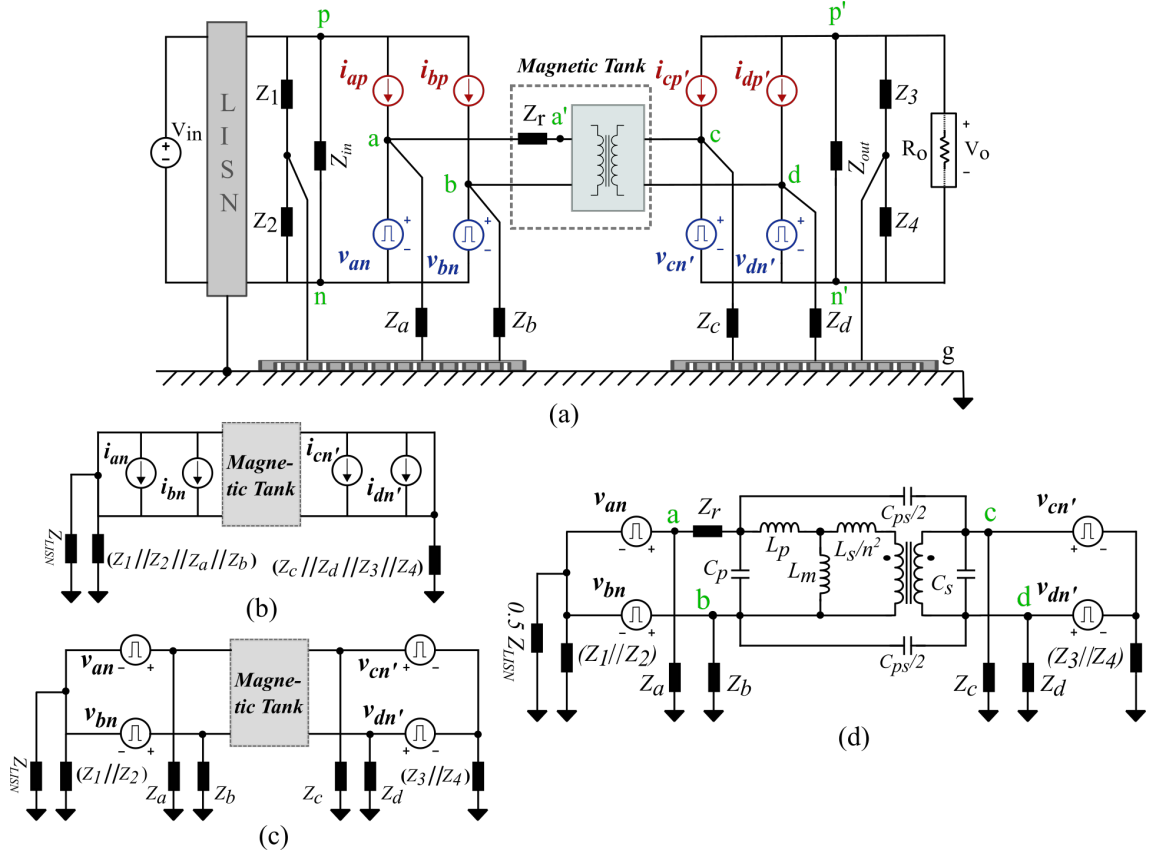
Figure 3.2: (a) Applying the substitution theorem to the switches, (b) CM circuit with current sources, (c) CM circuit with voltage sources, and (d) CM noise model.

secondary winding terminals (c and d) are short-circuited and the impedance is measured across a' and b terminals, as shown in Figure 3.1(e). Thus, the C_p capacitance is expressed as

$$C_p = \frac{1}{4\pi^2 f_{rp}^2 (L_p + L_s/n^2)} - \frac{C_{ps}}{4} \tag{3.1}$$

where f_{rp} is the resonant frequency of the impedance measured across a' and b terminals. Similarly, C_s capacitance is obtained from

$$C_s = \frac{1}{4\pi^2 n^2 f_{rs}^2 (L_p + L_s/n^2)} - \frac{C_{ps}}{4} \tag{3.2}$$

where f_{rs} is the resonant frequency of the impedance measured across c and d terminals, with a' and b terminals short-circuited.

3.3 Extraction of CM and DM Noise Models

Further, the detailed derivation of the CM and DM noise models is presented.

3.3.1 CM Noise Model

The DAB converter shown in Figure 3.1(a) is modified as shown in Figure 3.2(a) by applying the substitution theorem [52]. The LISN branches offer a lower impedance than Z_{C_1} and Z_{C_2}; hence, Z_{C_1} and Z_{C_2} are ignored. The switches S1, S3, Q1, and Q3 are replaced by the current sources i_{bp}, i_{ap}, $i_{dp'}$, and $i_{cp'}$, respectively; and the switches S2, S4, Q2, and Q4 are replaced by the voltage sources v_{an}, v_{bn}, $v_{cn'}$, and $v_{dn'}$, respectively [52].

By applying the superposition theorem, the circuit response is analyzed by considering only the current sources i_{ap}, i_{bp}, $i_{cp'}$, and $i_{dp'}$ of Figure 3.2(a), while replacing all the voltage sources by their internal impedances (short-circuited), as shown in Figure 3.2(b). In the conducted EMI frequency range, Z_{in} and Z_{out} offer very low impedance to the CM noise and hence are considered as short-circuit [51]. As evident from Figure 3.2(b), i_{ap}, i_{bp}, $i_{cp'}$, and $i_{dp'}$ do not result in current through the ground; hence, they will not contribute to the CM noise. The voltage sources v_{an}, v_{bn}, $v_{cn'}$, and $v_{dn'}$ of Figure 3.2(a) are considered acting alone and the current sources are replaced by their internal impedances (open-circuited); the circuit is simplified as shown in Figure 3.2(c). It is evident from Figure 3.2(c) that v_{an}, v_{bn}, $v_{cn'}$, and $v_{dn'}$ contribute to the current through the ground, hence they contribute to the CM noise. Thus, considering all the parasitics listed in Chapter 2.2, the resultant CM noise model of the DAB converter is obtained as shown in Figure 3.2(d).

3.3.2 DM Noise Model

The DAB converter shown in Figure 3.1(a) is modified as shown in Figure 3.3(a) by applying the substitution theorem [52]. The switches S1, S2, Q1, and Q2 are replaced by the voltage sources v_{ap}, v_{bn}, $v_{cp'}$, and $v_{dn'}$, respectively; and the switches S4, S3, Q4, and Q3 are replaced by the current sources i_{an}, i_{bp}, $i_{cn'}$, and $i_{dp'}$, respectively [52].

Similar to the CM equivalent circuit case, the superposition principle is applied to investigate the current and voltage components that contribute to the DM noise. The circuit condition considering the current sources acting alone is presented in Figure 3.3(b), while the simplified circuit considering the voltage sources acting alone is depicted in Figure 3.3(c). As evident from Figures. 3.3(b) and (c), both the current elements (i_{an}, i_{bp}, $i_{cn'}$, and $i_{dp'}$) and the voltage elements (v_{ap}, v_{bn}, $v_{cp'}$, and $v_{dn'}$) contribute to the DM noise in the converter. Thus, considering all the parasitics listed in Chapter 2.2, the resultant DM noise model of the DAB converter is obtained as shown in Figure 3.3(d).

The derived CM noise model in Figure 3.2(d) and the DM noise model in Figure
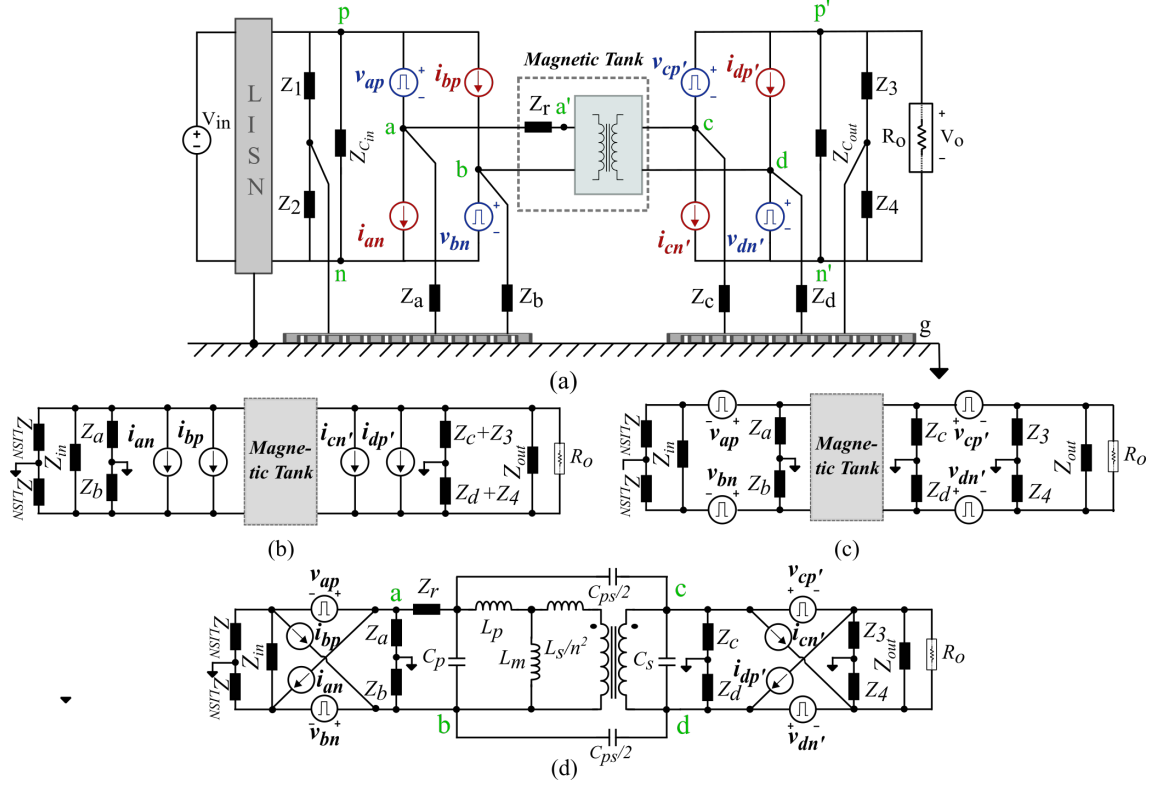
Figure 3.3: (a) Applying the substitution theorem to the switches, (b) DM circuit with current sources, (c) DM circuit with voltage sources, and (d) DM noise model.
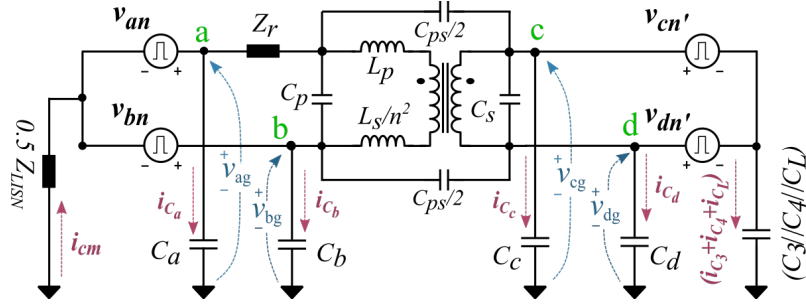
Figure 3.4: CM noise model indicating voltages and currents to ground.

3.3(d) are used for further analysis.

3.4 Analysis of CM Noise Propagation Path

To simplify the CM noise analysis, the parasitic impedance, Z_i, i={1,2,3,4,a,b,c,d} are considered to be capacitive, as shown in Figure 3.4. Moreover, as the LISN branches offer a lower impedance than Z_{C_1} and Z_{C_2}; hence, Z_{C_1} and Z_{C_2} are ignored. The currents through the transformer and the ground parasitics in the CM noise model are shown in Figure 3.4. The modulation scheme implemented to operate the DAB converter depicts the potential at nodes a, b, c, and d (here SPST). In the single-phase-shift modulation, if the dv/dt of v_{ag} is negative, then the dv/dt of v_{bg}

is positive and vice-versa. Likewise, if the dv/dt of v_{cg} is negative, then the dv/dt of v_{dg} is positive and vice-versa. Hence, i_{C_j} $(j = a, b, c, d, 3, 4, L)$ in Figure 3.4 differ in magnitude and direction. Therefore, the algebraic sum of i_{C_j} $(j = a, b, c, d, 3, 4, L)$ gives the total CM current, i_{cm} as

$$i_{cm} = \sum_{j=a}^{d} i_{C_j} + \sum_{j=3,4} i_{C_j} + i_{C_L}. \tag{3.3}$$

The return path for i_{C_j} $(j = c, d, 3, 4, L)$ is through C_{ps} and the LISN. Therefore, i_{cm} in terms of the CM current through C_{ps} (i.e., $i_{a'c} + i_{bd}$) is

$$i_{cm} = i_{C_a} + i_{C_b} + i_{a'c} + i_{bd} = i_{cm\_VSC1} + i_{cm\_TF} \tag{3.4}$$

where i_{cm_VSC1} and i_{cm_TF} are the net CM currents through the VSC1 and the transformer, respectively, and are given as

$$i_{cm\_VSC1} = i_{C_a} + i_{C_b} \text{ and } i_{cm\_TF} = i_{a'c} + i_{bd}. \tag{3.5}$$

In an ideal case, i.e., for perfect isolation in the transformer,

$$i_{cm\_TF} = 0 \implies i_{cm} = i_{cm\_VSC1} \tag{3.6}$$

In practice, the differential voltages $v_{a'c}$ and v_{bd} result in $i_{a'c}$ and i_{bd}, respectively, due to the imperfect isolation in the transformer.

From the above discussions, the following inferences are made for the CM noise propagation in the DAB converter:

1. The impact of VSC2 to the ground currents in i_{cm} is seen due to the imperfect isolation of the transformer.

2. The expression of i_{cm} in (3.4) is valid for the grounded and ungrounded load conditions. However, for the ungrounded load condition, the i_{C_L} in (3.3) would be zero, thus reducing the i_{cm}.

3. The unequal i_{C_a} and i_{C_b} results in the CM current component denoted by i_{cm_VSC1}.

Further, the DM current is discussed in detail and quantified. In addition, the DM current due to unequal i_{C_c} and i_{C_d} is also discussed in detail.
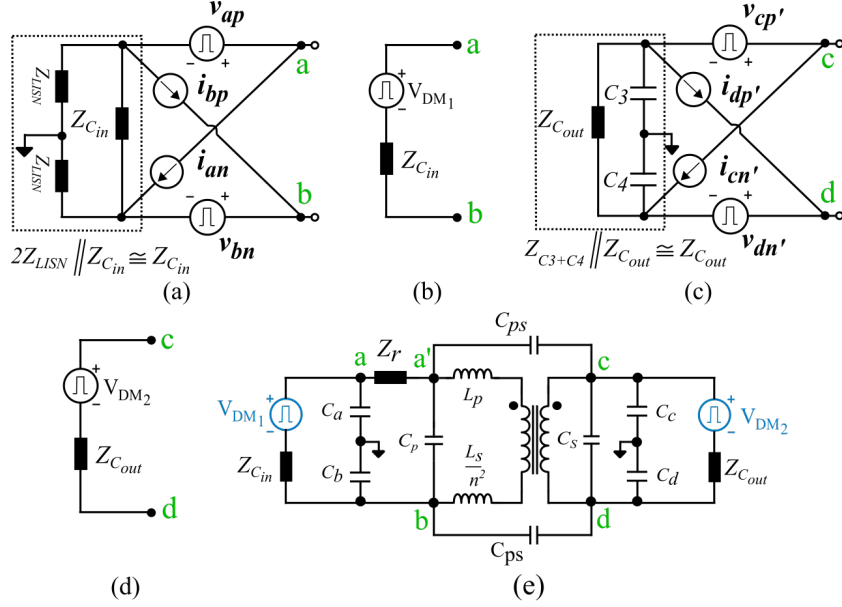
Figure 3.5: (a) Circuit seen through a and b terminals, (b) Thevenin equivalent across a and b terminals, (c) circuit seen through c and d terminals, (d) Thevenin equivalent across c and d terminals, and (e) simplified DM equivalent circuit.

3.5 Analysis of DM Noise Propagation Path

The DM noise model in Figure 3.3(d) is further analyzed for the intrinsic DM (IDM) and mixed-mode DM (MMDM) currents along with the measurement technique.

3.5.1 Reduced DM Noise Model

The DM equivalent circuit across a and b terminals is shown in Figure 3.5(a), and the corresponding Thevenin equivalent circuit is shown in Figure 3.5(b). The Thevenin voltage, V_{DM_1}, is

$$V_{DM_1} = v_{ap} - v_{bn} - Z_{in}(i_{an} + i_{bp}) \tag{3.7}$$

As Z_{in} offers far less impedance compared to $2Z_{LISN}$, the parallel combination of $2Z_{LISN}$ and Z_{in} is approximated to Z_{in}, as shown in Figure 3.5(a). Thus, Z_{in} is the Thevenin impedance across the a and b terminals, as mentioned in Figure 3.5(b).

Similarly, the DM circuit across the c and d terminals is shown in Figure 3.5(c), and its Thevenin equivalent circuit is presented in Figure 3.5(d). The Thevenin voltage, V_{DM_2} is

$$V_{DM_2} = v_{cp'} - v_{dn'} - Z_{out}(i_{cn'} + i_{dp'}) \tag{3.8}$$

With an assumption that only the DC component of the output current flows through R_o, the load parasitic capacitance C_L is ignored. As Z_{out} offers much lower impedance due to the high value of C_{out}, the Thevenin impedance seen through the
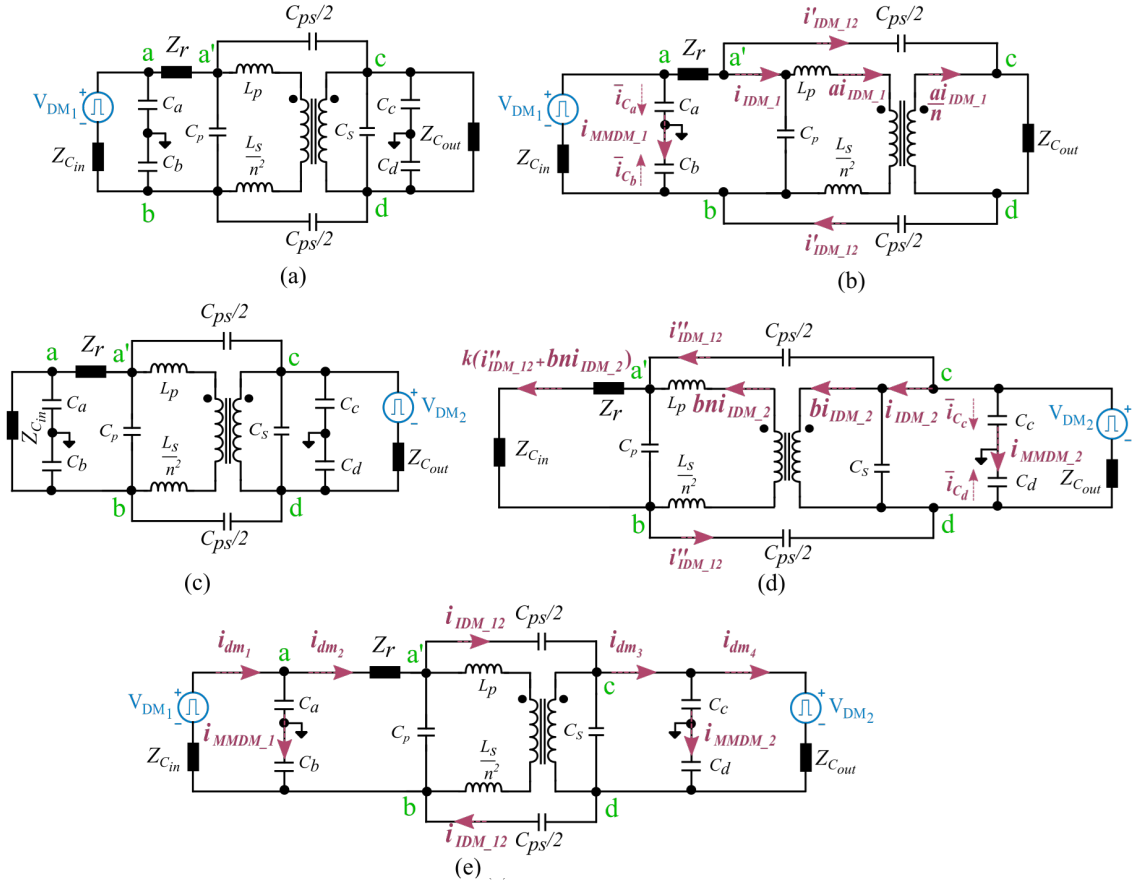
Figure 3.6: (a) V_{DM_1} acting alone (b) currents due to V_{DM_1}, (c) V_{DM_2} acting alone, (d) currents due to V_{DM_2}, and (e) resultant DM currents due to V_{DM_1} and V_{DM_2}.

c and d terminals is approximated as Z_{out}, as shown in Figure 3.5(d).

The Thevenin equivalent circuits, in Figures. 3.5(b) and (d), are incorporated in Figure 3.3(d) to obtain the simplified DM equivalent circuit, as shown in Figure 3.5(e). The individual branch currents due to V_{DM_1} and V_{DM_2} are further analyzed in detail.

3.5.2   Estimation of IDM and MMDM Currents

As evident from Figure 3.5(e), the V_{DM_1} and V_{DM_2} voltages result in the DM currents. Hence, the impact of individual voltage sources on the converter components is analyzed further in detail.

DM currents due to V_{DM_1}:

From the superposition theorem, the simplified DM circuit with V_{DM_1} acting alone (replacing V_{DM_2} with its internal impedance) is considered, as shown in Figure 3.6(a). As observed from Figure 3.6(a), capacitance C_s, the series combination of C_c and C_d, and the impedance Z_{out} are in parallel. In general, Z_{out} offers very low impedance due to high dc-link capacitance, C_{out}. Therefore, the circuit in Figure 3.6(a) is further reduced, as shown in Figure 3.6(b).

As seen from Figure 3.6(b), V_{DM_1} results in the DM current through C_p, C_a, C_b, and Z_{out}. The contribution of the current through the ground parasitics to the CM noise is anticipated; however, the charging/discharging nature of the currents through C_a and C_b results in the DM current as well. This DM current contributed by the unequal current through the ground parasitics is termed as the MMDM current [84], [3], and is expressed as

$$i_{MMDM\_1} = \frac{i_{C_a} - i_{C_b}}{2}, \tag{3.9}$$

where i_{C_a} and i_{C_b} are the currents through C_a and C_b, respectively, as shown in Figure 3.6(b). V_{DM_1} also results in high-frequency noise components in the transformer primary current of the DAB converter. This DM current is termed as the IDM current, as it is the actual DM current that flows due to the line impedance of the converter. Hence, the current through the transformer primary winding due to V_{DM_1} is denoted by i_{IDM_1}, as shown in Figure 3.6(b). As indicated in Figure 3.6(b), ai_{IDM_1} is the fraction of i_{IDM_1} that is transferred magnetically to the secondary winding. Another DM current component due to V_{DM_1}, denoted by i'_{IDM_12}, flows through Z_{out} and C_{ps}. It is to be noted that the sum of i_{IDM_1}, i_{MMDM_1}, and i'_{IDM_12} flows through Z_{in}, as shown in Figure 3.6(b).

DM currents due to V_{DM_2}:

The circuit condition of Figure 3.5(d) with V_{DM_2} acting alone (replacing V_{DM_1} with its internal impedance) is shown in Figure 3.6(c). Since Z_{out} is lower compared to the impedance offered by the series combination of C_a and C_b, the circuit in Figure 3.6(c) is simplified as shown in Figure 3.6(d). Similar to V_{DM_1}, V_{DM_2} results in i_{IDM_2}, i_{MMDM_2}, and i''_{IDM_12} as indicated in Figure 3.6(d). The expression for i_{MMDM_2} is written as

$$i_{MMDM\_2} = \frac{i_{C_c} - i_{C_d}}{2}, \tag{3.10}$$

where i_{C_c} and i_{C_d} are the currents through C_c and C_d, respectively, as shown in Figure 3.6(d). The IDM current due to V_{DM_2} (i.e., i_{IDM_2}) that flows through the secondary winding is the high-frequency component of the transformer secondary current. As indicated in Figure 3.6(d), bi_{IDM_2} is the fraction i_{IDM_2} that is transferred magnetically to the primary winding. Further, the i''_{IDM_12} current through C_{ps} is divided between Z_{in} and C_p, as indicated in Figure 3.6(d); where, k is the fraction of i''_{IDM_12} and bni_{IDM_12} that flows through Z_{in}. The currents i_{IDM_2}, i_{MMDM_2}, and i''_{IDM_12} flow through Z_{out} as shown in Figure 3.6(d).

As depicted in Figures. 3.6(b) and (d), the DM current through C_s, C_c, and C_d
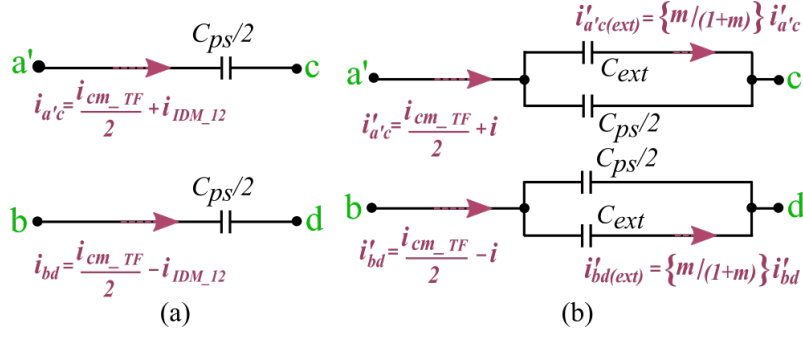
Figure 3.7: CM and DM currents through the transformer, (a) without C_{ext} and (b) with C_{ext}.

due to V_{DM_1} and the DM current through C_a, C_b due to V_{DM_2} are zero. The DM currents in various branches of Figure 3.5(d) are summarized in Figure 3.6(e); where the currents i_{IDM_12}, i_{dm_1}, i_{dm_2}, i_{dm_3}, and i_{dm_4} are obtained as,

$$i_{IDM\_12} = i'_{IDM\_12} - i''_{IDM\_12}, \tag{3.11}$$

$$i_{dm_1} = i_{IDM\_1} + i_{MMDM\_1} + i'_{IDM\_12} - ki''_{IDM\_12} \\ - kbni_{IDM\_2}, \tag{3.12}$$

$$i_{dm_2} = i_{IDM\_1} + i'_{IDM\_12} - ki''_{IDM\_12} - kbni_{IDM\_2}, \tag{3.13}$$

$$i_{dm_3} = i_{IDM\_12} - i_{IDM\_2} + \frac{a}{n}i_{IDM\_1}, \ and \tag{3.14}$$

$$i_{dm_4} = i_{IDM\_12} - i_{IDM\_2} - i_{MMDM\_2} + \frac{a}{n}i_{IDM\_1}. \tag{3.15}$$

From the above discussions, the following inferences are made for the DM noise.

1. Since i_{MMDM_1} and i_{MMDM_2} are the DM current components of ground parasitic capacitors, C_i ($i = a, b, c, d$), the noise due to these currents is termed as the MMDM noise.

2. The currents i_{IDM_1}, i_{IDM_2}, and i_{IDM_12} flow in the main power flow path, hence the noise due to these currents is termed as the IDM noise.

3. The DM current components due to V_{DM_1} and V_{DM_2} flow through Z_{in} and Z_{out}, respectively.

4. The i_{C_i} ($i = a, b, c, d$) currents cannot be directly measured using a current probe, as C_i ($i = a, b, c, d$) are the distributed parasitic components. Hence, an alternative indirect measurement method is necessary to measure the i_{MMDM_1} and i_{MMDM_2} currents.

3.5.3   Measurement of IDM and MMDM Currents

In this section, the measurement of the IDM current (i_{IDM_12}) and the MMDM currents (i_{MMDM_1} and i_{MMDM_2}) is discussed.

Measurement of IDM current through C_{ps} (i_{IDM_12})

The current through C_{ps} cannot be directly measured using a current probe as it is distributed between the primary and secondary windings of the transformer. Therefore, two additional capacitors denoted by C_{ext} are connected externally to match the impedance across the $a'c$ and bd terminals. The C_{ext} in terms of C_{ps} is

$$C_{ext} = m\Big(\frac{C_{ps}}{2}\Big) \tag{3.16}$$

where m is a positive integer. The currents $i_{a'c}$ and i_{bd} go through C_{ps} due to $v_{a'c}$ and v_{bd}, respectively, as shown in Figure 3.7(a). The $i_{a'c}$ and i_{bd} consist of the CM current component, i_{cm_TF} (given by (3.5)), and the DM current component, i_{IDM_12}. The i_{IDM_12} is given as

$$i_{IDM\_12} = \frac{v_{a'b} - v_{cd}}{2Z_{C_{ps}}}, \text{ where } Z_{C_{ps}} = \frac{2}{\omega C_{ps}}. \tag{3.17}$$

The modified $i_{a'c}$ and i_{bd} with C_{ext} are denoted by $i'_{a'c}$ and i'_{bd}, respectively, as shown in Figure 3.7(b). For the values of m that result in insignificant changes in $v_{a'c}$, v_{bd}, and i_{cm_TF} for with and without C_{ext}, the DM current through the transformer with C_{ext} is,

$$i = (1 + m)\frac{v_{a'b} - v_{cd}}{2Z_{C_{ps}}} = (1 + m)i_{IDM\_12}. \tag{3.18}$$

The currents $i'_{a'c}$ and i'_{bd} are divided between C_{ext} and C_{ps} in proportion to their capacitances, as indicated in Figure 3.7(b). Therefore, the currents through C_{ext} (i.e., $i'_{a'c(ext)}$ and $i'_{bd(ext)}$) in terms of $i'_{a'c}$ and i'_{bd} are as indicated in Figure 3.7(b). Thus, the measured i_{IDM_12} and i_{cm_TF} from the currents through C_{ext} are given by

$$i_{IDM\_12} = \frac{i'_{a'c(ext)} - i'_{bd(ext)}}{2m} \text{ and} \tag{3.19}$$

$$i_{cm\_TF} = \frac{1+m}{m}(i'_{a'c(ext)} + i'_{bd(ext)}). \tag{3.20}$$

Measurement of i_{MMDM_1} and i_{MMDM_2} currents:

The i_{dm_1}, i_{dm_2}, i_{dm_3}, and i_{dm_4} currents obtained in Figure 3.6(e) are measured at various places in the DAB converter, as shown in Figure 3.8. Thus, from
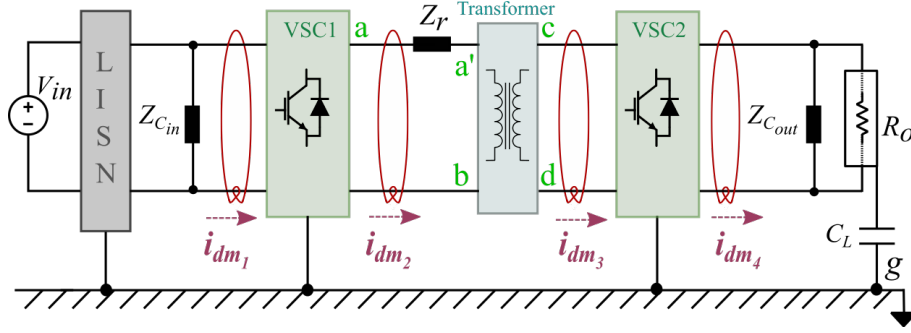
Figure 3.8: Measurement of i_{dm_1}, i_{dm_2}, i_{dm_3}, and i_{dm_4} currents.

(3.12)-(3.15), the i_{MMDM_1} and i_{MMDM_2} can be measured as

$$i_{MMDM\_1} = i_{dm_1} - i_{dm_2} \ and \ i_{MMDM\_2} = i_{dm_3} - i_{dm_4}. \tag{3.21}$$

The following inferences are made from the measurement of IDM and MMDM noise discussed above.

1. The externally connected capacitor, C_{ext} alters the IDM current by $(1+m)$ times. Thus, the actual IDM current (i.e., i_{IDM_12}) is measured from (3.19).

2. For the DAB converter mounted on a single PCB, the PCB design should be flexible to incorporate the external circuit required to measure the i_{IDM_12} current.

3. As evident from Figure 3.6(e), reducing the parasitic capacitance C_i ($i = a, b, c, d$), by altering either the power semiconductor switch to heat sink configuration or the heat sink to ground connections as discussed in [85], affects the i_{MMDM_1} and i_{MMDM_2} currents.

3.6 Results and Discussions

3.6.1 System Description

The DAB converter prototype incorporating Si-IGBT modules is shown in Figure 3.9, and is investigated for validating the above-discussed CM and DM noise analysis. The parameters of the experimental setup are provided in Table 3.1. The LISN (LI-3P-232) is connected to the dc input of the DAB converter prototype. All the experimental results are presented for the ungrounded load condition, as the grounding condition of the load does not alter either the analysis or the measurement methods. The frequency spectra are presented from 150 kHz to 30 MHz, which is the conducted EMI frequency range.
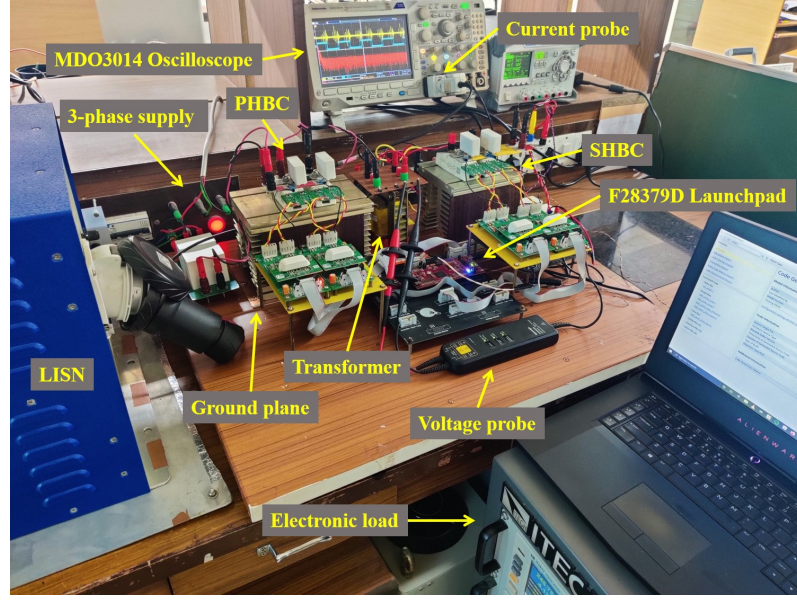
Figure 3.9: Experimental setup of DAB converter.

Table 3.1: System Operating Parameters Along with Parasitic Values

Parameter	Value
Input voltage, V_{in}	250 V
Output voltage, V_o	250 V
Output power, P_o	1 kW
Switching frequency, f_{sw}	10 kHz
Transformer turns ratio, n	1
External inductance, L_r	0.288 mH
Impedance-matched external capacitor, C_{ext}	70 pF
Winding capacitance of primary and secondary, C_p and C_s	140 pF
Parasitic capacitance of VSC1 and VSC2, C_a, C_b, C_c, and C_d	220 pF
Input and output dc rails to ground capacitance, C_1, C_2, C_3, and C_4	120 pF

The parasitic capacitances are measured using a PSM3750 impedance analyzer (that can measure the capacitance ranging from 1 pF to 1000 uF) at the switching frequency and are listed in Table 3.1. The transformer parasitics, i.e., C_p, C_s, C_{ps}, are measured using the procedure mentioned in Figures 3.1(d) and (e). The currents and voltages are measured using a high-bandwidth current probe (TCP202A) and a high-bandwidth voltage probe (THDP0200), respectively. The experimental frequency spectra data is obtained from Tektronix oscilloscope (MDO3014) which has a bandwidth of 100 MHz.

The conducted EMI noise models are simulated using MATLAB-Simulink with the system parameters listed in Table 3.1 to estimate the DM noise. The dv/dt imposed
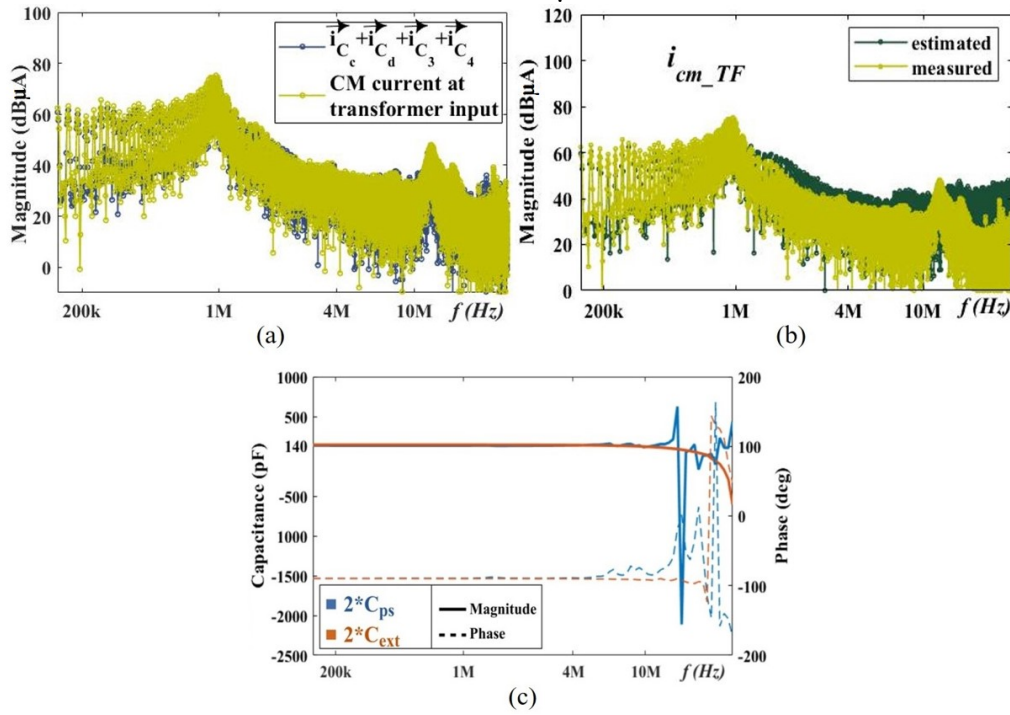
Figure 3.10: (a) Frequency spectra of total VSC2 to ground current and CM current at the primary side of the transformer, (b) measured and estimated frequency spectra of i_{cm_TF}, and (c) matching capacitance of C_{ps} and externally connected C_{ext}.
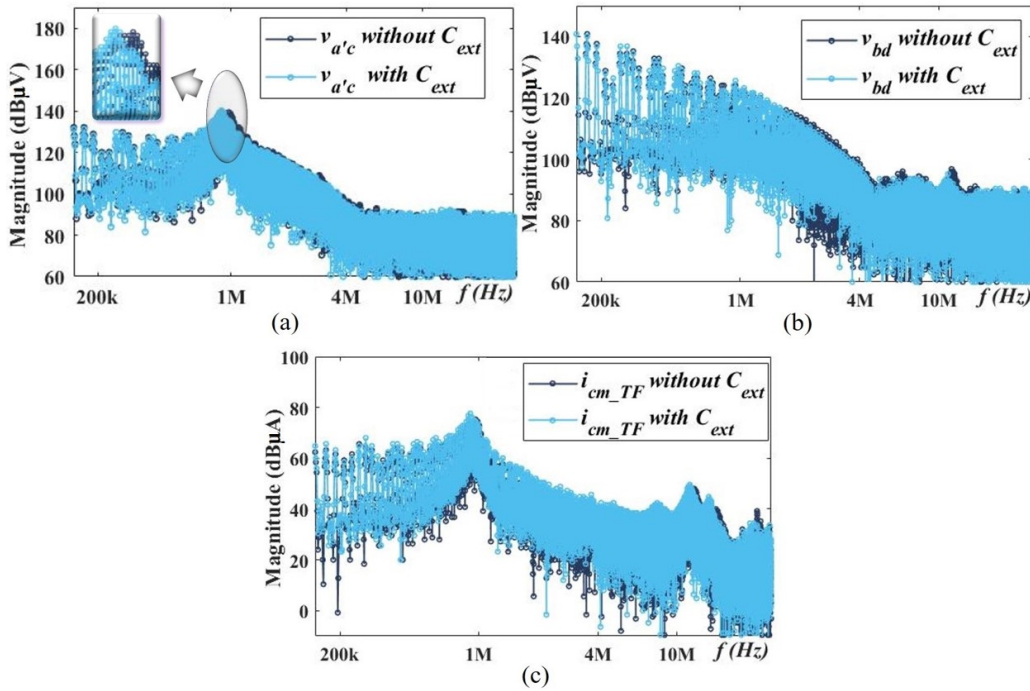
Figure 3.11: Frequency spectra for without and with C_{ext}, of (a) $v_{a'c}$, (b) v_{bd}, and (c) i_{cm_TF}.

due to the switching action of active devices that excites the converter parasitics is carefully matched in the numerical simulation with the exact hardware conditions to obtain an accurate estimate of i_{IDM_12}, i_{MMDM_1}, and i_{MMDM_2}. The results are discussed in the subsequent sections.
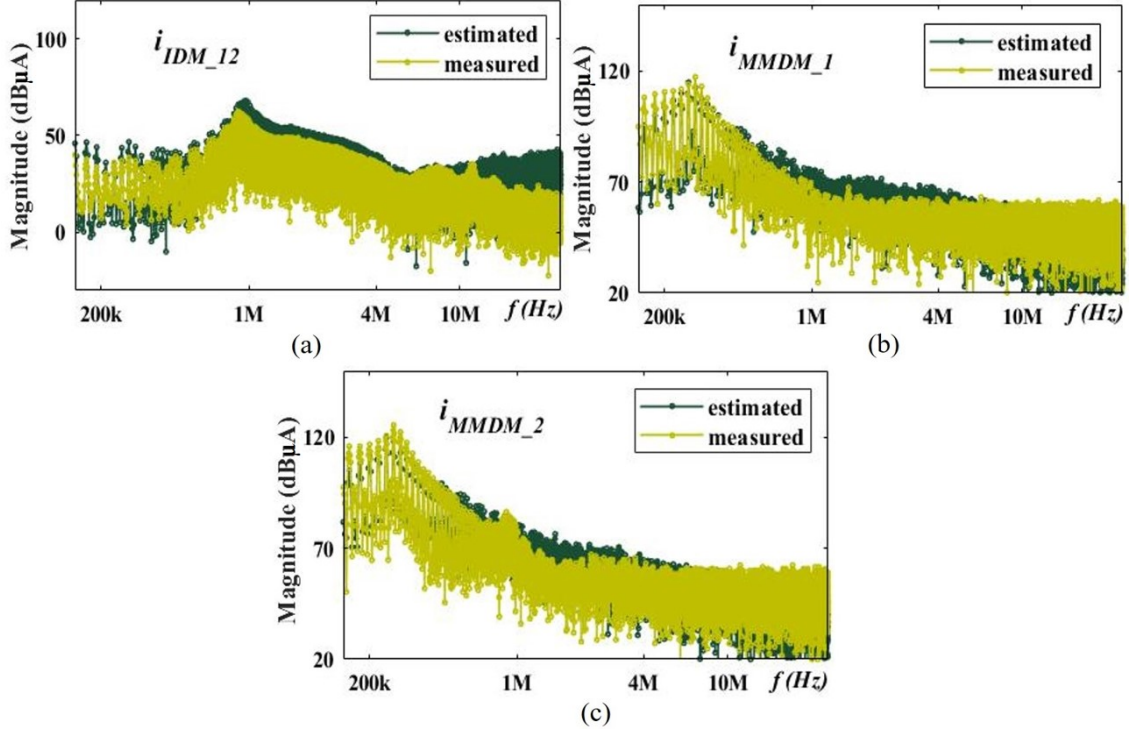
Figure 3.12: Measured and estimated frequency spectra of (a) i_{IDM_12}, (b) i_{MMDM_1}, and (c) i_{MMDM_2}.
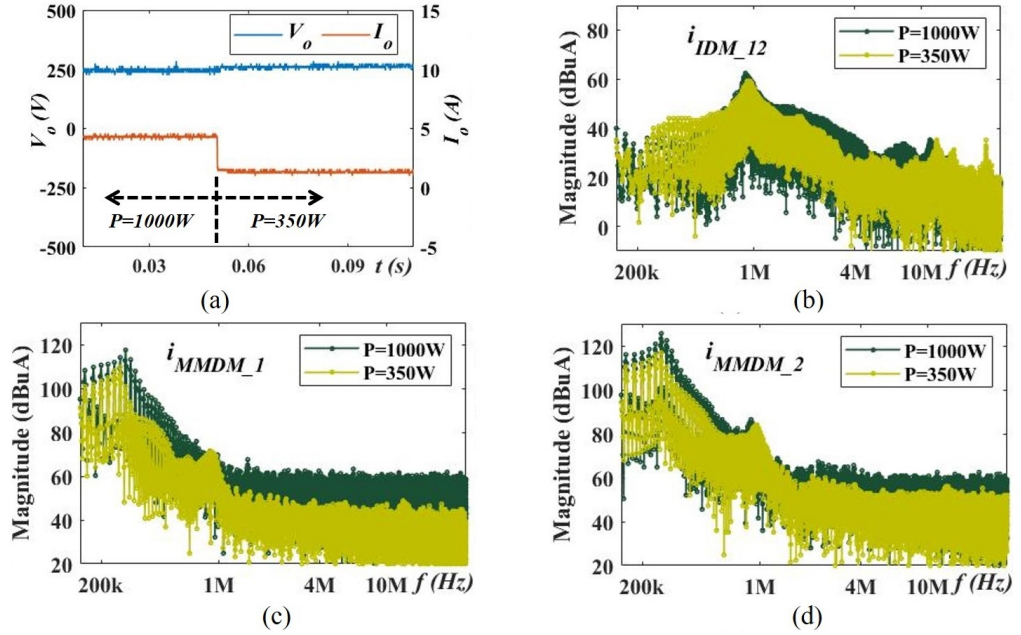
Figure 3.13: (a) Output voltage (V_o) and output current (I_o) for change in load power from 1000W to 350W, (b) measured frequency spectra i_{IDM_12} for 1000W and 350W, (c) measured frequency spectra i_{MMDM_1} for 1000W and 350W, and (e) measured frequency spectra i_{MMDM_2} for 1000W and 350W.

3.6.2 Measurement of i_{cm_TF} Current

The frequency spectra of the CM current measured at the primary side of the transformer and the VSC2 to ground current (i.e., $i_{C_c} + i_{C_d} + i_{C_3} + i_{C_4}$) are observed

to be equal, as shown in Figure 3.10(a). Thus, it can be concluded from Figure 3.10(a) that the VSC2 to ground current flow through C_{ps} and thus validating (3.4). The measured i_{cm_TF} in the DAB prototype using the current probe arrangement discussed in Chapter 1 is shown in Figure 3.10(b); the corresponding estimated spectrum using the CM equivalent circuit presented in Figure 3.2(d) is shown in Figure 3.10(b). As observed from Figure 3.10(b), the estimated and measured i_{cm_TF} is very close, which validates the transformer modelling and the CM equivalent circuit presented in Figure 3.2(d).

3.6.3 Measurement of IDM and MMDM Currents

To measure the i_{IDM_12} current, $C_{ext} = C_{ps} = 70$ pF is chosen i.e., $m = 1$. The matching capacitance profile of twice the C_{ps} with twice the C_{ext} is shown in Figure 3.10(c). It is observed from Figures. 3.11(a) and (b) that inserting C_{ext} does not alter either $v_{a'c}$ or v_{bd}. Also, from Figure 3.11(c), it is seen that i_{cm_TF} also does not vary without and with the C_{ext}. Therefore, the proposed external impedance-matched circuit is used to measure the DM current flowing through the transformer owing to the capacitive coupling.

The frequency spectra of i_{IDM_12} measured based on (3.19) and that estimated using the DM equivalent circuit presented in Figure 3.3(d) are shown in Figure (3.12)(a). The i_{MMDM_1} current is measured from i_{dm_1} and i_{dm_2}, as discussed in (3.21), and the same is estimated from the DM equivalent circuit. The corresponding results are shown in Figure 3.12(b). Similarly, the i_{MMDM_2} current is measured from i_{dm_3}, i_{dm_4} as discussed in (3.21); and the same is estimated from the DM equivalent circuit. The obtained frequency spectra of the measured and estimated i_{MMDM_2} are illustrated in Figure 3.12(c). It can be seen from the estimated and the measured i_{IDM_12} that the proposed equivalent circuit can predict the DM noise with a high degree of accuracy.

Moreover, the frequency spectra comparison of the i_{IDM_12}, i_{MMDM_1}, and i_{MMDM_2} current is shown in Figure 3.13 for the change in load from 1000W to 350W. The V_o and the output current (I_o) for the load change from 1000W to 350W is shown in Figure 3.13(a). It is observed from Figure 3.13(a) that, the V_o remain constant at 250V, while the I_o changes from 4.1A to 1.4A. The frequency spectra of the i_{IDM_12}, i_{MMDM_1}, and i_{MMDM_2} currents for change in P_o from 1000W to 350W are shown in Figures. 3.13(b), (c), and (d), respectively. It is observed that with reduction in P_o from 1000W to 350W, I_o decreases; thereby reducing the i_{IDM_12}, i_{MMDM_1}, and i_{MMDM_2} currents.
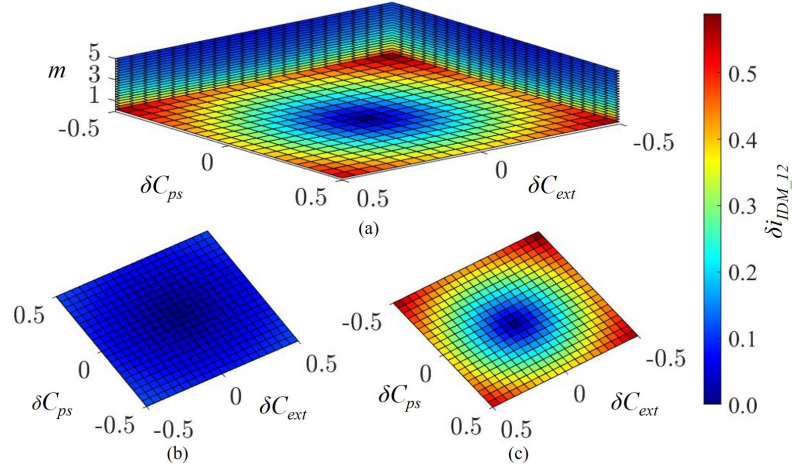
Figure 3.14: Uncertainty in i_{IDM_12} measurement due to uncertainty in C_{ps} and C_{ext} measurements for (a) m values ranging from 0.01 to 5, (b) $m = 0.01$, and (c) $m = 5$.

3.6.4 Sensitivity of the i_{IDM_12} Current Measurement Scheme to the Uncertainties in C_{ps} and C_{ext}

The uncertainties in the C_{ps} measurement during transformer parameter extraction affect the i_{IDM_12} current measurement. Also, the capacitor connected as C_{ext} has finite capacitance tolerance (varying between 5% to 20% for off-the-shelf components). Therefore, it is necessary to analyze the impact of these uncertainties on the measured i_{IDM_12} current. The DM current through the transformer with an impedance-matched external capacitor, C_{ext} is given by (3.18) and is simplified as

$$i = \frac{\omega(v_{a'b} - v_{cd})}{2}[C_{ps} + C_{ext}] \tag{3.22}$$

Let $\pm\delta C_{ps}$ and $\pm\delta C_{ext}$ be the uncertainties in the C_{ps} and C_{ext}, respectively. The uncertainty in i i.e., δi is [86]

$$\delta i = \frac{\omega(v_{a'b} - v_{cd})}{2}\sqrt{\delta C_{ps}^2 + \delta C_{ext}^2}. \tag{3.23}$$

Hence, the uncertainty in i_{IDM_12} i.e., δi_{IDM_12} is

$$\delta i_{IDM\_12} = \frac{\omega(v_{a'b} - v_{cd})}{2(1 + m)}\sqrt{\delta C_{ps}^2 + \delta C_{ext}^2}. \tag{3.24}$$

As evident from (3.24), the measured i_{IDM_12} is sensitive to uncertainty in C_{ps}, C_{ext}, and the choice of m; the same is quantified in Figure 3.14. It is observed from Figure 3.14(b) that the error in either C_{ps} or C_{ext} highly impacts i_{IDM_12} measurement for very low values of m. In addition, for high values of m, a significant change in $v_{a'c}$, v_{bd} and i_{cm_TF} can be observed for with and without C_{ext}; that leads to incorrect i_{IDM_12}

measurement.   Thus, the range of m has to be chosen considering the trade-off between the sensitivity and accuracy in the i_{IDM_12} current measurement.

3.7   Summary

The CM and DM equivalent circuits have been deduced to analyze the propagation paths of the individual ground currents and converter currents in the DAB converter. An impedance-match external capacitor is proposed as a suitable measurement technique to experimentally obtain the DM noise through the transformer.   The experimentally obtained CM and DM noise through the transformer is in close agreement with the analytical models. In addition, the sensitivity of the proposed measurement technique to the uncertainty in the estimated parasitics of the transformer and external measurement capacitor is also presented.   Along with the DM noise due to parasitics within the converter, termed IDM noise, the converter-to-ground parasitics result in additional DM noise, termed MMDM noise; thus increasing the overall DM noise in both primary and secondary sides of the transformer.   The propagation path for MMDM noise has been analyzed and the necessary mathematical expressions have been presented.

Chapter 4

CM Noise Mitigation Techniques with Integrated Magnetics

4.1 Introduction

The CM noise generated by the excitation of the converter-to-ground parasitics due to the high dv/dt switching nodes has to be reduced within the desired standard limits to ensure the EMC. Typically, passive CM filters, such as CM chokes and CM LC filters, are widely used at the DC input to attenuate the CM noise. This chapter introduces circulating CM current (CCMC), a persistent issue resulting from the incorporation of these CM filters. Additionally, a detailed discussion on a coupled-inductor-based integrated magnetic approach to mitigate CCMC is presented.

While the coupled inductor-based approach effectively reduces CCMC, it doesn't eliminate the need for a DC-input CM filter. Consequently, a concentric CM choke is designed to replace traditional toroidal CM chokes, aiming to reduce the space occupied by CM filters.

In addition to the aforementioned integrated magnetics approach for CM filtration, this chapter extensively explores a comparative analysis of the impact of discrete inductor and integrated transformers on the CM noise profile of the DAB converter. The CM choke requirement with the discrete inductor and the integrated transformer is presented in detail.

4.2 Coupled Inductor-Based Technique to Mitigate Circulating CM Current

In general, the propagation path of the circulating current, which arises due to the mismatch in the primary and the secondary voltages of the transformer, within the DAB converter is indicated by path A in Figure 4.1. The total CM current in the DAB converter tends to flow through the LISN, as indicated by path B in Figure 4.1. The CM noise analysis with the CM current propagating along Path B is widely explored [9], [87], [14]. Conventional input CM filters reduce the CM current through
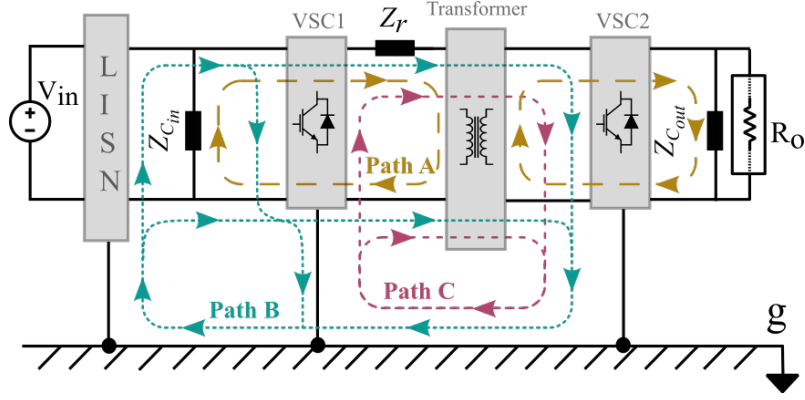
Figure 4.1: Indicating the propagation paths of CM current, circulating current (CC), and circulating CM current (CCMC).
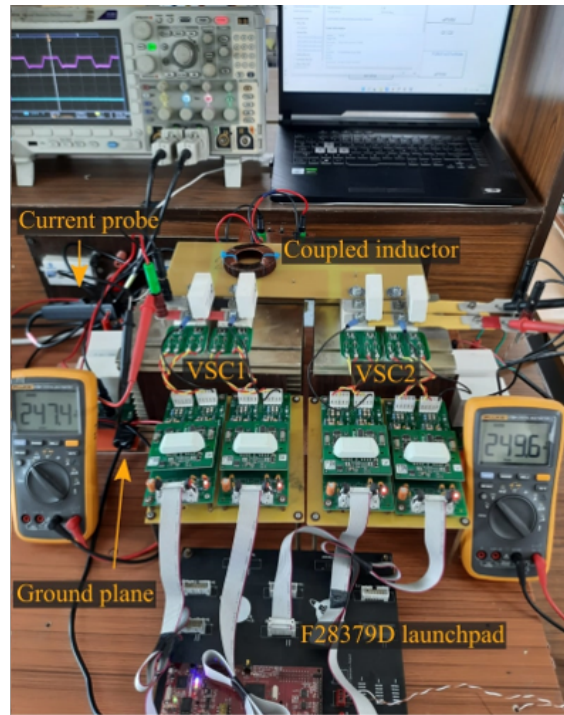
Figure 4.2: Experimental setup of isolated DAB converter.

the LISN within the desired standard limit. However, the CM current propagation through Path C, termed circulating CM current (CCMC), shown in Figure 4.1, is further discussed in detail.

As indicated by Path C in Figure 4.1, the high-frequency CCMC flows within the converter. This aids the near-field coupling between the converter components [88].

Table 4.1: Experimental Operating Conditions

Parameter	Value	Parameter	Value	Parameter	Value
V_{in}	250 V	V_o	250 V	Power	1 kW
f_{sw}	10 kHz	1:n	1:1	L_r	288 μH

4.2.1   Experimental Setup

The prototype DAB converter for the circulating CM current analysis is shown in Figure 4.2. The DAB converter is operated with SPST incorporating the F28379D launchpad. The detailed operating conditions are listed in Table 4.1. A LISN (LI-3P-232) is inserted at the DC input port to decouple the CM noise of the DAB converter from the external noise of the main supply. To analyze the CCMC, the CM noise model derived in Chapter 2 is considered, as shown in Figure 4.3(a). As seen the Figure 4.3(a), the ideal transformer windings in the CM noise model are replaced by the controlled voltage and current sources. Further, the reduced CM noise model, obtained from Figure 4.3(a), is shown in Figure 4.3(b) and is considered to analyze the CCMC in the DAB converter. The expressions for v_{cm_1} and v_{cm_2} in the simplified CM noise model shown in Fig. 4.3(b) are given by

$$v_{cm_1} = \frac{v_{an} + v_{bn}}{2} \ and \ v_{cm_2} = \frac{v_{cn'} + v_{dn'}}{2}. \tag{4.1}$$

While, the Z_k ($k = 1, 2, 3, 4, 5, 6$) impedance in Fig. 4.3(b) is given by

$$Z_1 = 0.5 Z_{LISN}, \ \ Z_2 = \frac{1}{j\omega(C_1 + C_2)}, \ \ Z_3 = \frac{1}{j\omega(C_a + C_b)}, \ \ Z_4 = \frac{1}{j\omega C_{ps}}, \tag{4.2}$$

$$Z_5 = \frac{1}{j\omega(C_c + C_d)}, Z_6 = \frac{1}{j\omega(C_3 + C_4)}, \ \ Z_7 = \frac{Z_r}{1 + j\omega Z_r C_p}, \ \ and \ Z_8 = j\omega(L_p + \frac{L_s}{n^2}). \tag{4.3}$$

(a)

(b)
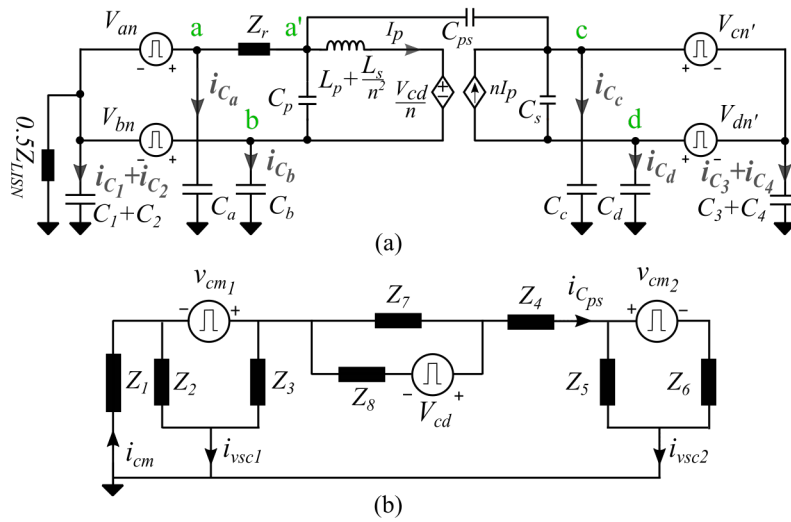
Figure 4.3: (a) CM noise model indicating the currents to the ground and (b) simplified CM noise model.
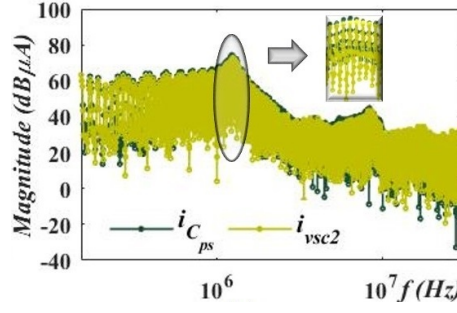
Figure 4.4: Frequency spectra of the i_{vsc2} and the $i_{C_{ps}}$ currents.
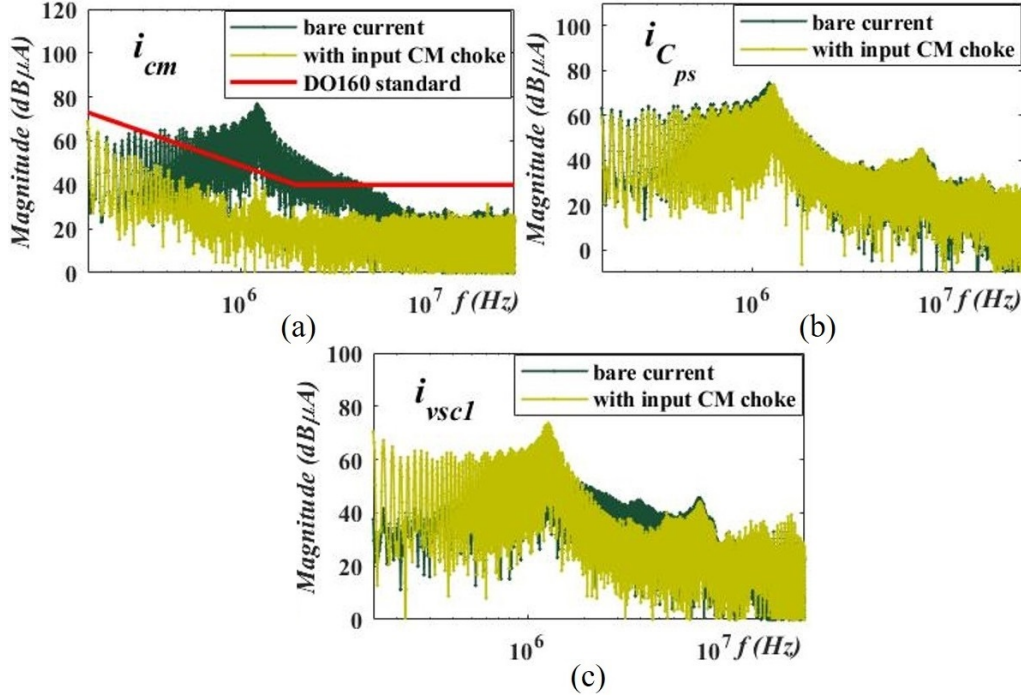
Figure 4.5: With the 1.5 mH CM choke, bare current frequency spectra of (a) i_{cm}, (b) $i_{C_{ps}}$, and (c) i_{vsc1}.

4.2.2   Origination of the CCMC

Further, the circumstances that originate the CCMC and the voltage source that results in the CCMC are discussed in detail.

The CM currents from the VSC1-to-ground and VSC2-to-ground are denoted by i_{vsc_1} and i_{vsc_2}, respectively, as indicated in Figure 4.3(b). The i_{vsc_1} and i_{vsc_2} are expressed in terms of the current through the parasitic capacitance, C_i $(i = a, b, c, d, 1, 2, 3, 4)$ as

$$i_{vsc1} = i_{C_a} + i_{C_b} + i_{C_1} + i_{C_2} \; and \; i_{vsc2} = i_{C_c} + i_{C_d} + + i_{C_3} + i_{C_4}. \qquad (4.4)$$

The algebraic sum of the i_{vsc1} and i_{vsc2} current gives the total CM current (i_{cm}) in the DAB converter. The i_{cm} current is measured by clamping the DC link wires into a high bandwidth current probe (TCP202A), as discussed in Chapter 1. As evident from Figure 4.3(b), the i_{vsc2} current returns from the ground to the converter through
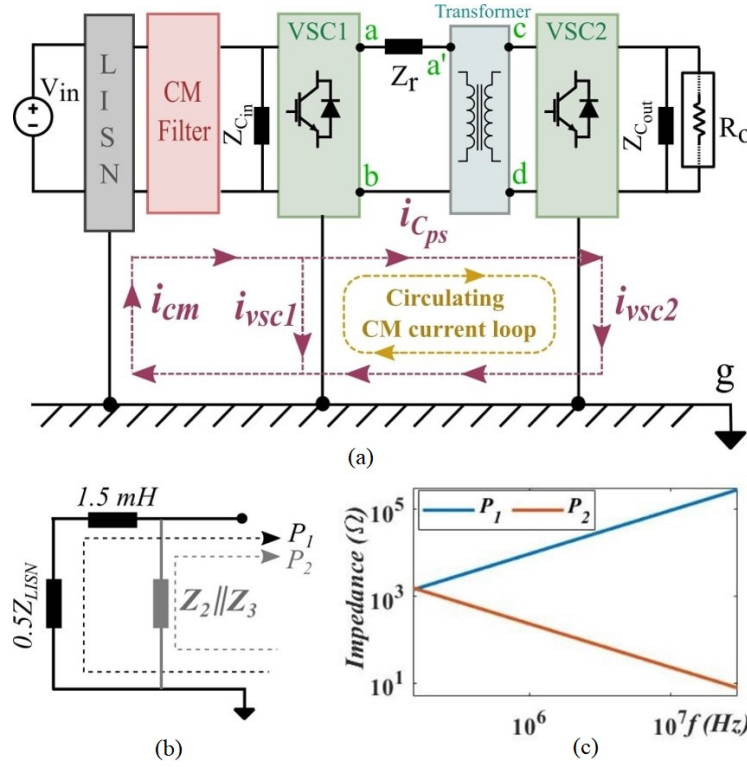
Figure 4.6: (a) CCMC loop formation, (b) impedances along path P_1 and P_2 with CM choke, and (c) impedances profile of P_1 and P_2 paths.

the Z_4 impedance. Therefore, the i_{vsc2} current is equal to the CM current through Z_4 or C_{ps} ($i_{C_{ps}}$) in the conducted EMI frequency range (150 KHz to 30 MHz), as shown from Figure 4.4. Since, the i_{vsc_2} and the $i_{C_{ps}}$ currents are identical, the i_{cm} current is rewritten as the algebraic sum of the i_{vsc_1} and the $i_{C_{ps}}$ currents.

The frequency spectrum of the measured i_{cm} current is shown in Figure 4.5(a). As observed from Figure 4.5(a), the i_{cm} current exceeds the DO160 limit line. To mitigate i_{cm} within the standard, the first-order and second-order CM filters namely CM choke and CM LC filter are employed at the DC-input port of the DAB converter, as shown in Figure 4.6(a). The impact of the input CM filters on the $i_{C_{ps}}$ and the i_{vsc1} currents are discussed further along with the origination of the CCMC.

Input CM choke to address the i_{cm} current

The frequency spectra of bare i_{cm}, $i_{C_{ps}}$, and i_{vsc1} currents measured simultaneously are shown in Figures 4.5(a), (b), and (c), respectively. It is observed from Figures 4.5(a) and (b) that, the $i_{C_{ps}}$ current component is dominant in the i_{cm} current. To mitigate i_{cm} within the standard limit, 1.5 mH CM choke is inserted at the input port of the DAB converter [89]. In Figure 4.5(a), the updated frequency spectrum of the i_{cm} current with the 1.5 mH CM choke is below the standard limit line. However, the 1.5 mH CM choke does not alter the $i_{C_{ps}}$ current, as evident from Figure 4.5(b); this is explained from the CM equivalent circuit shown in Figure 4.3(b). With the
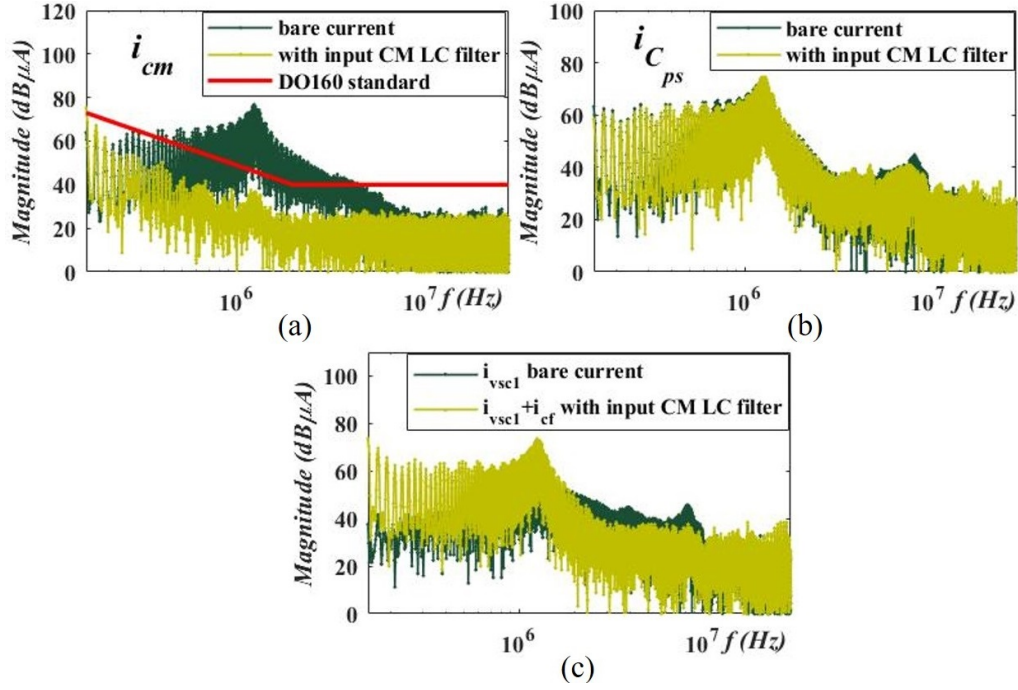
Figure 4.7: With the 1 mH and 1 nF CM LC filter, the frequency spectra for bare current of (a) i_{cm}, (b) $i_{C_{ps}}$, and (c) $i_{vsc1} + i_{cf}$.
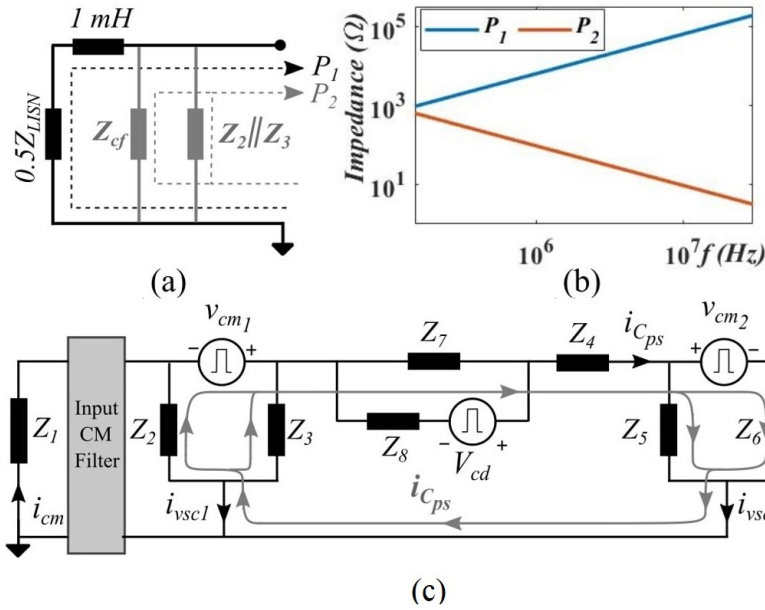
Figure 4.8: (a) Impedances along path P_1 and P_2 with CM LC filter, (b) impedances profile of P_1 and P_2 paths, and (c) indicating the propagation path of the CCMC with the input CM filter.

1.5 mH CM choke, the Z_1 is modified as shown in Figure 4.6(b), and is given by

$$Z_1(\omega) = \frac{Z_{LISN}}{2} + j\omega * (1.5 \ mH).\tag{4.5}$$

From (4.5), it is observed that, the 1.5 mH CM choke increases the impedance offered by Z_1. Therefore, the impedance offered by the P_1 path is higher than the

impedance offered along the P_2 path, as shown in Figure 4.6(c). Hence the $i_{C_{ps}}$ current tends to flow through the path P_2 i.e., through the Z_2 and Z_3 impedance; this results in the increment of the i_{vsc1} current, as evident from Figure 4.5(c). Thus, with the 1.5 mH CM choke, the $i_{C_{ps}}$ current tends to flow through the VSC1 to the ground parasitic impedances (Z_2, Z_3); thereby increasing the VSC1-to-ground current.

Input CM LC filter to address the i_{cm} current

To mitigate the i_{cm} current, the CM LC filter of 1 mH and 1 nF are inserted at the dc input port of the DAB converter [89]. With the input CM LC filter, the i_{cm} reduces within the standard limit line, as evident from Figure 4.7(a). However, the $i_{C_{ps}}$ current remains unchanged, as seen from Figure 4.7(b). This is analyzed from the CM equivalent circuit shown in Figure 4.3(c). With the CM LC filter, the modified Z_1 impedance is shown in Figure 4.8(a) and is given by

$$Z_1(\omega) = \frac{Z_{LISN}}{2} + j\omega * (1 \ mH) \tag{4.6}$$

The impedance offered by the Z_1 impedance increases due to the 1 mH inductance, as seen in (4.6). Therefore, the impedance along the path P_1 is higher than the impedance along the path P_2, as shown in Figure 4.8(b). The Z_{cf} in the path P_2 is the impedance of the 1 nF capacitance. Thus, the $i_{C_{ps}}$ current tends to flow through Z_{cf}, Z_2, and Z_3 and appears in the frequency spectrum of the currents in path P_2, as evident from Figure 4.7(c). Thus, with the input CM LC filter, the $i_{C_{ps}}$ current flows through the capacitor of the CM LC filter (Z_{cf}) and the VSC1-to-ground parasitic impedances (Z_2, Z_3); thereby increasing the VSC1-to-ground current.

Quantification of the CCMC and its voltage source

The bare $i_{C_{ps}}$ current, the $i_{C_{ps}}$ current with the input CM choke, and the $i_{C_{ps}}$ current with the input CM LC filter remain unaltered, as observed from Figures 4.5(b) and 4.7(b). Besides, inserting the input CM filter results in the flow of $i_{C_{ps}}$ through the Z_2, Z_3, Z_4, Z_5, Z_6, and the ground; thus, forming the CCMC loop, as indicated in Figure 4.8(c). Thus, the $i_{C_{ps}}$ is the CCMC that circulates between VSC1, VSC2, and the ground, as indicated in Figure 4.6(a).

Since $i_{C_{ps}}$ current is the CCMC, the voltage across Z_4 (v_{Z_4}) in the CM equivalent circuit in Figure 4.3(b) is the voltage source of the CCMC. To quantify the v_{Z_4}, the

Thevenin equivalent voltage and the impedance across the Z_4 is obtained as

$$V_{th} = \frac{Z_3(Z_1 + Z_2)}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3} v_{cm_1} - \frac{Z_5}{Z_5 + Z_6} v_{cm_2}$$

$$+ \frac{Z_7}{Z_7 + Z_8} v_{cd} \; and \tag{4.7}$$

$$Z_{th} = \frac{Z_1 Z_2 Z_3}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3} + \frac{Z_5 Z_6}{Z_5 + Z_6} + \frac{Z_7 Z_8}{Z_7 + Z_8} \tag{4.8}$$

Thus, the voltage source of CCMC (v_{Z_4}) is expressed as

$$v_{Z_4} = a v_{cm_1} - b v_{cm_2} + c V_{cd}, \tag{4.9}$$

$$a = \frac{Z_4 Z_3 (Z_1 + Z_2)}{(Z_4 + Z_{th})(Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3)}, \tag{4.10}$$

$$b = \frac{Z_4 Z_5}{(Z_4 + Z_{th})(Z_5 + Z_6)}, \; and \; c = \frac{Z_4 Z_7}{(Z_4 + Z_{th})(Z_7 + Z_8)}.$$

The following inferences are made from the above discussion.

1. The CCMC exists after inserting the input CM filters.

2. The $i_{C_{ps}}$ current forms a circulating current loop in the presence of the input CM filters. Hence, the CCMC is quantified as the $i_{C_{ps}}$ current.

3. The combined voltages, v_{cm1}, v_{cm2}, and V_{cd} acts as the voltage source of the $i_{C_{ps}}$ current, as evident from (4.9).

4.2.3   Design of Coupled Inductor to Mitigation CCMC

As the CCMC circulates between the VSC1 and VSC2 through Z_4, as observed from Figure 4.8(c), the CCMC can be addressed by altering the CM path impedance between the VSC1 and VSC2. Thus, the coupled inductor is chosen to address the CCMC as it (a) increases the CM impedance between VSC1 and VSC2; thereby reducing the CCMC and (b) incorporates the required L_r to transfer the desired power in the DAB converter without increasing the number of the magnetic components.

The coupled inductor is inserted at the transformer's primary side. The mutual inductance (M) and the self inductances $(L_1, \; L_2)$ of the coupled inductor are designed to serve as, (a) the CM filter to attenuate the CCMC and (b) the L_r to transfer the desired power to the load. The winding structure of the coupled inductor is simple and resembles that of the CM choke, as shown in Figure 4.9(a). The corresponding magnetic equivalent circuit is shown in Figure 4.9(b).
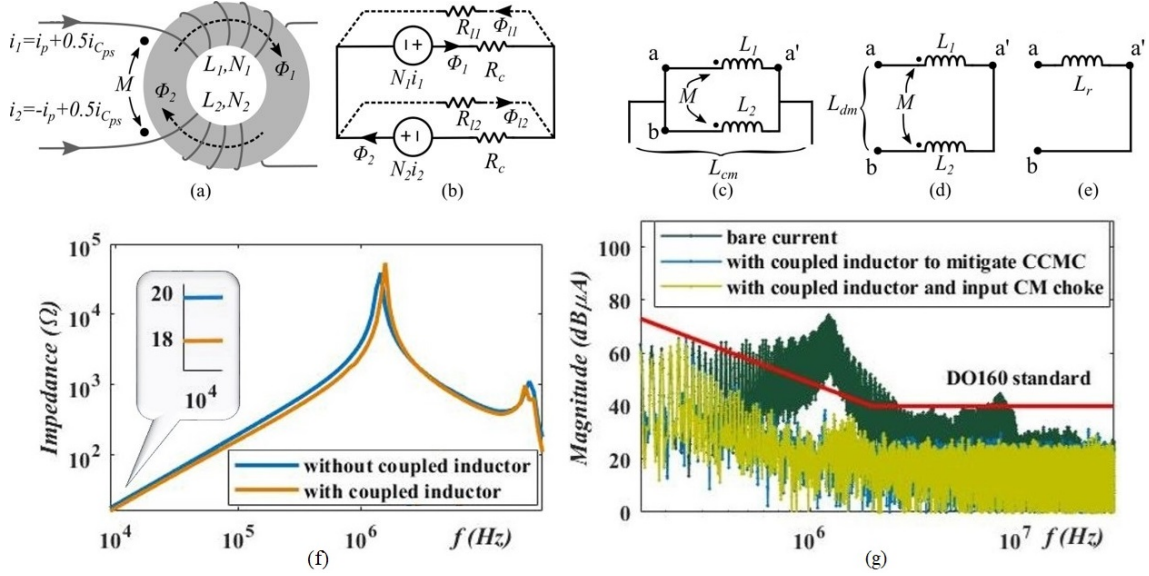
Figure 4.9: (a) Flux generated by the i_p and $i_{C_{ps}}$ in the coupled inductor, (b) magnetic equivalent circuit of the coupled inductor, (c) terminal connection to measure L_{cm}, (d) terminal connection to measure L_{dm}, (e) measurement of L_r, (f) matching differential mode impedance profile across a and b nodes with and without the coupled inductor, and (g) frequency spectra of bare current (dark green), with coupled inductor between VSC1 and VSC2 (blue), and with coupled inductor between VSC1 and VSC2 and the input CM choke for CCMC.

The CM and the differential mode (DM) inductance offered by the coupled inductor are given, using the CM and DM inductance measurement given in [90], as

$$L_{cm} = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} \ and \ L_{dm} = L_1 + L_2 - 2M. \tag{4.11}$$

The impedance due to L_{cm} attenuates the CCMC; the L_{dm} serves the purpose of L_r. To measure L_{cm} and L_{dm}, the terminal connections of the coupled inductor are indicated in Figure 4.9(c) and (d), respectively. For constant power transfer before and after employing the coupled inductor, the inductance measured across a and b nodes in Figure 4.9(d) should be equal to the inductance measured across a and b nodes in Figure 4.9(e). This implies that the L_{dm} is equal to L_r to maintain the desired operating conditions of the DAB converter. The L_1 and L_2 required to attain the desired L_{cm} and L_{dm} can be rewritten from (4.11) in terms of coupling coefficient (k) as

$$L_1 L_2 = \frac{L_{cm} L_{dm}}{1 - k^2} \ and \ L_1 + L_2 = L_{dm} + 2k \left(\frac{L_{cm} L_{dm}}{1 - k^2} \right)^{\frac{1}{2}}. \tag{4.12}$$

Thus, solving (4.12) gives the values of L_1 and L_2 of the coupled inductor to achieve the desired L_{cm} and L_{dm}.

Thus, the coupled inductor reduces the CCMC and avoids the necessity of the additional externally connected L_r. As the coupled inductor has weak coupling

between the windings, higher L_{dm} can be achieved; this increases the feasibility of the coupled inductors for various power levels in the DAB converter. Moreover, mitigation of the CCMC with the coupled inductor does not alter the number of magnetic components in the DAB converter while maintaining the system operating conditions.

To mitigate the CCMC in the prototype DAB converter, the L_{cm} and L_{dm} are calculated as 3.5 mH and 288 μH, respectively. The coupled inductor is indicated in Figure 4.2(a). Accordingly, the L_1 and L_2 values are calculated from (4.12) as 3.65 mH and 3.52 mH, respectively. The matching inductance profile of L_{dm} and L_r is shown in Figure 4.9(f); thus ensuring the 1 kW power flow with the coupled inductor. The DO160 EMI standard is chosen for the CCMC and the i_{cm} currents. From the frequency spectrum of the CCMC shown in Figure 4.9(g), it is evident that the coupled inductive passive mitigation technique effectively mitigates the CCMC. Thus, unlike the input CM filtration techniques, the coupled inductor-based technique effectively mitigates the CCMC.

4.3 Concentric CM Choke for CM Noise Mitigation

This section of the chapter presents the winding structure with concentric toroidal cores, termed concentric CM choke, to achieve higher CM inductance with minimal box volume, compared to the conventional CM choke. The step-by-step design guidelines are formulated to achieve volume reduction with the presented concentric CM choke configuration. Following the given design guidelines, the presented concentric CM choke can achieve the desired CM inductance by incorporating the 'n' number of concentric cores of different core materials. Unlike the concentric CM choke presented to achieve volume reduction in this paper, the similar configurations discussed in [91], [92], and [72] intend to increase the DM inductance of the conventional CM choke. This increase in the leakage inductance of the CM choke, at the expense of reduced DM saturation current, emanates the saturation issues in the CM choke core. Besides, the DM noise is usually filtered out with a small input filter and high-frequency capacitors; whereas the CM noise attenuation requires a bulky discrete filter which limits the power density of the converter [93],[94]. Thus, the winding structure and design of the concentric CM choke presented in this chapter reduce the box volume by retaining the design simplicity of the conventional CM choke, without any additional design considerations in terms of saturation of the core. The reduction in the box volume of the designed concentric CM choke, compared to the conventional CM choke, is verified experimentally for a DAB converter prototype.
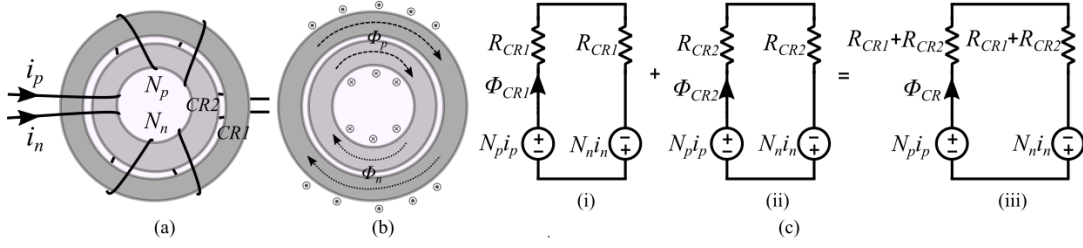
Figure 4.10: (a) Concentric CM choke, (b) flux distribution in cores CR1 and CR2, (c) magnetic circuits of (i) CR1 core, (ii) CR2 core, and (iii) concentric CM choke.

4.3.1 Design of Concentric CM Choke

The winding structure of the concentric CM choke with two cores, $CR1$, and $CR2$ is shown in Figure 4.10(a). The orientation of flux generated by the phase and null windings with N_p and N_n number of turns, respectively, in $CR1$ and $CR2$ cores is shown in Figure 4.10(b). The magnetic circuit of $CR1$ and $CR2$, and the concentric CM choke are given in Figure 4.10(c)(i), (ii), and (iii), respectively. ϕ_{CR1}, ϕ_{CR2} and ϕ_{CR} are the total flux in $CR1$, $CR2$ and the concentric CM choke, respectively. In Figure 4.10(c), R_{CR1} and R_{CR2} are half the reluctance of $CR1$ and $CR2$ cores, respectively, and are given by

$$R_{CRi} = \frac{l_{ei}/2}{\mu_o \mu_{ri} A_{ei}}, \tag{4.13}$$

where, l_{ei}, μ_{ri}, and A_{ei} are the mean magnetic length, relative permeability, and the area of the cross-section of the ith core, respectively. The flux in the concentric CM choke can be written as

$$\begin{aligned}
\phi_p &= \phi_{lp} + \phi_{m_{pp}} + \phi_{m_{pn}} \\
&= \phi_{lp} + \frac{N_p i_p}{2(R_{CR1} + R_{CR2})} + \frac{N_n i_n}{2(R_{CR1} + R_{CR2})} \ and
\end{aligned} \tag{4.14}$$

$$\begin{aligned}
\phi_n &= \phi_{ln} + \phi_{m_{nn}} + \phi_{m_{np}} \\
&= \phi_{ln} + \frac{N_n i_n}{2(R_{CR1} + R_{CR2})} + \frac{N_p i_p}{2(R_{CR1} + R_{CR2})},
\end{aligned} \tag{4.15}$$

where ϕ_p and ϕ_n are the fluxes due to phase and null windings, respectively; ϕ_{li} is the leakage flux of i_{th} winding, ϕ_{mii} is the magnetizing flux of i_{th} winding linking itself, and ϕ_{mij} is the magnetizing flux of ith winding linking the jth winding. Thus, the total flux generated in the concentric CM core is $\phi_{CR} = \phi_p + \phi_n$. If r_p and r_n are the winding resistances of phase and null windings, respectively, the respective

$$\begin{bmatrix} V_p \\ V_n \end{bmatrix} = \begin{bmatrix} r_p & 0 \\ 0 & r_n \end{bmatrix} \begin{bmatrix} i_p \\ i_n \end{bmatrix} + \begin{bmatrix} L_{lp} + \frac{N_p^2}{2}(\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}}) & \frac{N_p N_n}{2}(\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}}) \\ \frac{N_p N_n}{2}(\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}}) & L_{ln} + \frac{N_n^2}{2}(\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}}) \end{bmatrix} \begin{bmatrix} \frac{di_p}{dt} \\ \frac{di_n}{dt} \end{bmatrix}$$
(4.17)

voltages are given by

$$\begin{bmatrix} V_p \\ V_n \end{bmatrix} = \begin{bmatrix} r_p & 0 \\ 0 & r_n \end{bmatrix} \begin{bmatrix} i_p \\ i_n \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} N_p \phi_p \\ N_n \phi_n \end{bmatrix}.$$
(4.16)

Substituting (4.14) and (4.15) in (4.16) gives the voltage across phase and null windings as shown in (4.17).

4.3.2 Estimation of CM Inductance

To analyze the CM performance of the concentric CM choke, substituting, $N_p = N_n = N$, $i_p = i_n = i_{cm}/2$, and $V_p = V_n = v_{cm}$ in (4.17) gives

$$v_{cm} = r_p \frac{i_{cm}}{2} + \Big(\frac{L_{lp}}{2} + \frac{N^2}{2}\Big[\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}}\Big]\Big)\frac{di_{cm}}{dt}.$$
(4.18)

Neglecting the winding resistance (r_p) and the leakage inductance (L_{lp}) gives the CM inductance of the concentric CM choke as

$$L_{cm} = \frac{N^2}{2}\Big(\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}}\Big).$$
(4.19)

Thus, the generalized expression for the CM inductance of the concentric CM choke with n concentric cores can be written as

$$L_{cm} = \frac{N^2}{2}\Big(\frac{1}{R_{CR1}} + \frac{1}{R_{CR2}} + \frac{1}{R_{CR3}} + ... + \frac{1}{R_{CRn}}\Big),$$
(4.20)

where R_{CRn} is half the reluctance of the nth core. Besides, the L_{cm} of the conventional CM choke is given by [95]

$$L_{cm_{conv}} = \frac{N^2}{2R_{CR}},$$
(4.21)

where N is the number of turns and R_{CR} is the reluctance of one-half of the conventional CM choke core.

Thus, from (4.20) and (4.21), it is evident that the concentric CM choke has more flexibility to combine various cores and obtain the desired L_{cm}, unlike the conventional CM choke. The design guideline to achieve the desired L_{cm} with the concentric CM choke is formulated in the flowchart given in Figure 4.11.

Table 4.2: Volume Comparison of Conventional and Concentric CM Chokes of 9 mH

CM choke	Core	Core material	μ_r	OD (mm)	ID (mm)	H_t (mm)	R_{CRi}	N	Box volume (mm^3)
Conventional	CR1	Nanocrystalline	55000	29.2	24.19	16.2	29812.92	16	13812.768
Concentric	CR2	Nanocrystalline	15000	25.26	19.89	11.11	125532.92	12	7088.931
	CR3	Nanocrystalline	55000	17.13	8.23	7.4	16758.875	12	
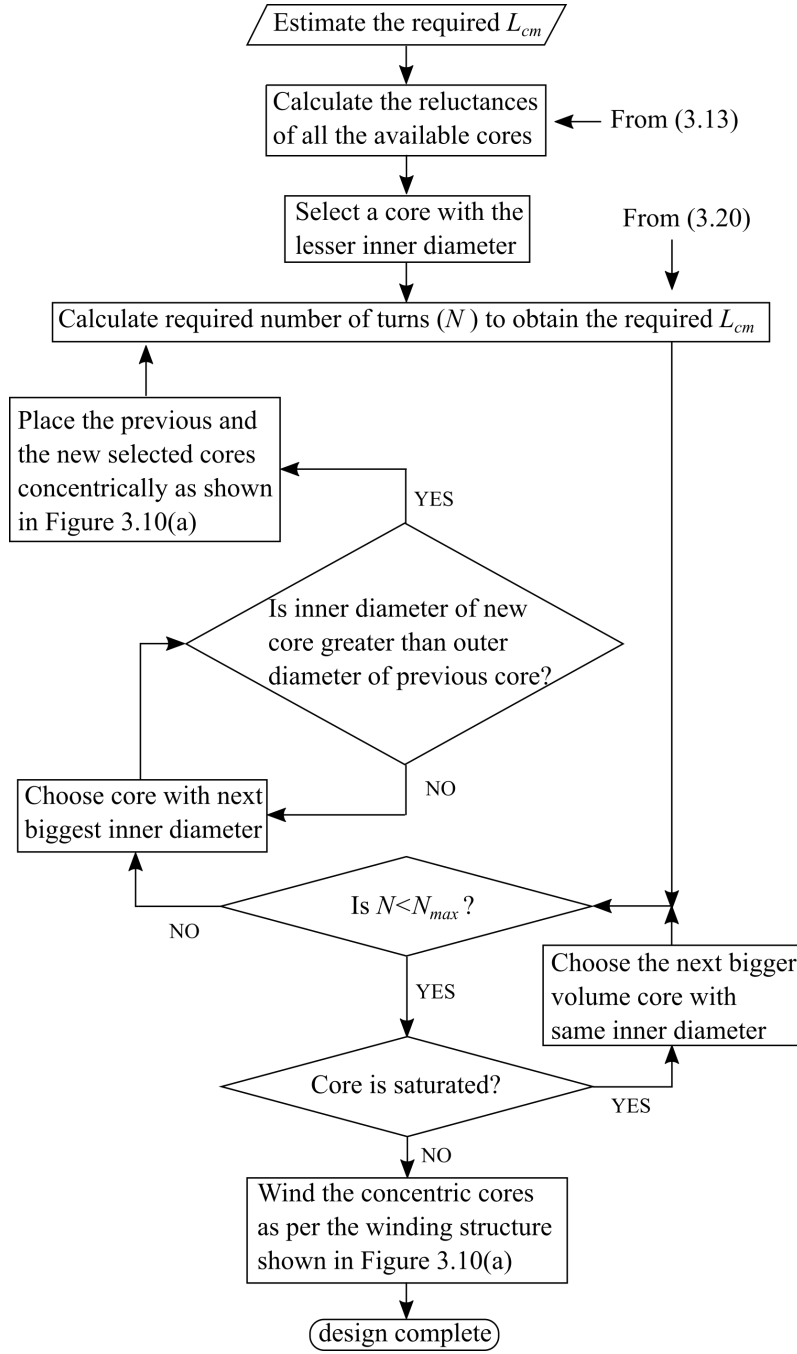
Figure 4.11: Design guidelines for concentric CM choke.

As per the guidelines in Figure 4.11, initially, the core with a smaller inner diameter has to be chosen and then another core that fits concentrically with the previous core is selected. If the L_{cm} of this concentric structure, calculated from (4.20), does not meet the desired L_{cm}, another core is chosen to place concentrically with the previous concentric structure. Thus, the procedure is repeated till L_{cm} calculated from (4.20), meets the desired L_{cm}.

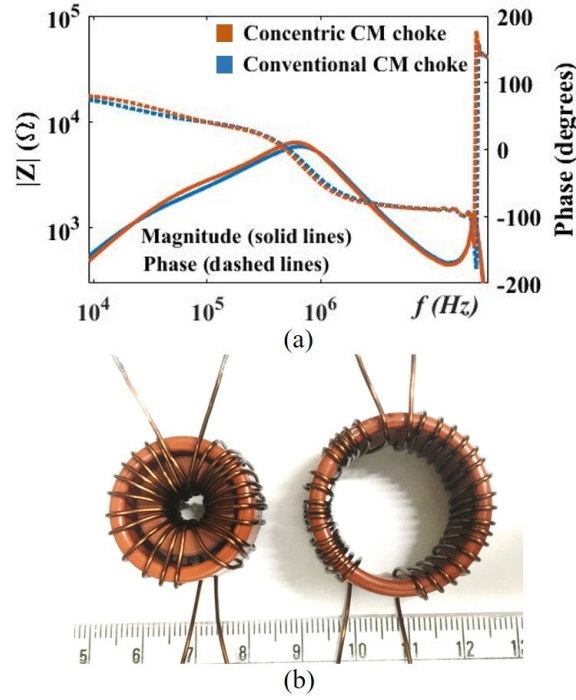
Figure 4.12: Comparison of (a) impedance profile and (b) volume, for concentric and conventional CM chokes.

4.3.3 Box Volume Comparison of Concentric and Conventional CM Choke

Let the desired CM inductance (L_{cm}) be 9 mH. The $CR1$ core with the magnetic properties and the physical dimensions mentioned in Table 4.2 is used to design the conventional CM choke. With the number of turns and the reluctance as given in Table 4.2, the L_{cm} estimated from (4.21) is 8.58 mH; while the L_{cm} measured with the impedance analyzer is 8.44 mH. The CM impedance profile of the designed conventional CM choke is shown in Figure 4.12(a).

Further, to design the concentric CM choke, $CR2$ and $CR3$ cores with the physical dimensions and the magnetic properties given in Table 4.2 are chosen, as per the guidelines mentioned in Figure 4.11. To attain the desired L_{cm} (i.e., 9 mH) with $CR2$ and $CR3$ cores, the number of turns estimated from (4.20) is 12. Thus, the L_{cm} of the designed concentric CM choke is measured using an impedance analyzer (PSM3750) as 9.16 mH. The CM impedance profile of the concentric CM choke is shown in Figure 4.12(a). It is to be noted that, the CM impedance profiles of conventional and concentric CM chokes match with great accuracy within the conducted EMI frequency range (i.e., from 150 kHz to 30 MHz).

The box volume of the conventional CM choke and concentric CM choke is calculated as 13812.768 mm^3 and 7088.931 mm^3, respectively, as mentioned in Table 4.2. It is to be noted that the $CR1$ core depicts the box volume of the conventional CM
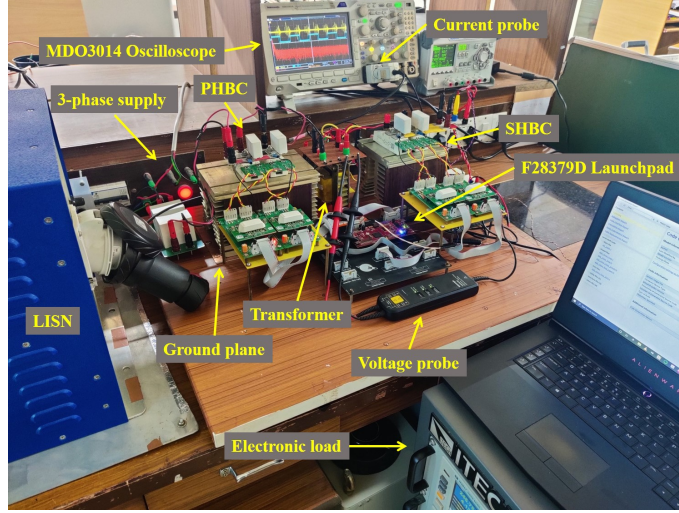
Figure 4.13: Experimental setup of DAB converter.

Table 4.3: System Operating Parameters

Parameter	Value	Parameter	Value	Parameter	Value
V_{in}	300 V	f_{sw}	10 kHz	Power	1115W
V_o	300V	1:n	1:1	$L_r + L_l$	618 µH

choke; while the physical dimensions of the $CR2$ core depict the box volume of the concentric CM choke. Hence, the box volume of the concentric CM choke is reduced by 48.67% when compared to the conventional CM choke, as shown in Figure 4.12(b). Thus, for the desired CM inductance, the concentric CM choke occupies a lower box volume compared to the conventional CM choke.

4.3.4   Experimental Validation of Concentric CM Choke

The analysis presented for the concentric CM choke is validated experimentally using a single-phase DAB converter prototype incorporating Si-IGBT modules.The experimental setup of the DAB converter prototype is shown in Figure 4.13. The experimental parameters for testing are mentioned in Table 4.3 with the DAB controlled using the SPS control technique.

A CM choke of 1.75 mH attenuates the i_{cm} within the DO160 standard limit line, as evident from Figure 4.14(a). Therefore, a concentric CM choke of 1.75 mH is designed as per the guidelines in the flowchart given in Figure 4.11. The magnetic properties and dimensions of the conventional and the designed concentric CM choke are detailed in Table 4.4. It is evident from Figure 4.14(a) that the conventional CM choke and the designed concentric CM choke attenuate i_{cm} within the standard.

The calculated box volume of the conventional CM choke and the designed concentric CM choke are given in Table 4.4. The box volume of the concentric CM choke is

Table 4.4: Volume Comparison of Conventional and Concentric CM Choke

	L_{cm} (mH)	N	μ_r	OD (mm)	ID (mm)	H_t (mm)	R_{CRi}	Box volume (mm³)
Conventional CM choke	1.75	40	800	61	35.55	12.7	911456.31	**47256.7**
Concentric CM choke	1.74	19	800	35.55	22.85	12.7	1113434.80	**16050.3**
			5000	22.01	13.52	8.04	255225.25	
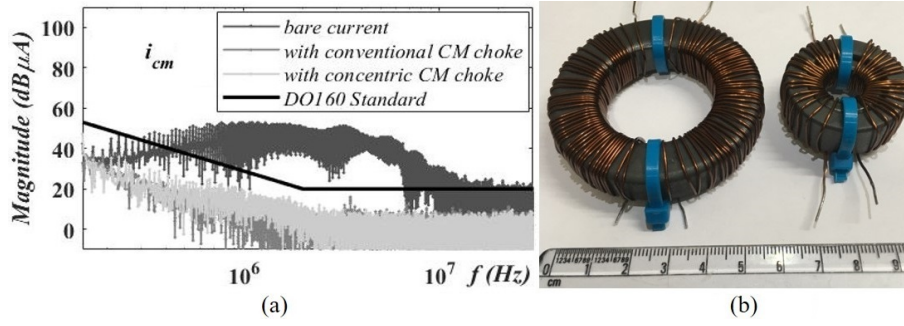
Figure 4.14:   (a) Frequency spectrum of bare i_{cm} current, with 1.75 mH conventional CM choke, and with 1.74 mH concentric CM choke, and (b) size comparison of conventional (left) and concentric (right) CM chokes.

reduced by 77.46% compared to the conventional CM choke, as evident from Table 4.4. This reduction in the box volume can also be observed from the conventional and concentric CM chokes of 1.75 mH shown in Figure 4.14(b). Hence, the proposed concentric CM choke attenuates the i_{cm} current with the reduced box volume when compared to the conventional CM choke. Thus, the concentric CM choke acts as a better replacement for the conventional CM chokes in terms of volume occupancy.

4.4   CM Noise Analysis of DAB Converter with Integrated Transformer

With the concept of integrated magnetics, the externally connected discrete inductor, employed to transfer the desired power flow, is integrated into the transformer, termed integrated transformer, by suitably designing its leakage inductance [63]. Studies reveal that incorporating the integrated transformer has the benefits of a minimum number of magnetic components, lower losses, and lesser volume, thereby improving the power density of the converter [63], [64], [65]. The general techniques employed to design an integrated transformer with the desired leakage inductance are as follows [63], [96].

1. By altering the distance between the primary (p) and secondary (s) windings, as shown in Figures 4.15(a), (b), and (c), the leakage inductance requirement of few μH can be achieved.

2. By modifying the transformer core structure either by increasing the air gap, as shown in Figures 4.15(c) and (d), or by employing external magnetic components such as leakage layers and magnetic shunts, as shown in Figures 4.15(e) and (f).

The above-listed techniques to design the integrated transformer result in a change in the transformer intrawinding parasitic capacitance, which significantly influences
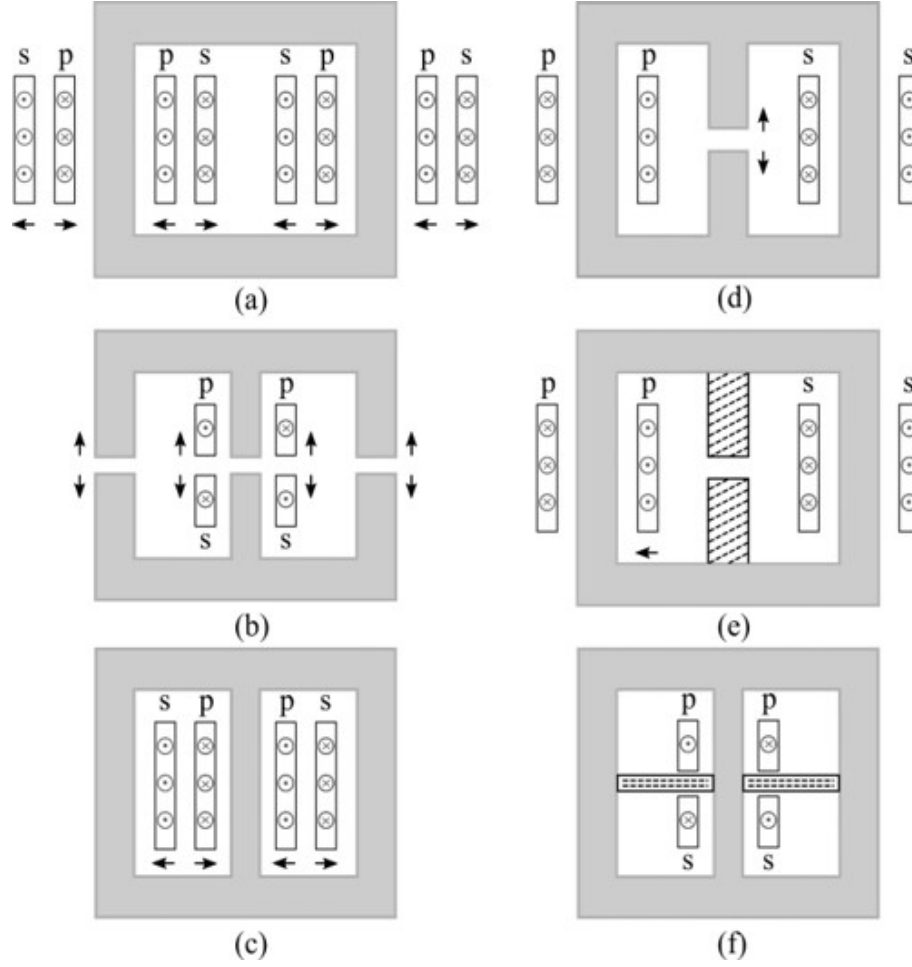
Figure 4.15: Winding and core modifications for improving leakage inductance of integrated transformers employed for DAB converter.

the CM noise of the DAB converter. Therefore, the change in the transformer's intrawinding parasitic capacitance is understood from the electric field distribution simulated in ANSYS, as shown in Figure 4.16.

4.4.1 Magnetic Tank Parasitic Consideration for CM Noise Analysis

In the magnetic tank, a shell-type transformer with the increase in the distance (d) between primary (p) and secondary (s) windings is considered, to achieve the desired leakage inductance, as shown in Figure 4.17(a). The parasitic elements of the transformer constitute primary leakage inductance (L_p), secondary leakage inductance (L_s), magnetizing inductance (L_m), primary winding turn-to-turn capacitance (C_p), secondary winding turn-to-turn capacitance (C_s), and primary-to-secondary winding parasitic capacitance (C_{ps}), as shown in Figure 4.18(a). L_p and L_s contribute to the power transfer in the DAB converter. The C_{ps} of the integrated transformer accounts for the CM noise propagation between VSC1
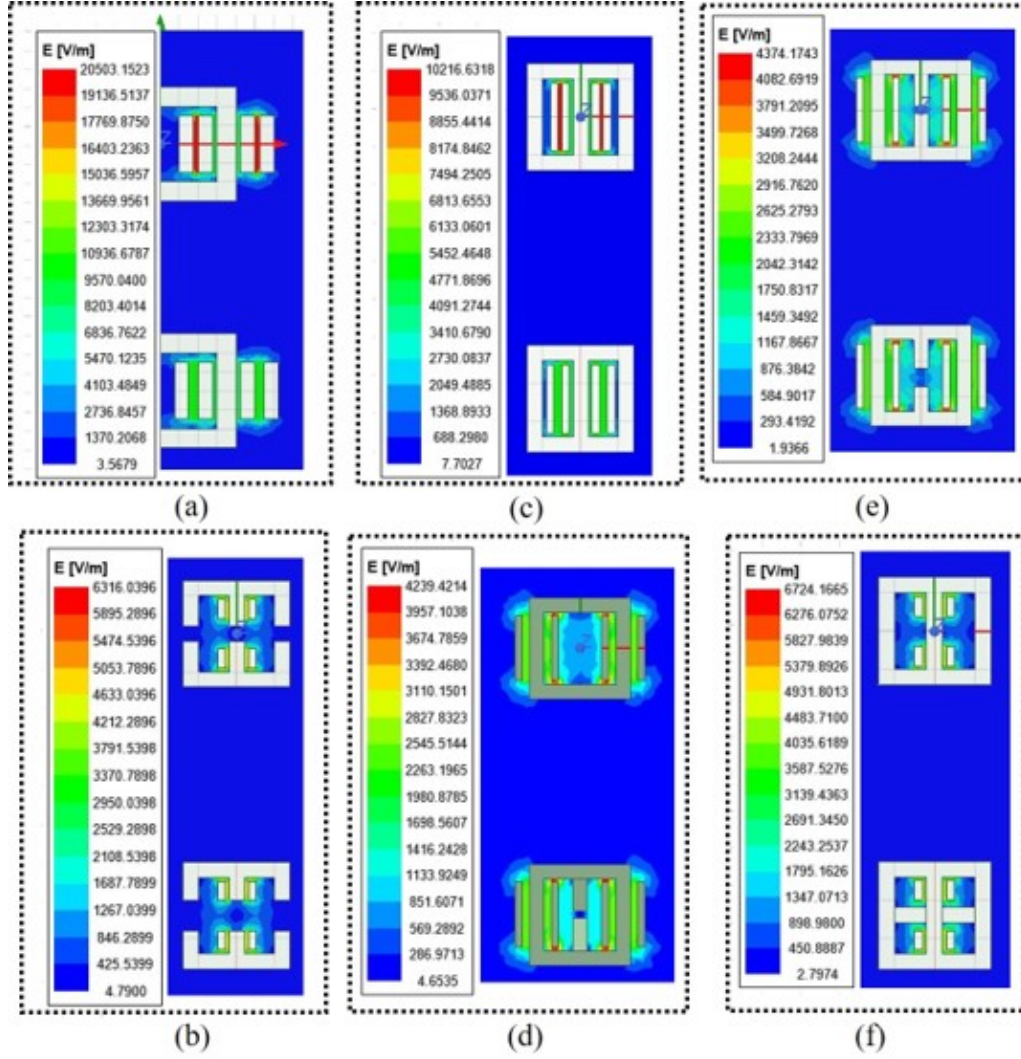
Figure 4.16:   Electric field distribution to analyze the various integrated transformer's intrawinding parasitic capacitance, C_{ps}.

and VSC2. Hence, the impact of the increase in d to achieve the desired leakage inductance on C_{ps} is further analyzed.

The capacitance C_{ps} for the cylindrical winding structure is given by [80]

$$C_{ps} = \frac{4\pi\epsilon_o\epsilon_r z r_o}{\ln\frac{r+d}{r}},$$

(4.22)

where z is the number of turns per layer, r is the radius of the primary winding, and r_o is the radius of the copper wire including the insulation. The effective dielectric constant (ϵ_r) is calculated from

$$\epsilon_r = \frac{d}{\frac{d_1}{k_1} + \frac{d_2}{k_2} + \frac{d_3}{k_3} + ...},$$

(4.23)

where k_i, $i = \{1, 2, 3, ...\}$ is the dielectric constant of each insulating layer spread
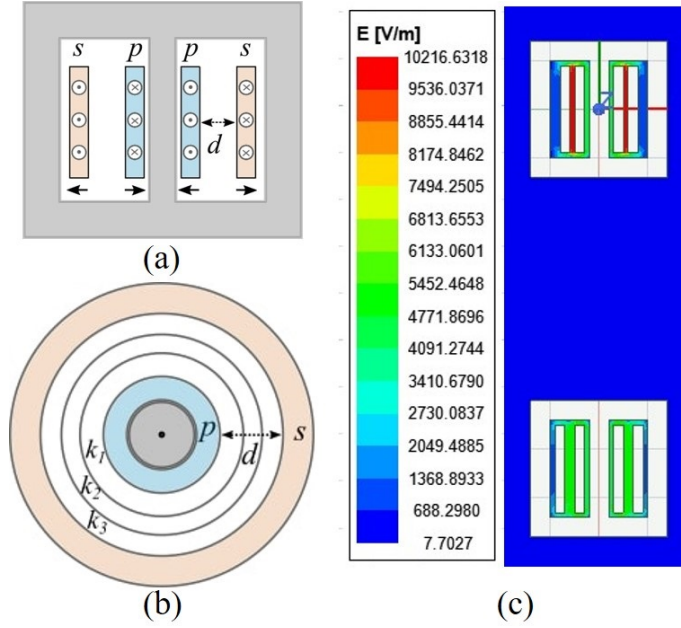
Figure 4.17: (a) Modifications in a shell-type transformer to achieve the desired leakage inductance, (b) top cross-sectional view of the transformer, and (c) electric field variation with the increase in d.

with thickness d_i, $i = \{1, 2, 3, ...\}$, as shown in Figure 4.17(b). With an increase in d, the electric field between the primary and secondary windings decreases, as shown in Figure 4.17(c); therefore, an increase in d reduces C_{ps}. Thus, it can be concluded that an increase in the distance between the p and s windings, to obtain the desired leakage inductance, reduces C_{ps}. In addition, the reduction in C_{ps} reduces the VSC2-to-ground currents and thereby reduces the total CM noise in the DAB converter.

Further, the CM noise analysis of the DAB converter incorporating the integrated transformer shown in Figure 4.17(a) is discussed in detail.

4.4.2 CM Noise Analysis with Integrated Transformer

The CM noise model of the DAB converter is shown in Figure 4.18(a). The Thevenin impedance across Z_{LISN} gives the CM impedance (Z_{cm}) of the DAB converter, as shown in Figure 4.18(b). Further simplifying the circuit in Figure 4.18(b) gives the Z_{cm} circuit shown in Figure 4.18(c). In general, as L_s is comparatively lower than L_m, the parallel combination of L_m and L_s in Figure 4.18(c) is approximated as L_s. The series combination of L_p and L_s gives the total leakage inductance of the transformer (L_l). Thus, the resultant Z_{cm} circuit is shown in Figure 4.18(d). Where, Z_{vsc1} and Z_{vsc2} are the equivalent ground parasitic impedances of VSC1 and VSC2,
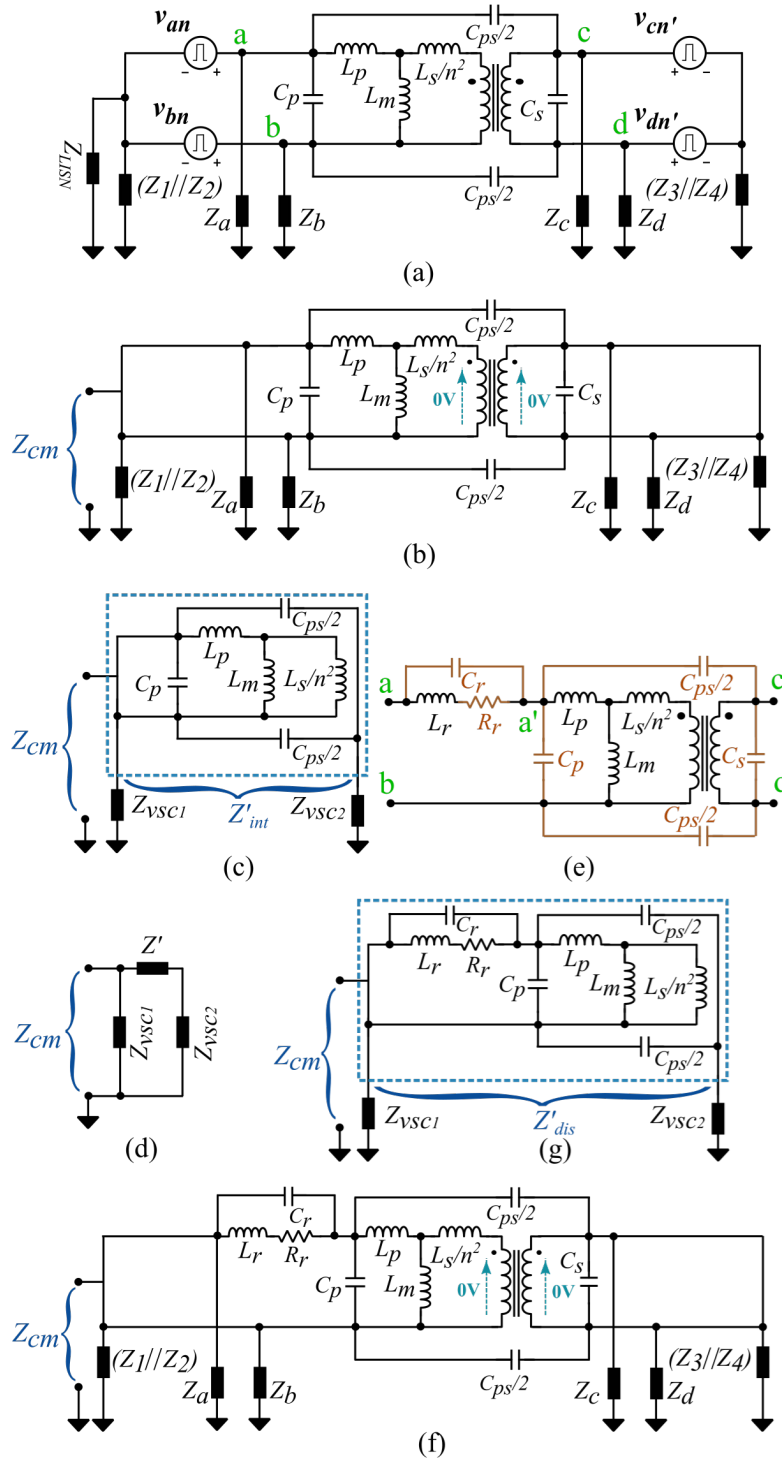
Figure 4.18: (a) CM noise model, (b) Z_{cm} circuit, (c) intermediate Z_{cm} circuit, (d) resultant Z_{cm} circuit, (e) magnetic tank with discrete L_r, (f) Z_{cm} circuit with discrete L_r, and (g) intermediate Z_{cm} circuit with discrete L_r.

respectively, and are given as

$$Z_{vsc1} = \frac{Z_a Z_b Z_1 Z_2}{Z_a Z_b (Z_1 + Z_2) + Z_1 Z_2 (Z_a + Z_b)}, \tag{4.24}$$

$$Z_{vsc2} = \frac{Z_c Z_d Z_3 Z_4}{Z_c Z_d (Z_3 + Z_4) + Z_3 Z_4 (Z_c + Z_d)}. \tag{4.25}$$

The impedance Z' in Figure 4.18(d) is the impedance of the magnetic tank circuit. Thus, from Figure 4.18(d), Z_{cm} can be written as

$$Z_{cm} = \frac{Z_{vsc1}(Z_{vsc2} + Z')}{Z_{vsc1} + Z_{vsc2} + Z'}. \tag{4.26}$$

The impedance Z' with integrated transformer (Z'_{int}) is given from Figure 4.18(c) as

$$Z'_{int} = \frac{1}{sC_{ps}}. \tag{4.27}$$
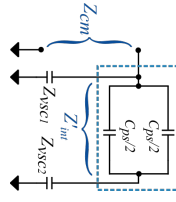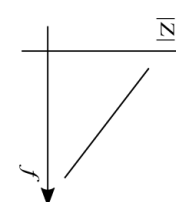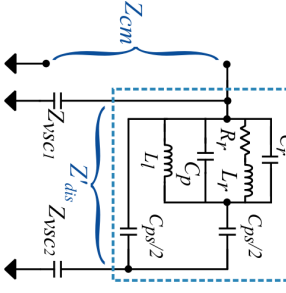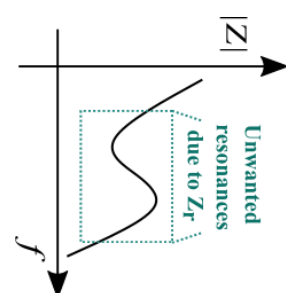
Thus, the Z_{cm} in the DAB converter with an integrated transformer is ideally capacitive, as mentioned in Table 4.5.

4.4.3   Comparison of CM Impedance without and with the Integrated Transformer

The magnetic tank circuit, without the integrated transformer, is composed of a discrete inductor (L_r) and a transformer, as shown in Figure 4.18(e). In Figure 4.18(e), R_r and C_r denote the equivalent series resistance and equivalent shunt capacitance of L_r, respectively. Thus, the Z_{cm} circuit incorporating the magnetic tank with discrete L_r is shown in Figure 4.18(f). Further simplifying the circuit in Figure 4.18(f) gives the Z_{cm} circuit shown in Figure 4.18(g). The Z' with discrete L_r (Z'_{dis}) is obtained from Figure 4.18(g) and is given by (4.28) in Table 4.5.

As evident from Figure 4.18(g), the presence of discrete L_r stimulates the influence of C_p, L_p, and L_s on the Z_{cm} along with C_{ps}, C_{phbc}, and C_{shbc}. Hence, the presence of discrete L_r generates unwanted resonances in the Z_{cm} impedance profile, as shown in Table 4.5; thereby increasing the CM noise of the DAB converter at resonant frequency with minimum Z_{cm} magnitude. The impedance profiles of Z_{cm} with integrated and discrete L_r are given in Table 4.5 assuming the Z_{vsc1} and Z_{vsc2} as capacitive impedances. With integrated L_r, the values of C_p, L_p, and L_s do not affect the Z_{cm} impedance profile and thereby do not influence the CM noise; thus eliminating the undesired resonances in the impedance profile of Z_{cm}. Hence, the integrated L_r improves the CM noise performance of the DAB converter. Thus, from the aforementioned analysis, the magnetic tank with an integrated transformer is preferred over the magnetic tank with discrete L_r for better CM noise performance of the DAB converter.

Table 4.5: CM Impedance Models for Discrete and Integrated Magnetic Tank Cases

Case	Approximate Z_{cm} model	Approximate Z_{cm} plot	Remarks
Integrated L_r			• Impact of only C_{ps}, C_{vsc1}, and C_{vsc2} is seen in Z_{cm}. • Comparatively fewer design complications.
Discrete L_r			• Effect of C_p comes into play along with C_r, C_{ps}, C_{vsc1}, and C_{vsc2} (increases the parameters that complicate the effective design for pre-compliance test). • Additionally, unwanted resonances occur at a frequency defined by L_r, L_l, C_p, and C_r. $$Z'_{dis} = \frac{2}{sC'_{ps}}\left[\frac{s^2L_l(sL_r+R_r)(C_{ps}+2C'_r+2C_p)+2s(L_r+L_l)+2R_r}{s^2L_l(sL_r+R_r)(C_{ps}+4C'_r+4C_p)+4s(L_r+L_l)+4R_r}\right]$$ (4.28)
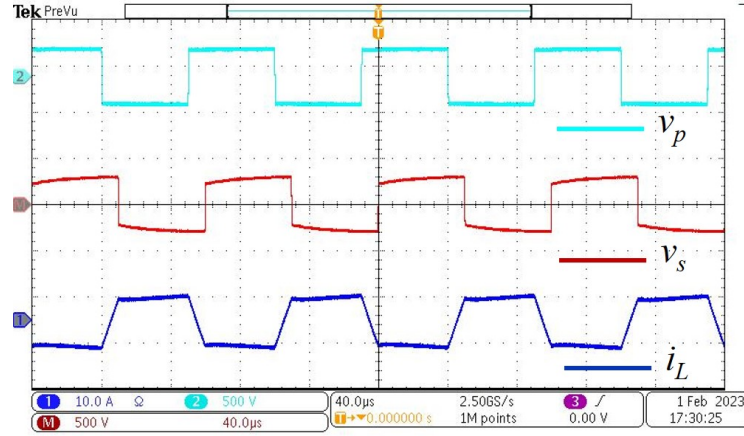
Figure 4.19: Time-domain profiles of transformer's primary voltage (v_p), secondary voltage (v_s), and primary current (i_L) of the DAB converter incorporating the integrated transformer.
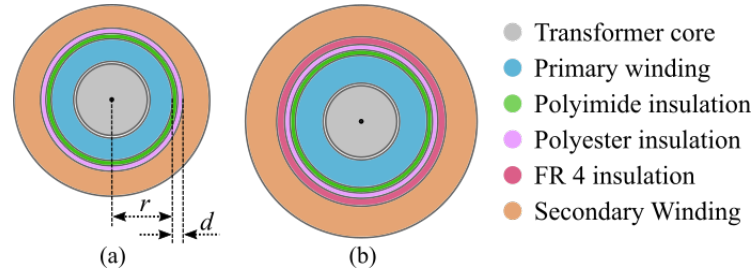
Figure 4.20: Top cross-sectional view of (a) conventional transformer incorporated with the discrete L_r in the magnetic tank and (b) integrated transformer.
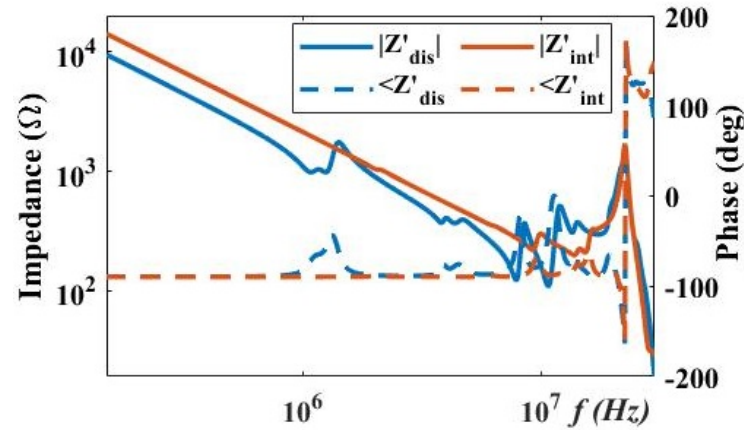
Figure 4.21: Impedance and phase profiles of Z'_{int} and Z'_{dis}.

4.4.4 Experimental Results

The analysis presented for the integrated transformer is validated experimentally using a single-phase DAB converter prototype. The experimental setup and operating conditions of the DAB converter prototype are the same as that shown in Figure 4.13 and Table 4.3, respectively. The primary voltage (v_p), secondary voltage (v_s) of the transformer, and inductor current i_L incorporating the integrated transformer are shown in Figure 4.19.

	k_1	k_2	k_3	d_1 (mm)	d_2 (mm)	d_3 (mm)	d (mm)	ϵ_r	z	r_o (mm)	r (mm)	C_{ps} (pF) estimated	C_{ps} (pF) measured
Discrete L_r	3.4	3.3	-	0.045	1.86	-	1.905	3.3	42	1	13.1	113.58	115
Integrated L_r	3.4	3.3	4.4	0.045	1	3.95	5	4.118	42	1	18	78.5	77

Table 4.6: Estimated and Measured C_{ps} with Discrete and Integral L_r

Impact of d on C_{ps} of the integrated transformer

The distance (d) between p and s windings of the conventional transformer is increased to design the integrated transformer with the desired leakage inductance of 618 μH, as given in Table 4.3. The top cross-sectional views of the conventional transformer and the integrated transformer are shown in Figures 4.20(a) and (b), respectively. As observed from Figure 4.20(b), the discrete L_r is integrated into the transformer by increasing the distance d using FR4 insulation of 3.95 mm thickness. Substituting the dielectric constants of the insulating layers and the thickness of the insulation mentioned in Table 4.6 in (4.22), the estimated C_{ps} of the transformer incorporated with the discrete L_r is 113.58 pF; while the measured C_{ps} is 115 pF, as given in Table 4.6. Similarly, the C_{ps} estimated for the transformer with integrated L_r is 78.5 pF; while the measured C_{ps} is 77 pF, as given in Table 4.6. Thus, from Table 4.6, it can be concluded that the C_{ps} reduces with an increase in the distance d between p and s windings; thus validating the analysis.

In addition, the impedance and phase profiles of Z'_{int} and Z'_{dis} is shown in Figure 4.21. It is observed from Figure 4.21 that, the Z'_{int} impedance is higher than the Z'_{dis} impedance, in particular for frequencies below 1.5 MHz, due to the reduction in C_{ps} capacitance with integrated L_r. Hence, the i_{cm} current with integrated L_r is less compared to discrete L_r, as shown in Figure 4.22.
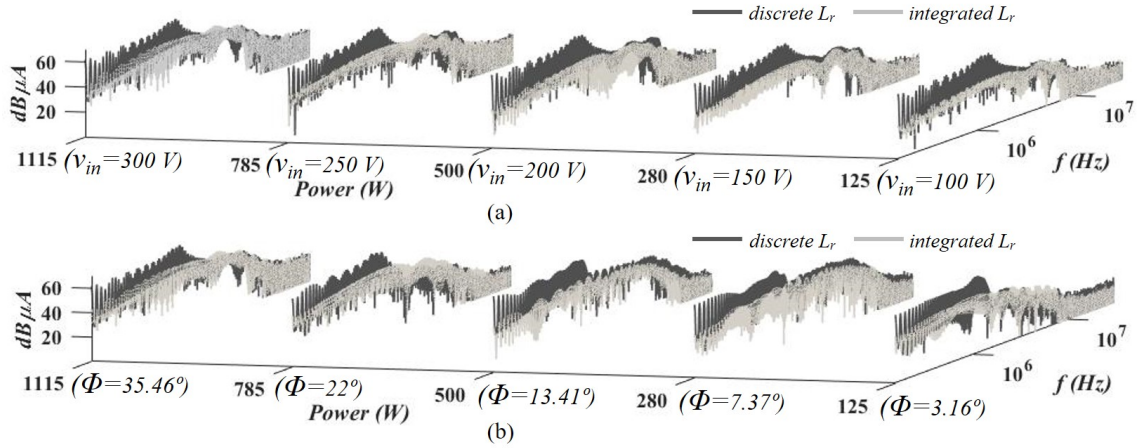
Figure 4.22: Frequency spectrum of i_{cm} current with discrete L_r (dark) and integrated L_r (light) for various (a) output voltages and (b) phase-shift, with SPST.

CM Noise with discrete and integrated L_r

The frequency spectra of i_{cm} measured at the dc input port with discrete and integrated L_r for various power levels are shown in Figure 4.22. It is observed from Figure 4.22 that integrating L_r into the transformer eliminates the undesired resonance at around 1.4 MHz and thus reduces the i_{cm} current. Moreover, it is
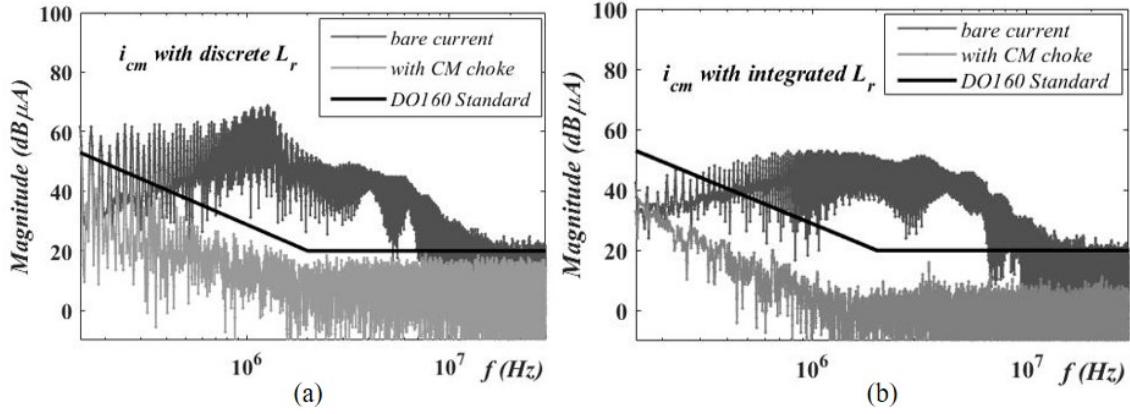
Figure 4.23: (a) Frequency spectrum of bare i_{cm} current with discrete L_r and with 3.5 mH conventional CM choke and (b) frequency spectrum of bare i_{cm} current with integrated transformer and with 1.75 mH conventional CM choke.

observed that with the discrete L_r, a CM choke of 3.5 mH attenuates the i_{cm} within the DO160 standard limit line, as evident from Figure 4.23(a); whereas with the integrated L_r, a CM choke of 1.75 mH is sufficient to attenuate i_{cm} within the standard, as evident from Figure 4.23(b). Thus, the input CM choke requirement for the DAB converter prototype is reduced by 50% with the integrated L_r. Therefore, the DAB converter with the integrated transformer gives better CM noise performance; thus validating the analysis.

4.5   Summary

The analysis of the CCMC is carried out with the help of the CM equivalent circuit. It is verified experimentally that, the input CM filtration techniques incorporated to reduce the total CM current in the DAB converter results in the CCMC. With the input CM choke, the CCMC propagates through the VSC1 and VSC2 ground parasitic capacitance via the ground. The voltage source of the CCMC constitutes the CM voltage sources of VSC1 and VSC2. Based on the analysis of the CCMC, the coupled inductor-based approach is incorporated to mitigate the CCMC along with providing the required inductance between VSC1 and VSC2 for the desired power transfer.

The experimental results prove that the designed concentric CM choke attenuates the CM noise of the DAB converter with a reduced box volume by 77.46% compared to the conventional CM choke. Hence, employing the concentric CM choke winding configuration instead of the conventional CM choke significantly reduces the volume occupied by the CM filter.

The CM noise analysis of the DAB converter with the magnetic tank incorporating an integrated transformer has been presented in detail.   The analysis and

experimental results prove that the magnetic tank with the discrete inductor results in unwanted resonances in the CM noise spectrum; while the magnetic tank with the integrated transformer has low CM noise. This is because, the increase in the distance between the primary and secondary windings, to achieve the desired leakage inductance, results in a reduction in the primary-to-secondary winding capacitance; thereby reducing the CM noise of the DAB converter. For the DAB converter prototype, the conventional CM choke requirement is reduced by 50% with the integrated transformer. Thus, incorporating the integrated transformer improves the CM noise performance of the DAB converter with reduced input CM filter requirement.

Chapter 5

DM Noise Mitigation Techniques With Integrated Magnetics

5.1   Introduction

To meet the higher inductance requirement without increasing the volume occupied by the inductor, this chapter presents toroidal inductor configurations namely concentric toroidal inductor (CTI) and concentric toroidal differential-mode choke (CTDMC). The CTI and CTDMC structures help in achieving higher inductances within the given box volume. The detailed analysis to estimate the inductances of CTI and CTDMC is presented along with the experimental validation.

5.2   Concentric Toroidal Inductor

The winding structure, analytical expression to estimate the inductance, and the experimental verification for the CTI configuration are further discussed. Additionally, the inductance comparison of CTI with the traditional inductor of the same volume is discussed in detail.

5.2.1   Analysis of CTI

The winding structure of the traditional inductor and the CTI are shown in Figures 5.1(a) and (b), respectively. As illustrated in Figure 5.1(b), the CTI consists of an outer core (C1) with N_1 turns and an inner core (C2) with N_2 turns. The magnetic equivalent circuits of C1, C2, and the CTI are shown in Figure 5.1(c)(i), (ii) and (iii), respectively.

The induced voltages on the windings of C1 and C2 are given by

$$V_1 = r_1 i + N_1 \frac{d\phi_1}{dt} = r_1 i + \left(L_{l1} + \frac{N_1^2}{2R_{C1}} \right) \frac{di}{dt} \tag{5.1}$$

$$V_2 = r_1 i + N_2 \frac{d\phi_2}{dt} = r_2 i + \left(L_{l2} + \frac{N_2^2}{2R_{C2}} \right) \frac{di}{dt} \tag{5.2}$$

where, r_1 and r_2 are the winding resistance of N_1 and N_2 turns, respectively; ϕ_1 and ϕ_2 are the flux in C1 and C2, respectively; L_{l1} and L_{l2} are the leakage inductances
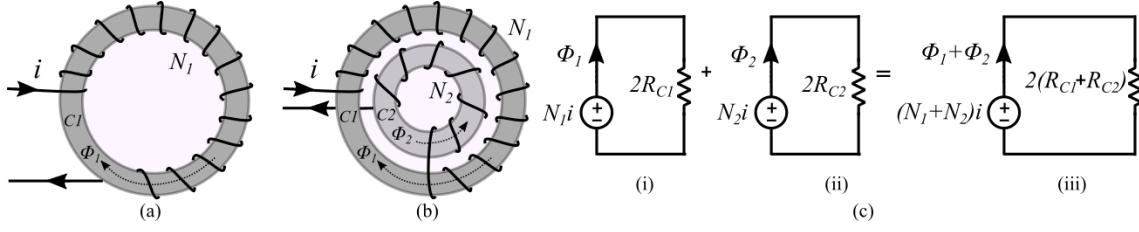
Figure 5.1: (a) Traditional inductor, (b) CTI, and (c) magnetic equivalent circuit of (i) outer core C1 (traditional inductor), (ii) inner core C2, and (iii) CTI.
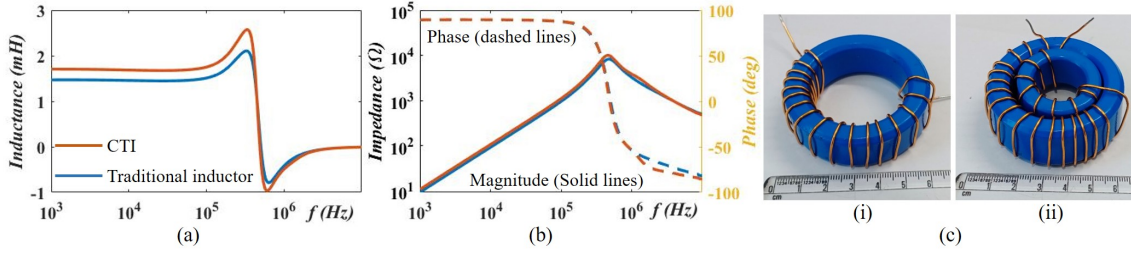
Figure 5.2: Traditional inductor (blue) and CTI (orange) (a) inductance profiles, (b) DM impedance profiles, and (c) (i) traditional inductor and (ii) CTI used for experimental validation.

of C1 and C2, respectively. R_{C1} and R_{C2} are half the reluctance of cores C1 and C2, respectively.

The induced voltage V_1 corresponds to the traditional inductor with N_1 turns wound on C1. Hence, the inductance of the traditional inductor is written from (5.1) as,

$$L_{conv} = L_{l1} + \frac{N_1^2}{2R_{C1}} \approx \frac{N_1^2}{2R_{C1}} \tag{5.3}$$

While the induced voltage corresponding to the CTI is the sum of V_1 and V_2, that is expressed using (5.1) and (5.2) as

$$V = (r_1 + r_2)i + (L_{l1} + L_{l2} + \frac{N_1^2}{2R_{C1}} + \frac{N_2^2}{2R_{C2}})\frac{di}{dt} \tag{5.4}$$

Thus, assuming negligible winding resistances (r_1, r_2) and the leakage inductances (L_{l1}, L_{l2}) in (5.4), the inductance offered by the CTI can be expressed as

$$L_{CTI} = L_{l1} + L_{l2} + \frac{N_1^2}{2R_{C1}} + \frac{N_2^2}{2R_{C2}} \approx \frac{N_1^2}{2R_{C1}} + \frac{N_2^2}{2R_{C2}} \tag{5.5}$$

Hence, from (5.3) and (5.5) it can be concluded that with the same volume, the CTI provides higher inductance compared to the traditional inductor. This increase in the inductance of CTI is further verified experimentally.

Table 5.1: Magnetic Properties of Cores

Core	OD (mm)	ID (mm)	H_T (mm)	μ_r	Reluctance
C1	58.90	40.56	18.87	4000	177481.9745
C2	36.50	22.85	14.82	2000	360230.5476

* OD is the outer diameter, ID is the inner diameter, and H_T is the height of the core.

Table 5.2: Estimated and Experimental L_{conv} and L_{CTI}

	N_1	N_2	Estimated	Experimental
L_{conv}	16	-	1.44 mH	1.45 mH
L_{CTI}	16	9	1.67 mH	1.69 mH

5.2.2 Experimental Validation of CTI

The CTI is built with two cores C1 and C2 of dimensions, relative permeability (μ_r), and reluctance mentioned in Table 5.1. The estimated value of L_{conv} from (5.3) with 16 turns wound on C1 is 1.44mH; while the experimentally measured inductance is 1.45mH, as shown in Figure 5.2(a). Similarly, the L_{CTI} for $N_1 = 16$ and $N_2 = 9$ on C1 and C2 cores, respectively, is estimated to be 1.67mH; while the experimentally measured value is 1.69mH, as shown in Figure 5.2(a). Hence, the L_{CTI} given by (5.5) accurately estimates the inductance of the CTI; and L_{CTI} is higher than L_{conv} by 240μH, as evident from Table 5.2. Due to higher L_{CTI} when compared to L_{conv}, the impedance offered by the CTI is higher than the traditional inductor, as shown in Figure 5.2(b). The traditional inductor and CTI employed for experimental validation are shown in Figure 5.2(c)(i) and (ii), respectively. Thus, the inductance of the proposed CTI configuration is higher than the traditional inductor with the same volume.

5.3 Concentric Toroidal DM Choke

The winding structure, analytical expression to estimate the inductance, and the experimental verification for the CTDMC configuration are further discussed. Additionally, the inductance comparison of CTDMC with the traditional inductor of the same volume is discussed in detail.

5.3.1 Analysis of CTDMC

The traditional DM choke and the CTDMC winding structures are shown in Figure 5.3(a) and (b), respectively. As evident from Figure 5.3(a), the inductance in the traditional DM choke is due to ϕ_1 and ϕ_4 in core C1; while the inductance of CTDMC
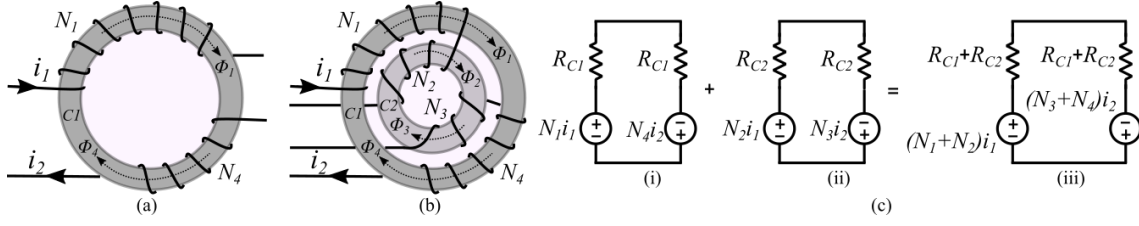
Figure 5.3: (a) Traditional DM choke, (b) CTDMC, and (c) magnetic circuit of (i) outer core C1 (traditional DM choke), (ii) inner core C2, and (iii) CTDMC.
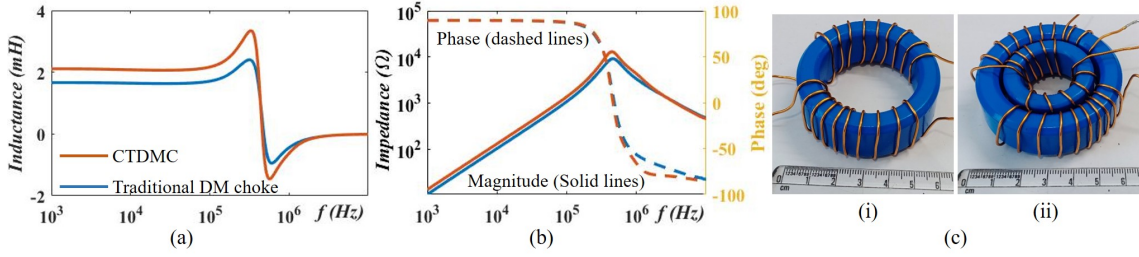
Figure 5.4: Traditional DM choke (blue) and CTDMC (orange) (a) inductance profiles, (b) DM impedance profiles, and (c) (i) traditional DM choke and (ii) CTDMC used for experimental validation.

is contributed by the flux ϕ_1 and ϕ_4 in core C1 along with the flux ϕ_2 and ϕ_3 in core C2. The magnetic equivalent circuits of C1, C2, and the CTDMC are shown in Figure 5.3(c)(i), (ii), and (iii), respectively. The flux ϕ_i $(i = 1, 2, 3, 4)$ due to winding of N_i $(i = 1, 2, 3, 4)$ turns is given by [95]

$$\phi_1 = \phi_{l1} + \phi_{m11} + \phi_{m14} = \phi_{l1} + \frac{N_1 i_1}{2R_{c1}} + \frac{N_4 i_2}{2R_{c1}}, \tag{5.6}$$

$$\phi_2 = \phi_{l2} + \phi_{m22} + \phi_{m23} = \phi_{l2} + \frac{N_2 i_1}{2R_{c2}} + \frac{N_3 i_2}{2R_{c2}}, \tag{5.7}$$

$$\phi_3 = \phi_{l3} + \phi_{m33} + \phi_{m32} = \phi_{l3} + \frac{N_3 i_2}{2R_{c2}} + \frac{N_2 i_1}{2R_{c2}}, \tag{5.8}$$

$$\phi_4 = \phi_{l4} + \phi_{m44} + \phi_{m41} = \phi_{l1} + \frac{N_4 i_2}{2R_{c1}} + \frac{N_1 i_1}{2R_{c1}}, \tag{5.9}$$

where ϕ_{li} is the leakage flux in winding with N_i turns, ϕ_{mij} is the mutual flux due to winding with N_i turns linking the winding with N_j turns; R_{C1} and R_{C2} are half the reluctance of cores C1 and C2, respectively.

The DM inductance of the traditional DM choke (L_{dm_conv}) is obtained by replacing N_1 by $(N_1 + N_4)$ in (5.3), as $i_1 = i_2 = i$ that flows through the $(N_1 + N_4)$ turns generate the total flux in C1. Hence, L_{dm_conv} is expressed as,

$$L_{dm\_conv} = L_{l1} + L_{l4} + \frac{(N_1 + N_4)^2}{2R_{C1}} \approx \frac{(N_1 + N_4)^2}{2R_{C1}}, \tag{5.10}$$

where L_{li} is the leakage inductance of the winding with N_i turns. Similarly, to obtain the DM inductance of CTDMC, initially, the voltage induced in winding with the

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} r_1 & 0 \\ 0 & r_2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} L_{l1} + L_{l2} + \frac{N_1^2}{2R_{C1}} + \frac{N_2^2}{2R_{C2}} & \frac{N_1 N_4}{2R_{C1}} + \frac{N_2 N_3}{2R_{C2}} \\ \frac{N_2 N_3}{2R_{C2}} + \frac{N_1 N_4}{2R_{C1}} & L_{l3} + L_{l4} + \frac{N_3^2}{2R_{C2}} + \frac{N_4^2}{2R_{C1}} \end{bmatrix} \begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \end{bmatrix}$$

i_1 and i_2 currents is written as in (5.11) [95]. The induced voltage ($V = V_1 + V_2$) due to the DM current in CTDMC is obtained by substituting $i_1 = i_2 = i$ in (5.11). Hence, V is written from (5.11) as,

$$V = i \sum_{i=1}^{4} r_i + \frac{di}{dt} \Big(\sum_{i=1}^{4} L_{li} + \frac{(N_1 + N_4)^2}{2R_{C1}} + \frac{(N_2 + N_3)^2}{2R_{C2}} \Big) \tag{5.11}$$

Thus, the DM inductance of CTDMC (L_{dm_CTDMC}), neglecting the leakage inductances, is written from (5.11) as,

$$L_{dm\_CTDMC} \approx \frac{(N_1 + N_4)^2}{2R_{C1}} + \frac{(N_2 + N_3)^2}{2R_{C2}} \tag{5.12}$$

Hence, from (5.10) and (5.12) it can be concluded that the proposed CTDMC provides higher inductance compared to the traditional DM choke of the same volume.

5.3.2   Experimental Validation of CTDMC

To validate the analysis, a traditional DM choke built with $N_1 = 9$ and $N_4 = 8$ turns wound on core C1 is chosen; while the CTDMC is built on cores C1 and C2 with the number of turns mentioned in Table 5.3. The L_{dm_conv} and L_{dm_CTDMC} estimated from (5.10) and (5.12) are 1.63mH and 2.1mH, respectively; while, the experimentally obtained L_{dm_conv} and L_{dm_CTDMC} are 1.66mH and 2.1mH, respectively, as shown in Figure 5.4(a). It is evident from Figure 5.3 that, the expression in (5.12) provides accurate estimation of L_{dm_CTDMC}; and the L_{dm_CTDMC} is greater than L_{dm_conv} by $440\mu H$. Due to the high L_{dm_CTDMC}, the impedance of L_{dm_CTDMC} is higher than the impedance offered by L_{dm_conv}, as evident from Figure 5.4(b). The traditional DM choke and the CTDMC used for experimental verification are shown in Figure 5.4(c)(i) and (ii), respectively. Thus, the experimental verification validates that the DM inductance of the proposed CTDMC is higher than the traditional DM choke of the same box volume.

5.4   Summary

The analytical expressions of the proposed CTI and CTDMC configurations are derived and validated experimentally. The theoretical analysis and the experimental

Table 5.3: Estimated and Experimental L_{dm_conv} and L_{dm_CTDMC}

	N_1	N_2	N_3	N_4	**Estimated**	**Experimental**
L_{dm_conv}	9	-	-	8	1.63 mH	1.66 mH
L_{dm_CTDMC}	9	5	5	9	2.1 mH	2.1 mH

results prove that the CTI and CTDMC provide higher inductance by 16.5% and 26.5% than the traditional inductor and the traditional DM choke, respectively, of the same volume. Hence, in the scenarios with the limitation in flexibility to increase the volume occupancy, the proposed CTI and CTDMC are preferred to achieve higher inductance values.

Chapter 6

Passive Integrated Chokes with Improved DM Inductance

6.1 Introduction

This chapter presents two integrated chokes, IC-1 and IC-2, by incorporating either ER cores or ER and I cores into the window area of the toroidal CM choke. Based on the CM and DM noise attenuation requirement, either the IC-1 or the IC-2 can be designed to reduce the PCB area and volume of the EMI filter. A similar core arrangement is utilized in [97], the winding structure does not fully utilize the ER core; thus limiting the achievable DM inductance. Thus, the proposed integrated chokes offer the following advantages.

1. The commercially available ER and I cores are utilized.

2. The adjustable air gap between the two ER cores or between the ER and I cores eliminates the risk of DM choke core saturation.

3. The winding structure of the proposed integrated chokes fully utilizes the cores, thus resulting in higher inductances.

The analytical approach to calculate the CM and DM inductance of the two proposed integrated chokes is presented with experimental validation. The CM and DM flux paths and magnetic core saturation analysis are presented using ANSYS simulations. The EMI filter volume reduction with the conventional CM and proposed integrated choke is verified on a SiC-DAB converter.

6.2 Design of Proposed Integrated Choke, IC-1

The core structural arrangement of one of the proposed integrated chokes, denoted by IC-1, is shown in Figure 6.1(a). The integrated choke IC-1 consists of an ER core inserted in the window area of the toroidal core. The electrical equivalence of IC-1 is as shown in Figure 6.1(b). The CM and DM inductance offered by IC-1 is denoted by $L_{cm(IC-1)}$ and $L_{dm(IC-1)}$. The winding arrangement on the toroidal
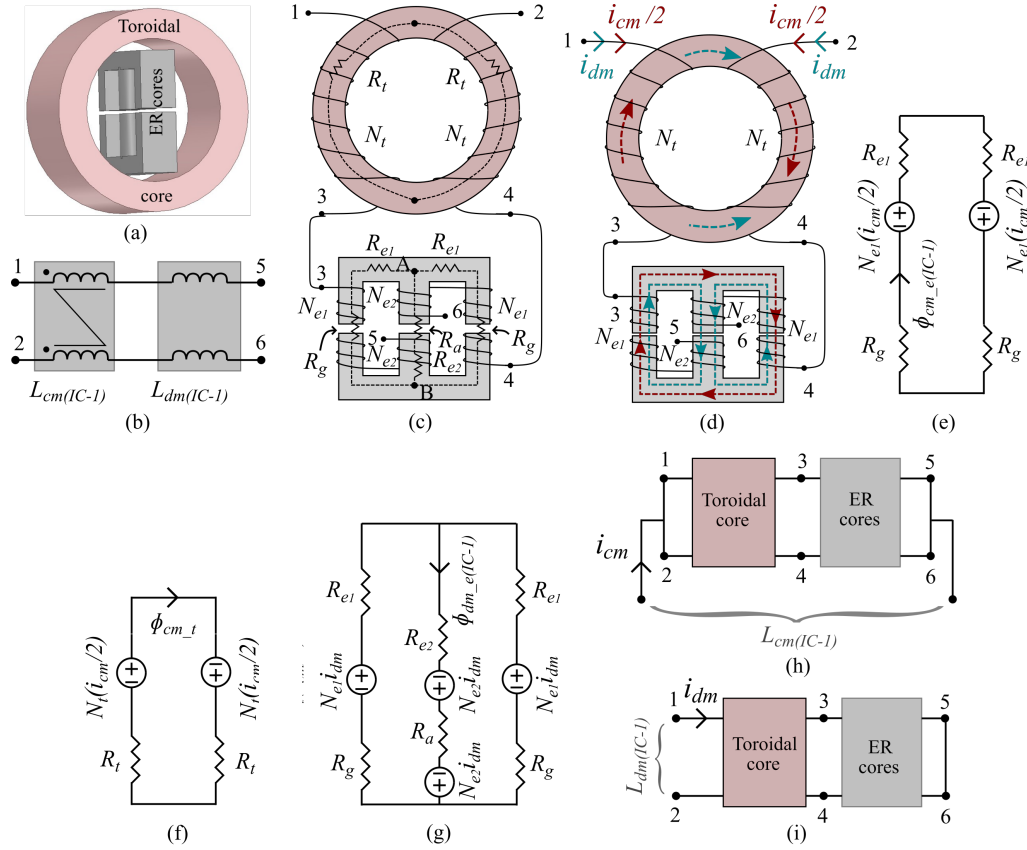
Figure 6.1: (a) Structural arrangement of IC-1, (b) electrical equivalence of IC-1, (c) winding arrangement in ER and toroidal cores of IC-1, (d) CM and DM flux distribution in the cores of IC-1, (e) magnetic equivalent circuit for i_{cm} current excitation in ER core of IC-1, (f) magnetic equivalent circuit for i_{cm} current excitation in the toroidal core of IC-1, (g) magnetic equivalent circuit with i_{dm} current excitation in ER core of IC-1, (h) winding terminal connections of IC-1 to measure the $L_{cm(IC-1)}$ inductance, and (i) winding terminal connections of IC-1 to measure the $L_{dm(IC-1)}$ inductance.

and the ER cores of IC-1 is shown in Figure 6.1(c). In Figure 6.1(c), N_{e1} and N_{e2} denote the number of turns on the outer limb and the center limbs of the ER core, respectively; N_t denotes half the number of turns on the toroidal core; R_{e1} and R_{e2} are the reluctance of the outer and center limbs of the ER core, respectively; R_a and R_g denote the air gap reluctance of the outer and center limbs of the ER core, respectively; R_t denotes half the reluctance of the toroidal core. The reluctance in k^{th} section (R_k) can be obtained from [69]

$$R_k = \frac{l_k}{\mu_o \mu_{rk} A_k}, \tag{6.1}$$

where l_k, A_k, and μ_{rk} are the mean magnetic path length, cross-sectional area, and relative permeability corresponding to k^{th} section respectively; μ_o is the relative permeability of free space. The theoretical estimation of $L_{cm(IC-1)}$ and $L_{dm(IC-1)}$ inductance of the proposed integrated choke is discussed further.

6.2.1 Estimation of $L_{cm(IC-1)}$ Inductance

The flux generated in the toroidal and ER cores with the CM current (i_{cm}) excitation is shown in Figure 6.1(d). The corresponding magnetic equivalent circuit of the ER core with the i_{cm} current excitation is shown in Figure 6.1(e). As indicated in Figure 6.1(e), the flux due to the i_{cm} current in the ER core, $\phi_{cm\_e(IC-1)}$, is given by

$$\phi_{cm\_e(IC-1)} = \frac{N_{e1}i_{cm}}{2(R_{e1} + R_a)}. \tag{6.2}$$

Therefore, the CM inductance offered by the ER core, $L_{cm\_e(IC-1)}$, can be written as

$$L_{cm\_e(IC-1)} = \frac{N_{e1}^2}{2(R_{e1} + R_g)}. \tag{6.3}$$

Similarly, the flux generated by the i_{cm} current in the toroidal core, ϕ_{cm_t}, is shown in Figure 6.1(d). The corresponding magnetic equivalent circuit of the toroidal core with the i_{cm} current excitation is shown in Figure 6.1(f). Thus, the CM inductance, L_{cm_t}, due to the ϕ_{cm_t} flux in the toroidal core can be written as [69]

$$L_{cm\_t} = \frac{N_t^2}{2R_t}. \tag{6.4}$$

Thus, the total CM inductance offered by IC-1, $L_{cm(IC-1)}$, is the sum of the CM inductance offered by the ER and the toroidal core. Thus, the $L_{cm(IC-1)}$ inductance of IC-1, is obtained from (6.3) and (6.4) as

$$L_{cm(IC-1)} = L_{cm\_e(IC-1)} + L_{cm\_t} = \frac{N_{e1}^2}{2(R_{e1} + R_g)} + \frac{N_t^2}{2R_t}. \tag{6.5}$$

To experimentally measure the $L_{cm(IC-1)}$ inductance, the winding terminal connections of $IC-1$ are shown in Figure 6.1(h).

6.2.2 Estimation of $L_{dm(IC-1)}$ Inductance

The flux generated in the toroidal and ER cores with the DM current (i_{dm}) excitation is shown in Figure 6.1(d). The magnetic equivalent circuit of the ER cores with the i_{dm} current excitation is shown in Figure 6.1(g). As indicated in Figure 6.1(g), the flux due to the i_{dm} current in the ER core, $\phi_{dm\_e(IC-1)}$, is given by

$$\phi_{dm\_e(IC-1)} = \frac{(2N_{e1} + 4N_{e2})i_{dm}}{R_{e1} + 2R_{e2} + 2R_a + R_g}. \tag{6.6}$$

Therefore, the DM inductance offered by the ER core, $L_{dm\_e(IC-1)}$, can be written as

$$L_{dm\_e(IC-1)} = \frac{2(N_{e1} + 2N_{e2})^2}{R_{e1} + 2R_{e2} + 2R_a + R_g}. \tag{6.7}$$

Similarly, the flux generated in the toroidal core with the i_{dm} current excitation results in the DM inductance, L_{dm_t}, given by

$$L_{dm\_t} = \frac{\mu_o \mu_{dm\_eff} A_t N_t^2}{l_{eff}}. \tag{6.8}$$

where, A_t, μ_{dm_eff}, and l_{eff} are the cross-sectional area of the toroidal core, effective DM permeability, and the effective mean magnetic length, respectively. The l_{eff} is expressed in terms of the outer diameter (OD), inner diameter (ID) and angle covered by each winding (θ) as [69]

$$l_{eff} = \sqrt{\frac{OD^2}{\sqrt{2}}\left(\frac{\theta}{4} + 1 + sin\frac{\theta}{2}\right)^2 + ID^2\left(\frac{\theta}{4} - 1 + sin\frac{\theta}{2}\right)^2}. \tag{6.9}$$

Thus, the total DM inductance, $L_{dm(IC-1)}$, offered by the proposed integrated choke IC-1 is given from (6.7) and (6.8) as

$$\begin{aligned} L_{dm(IC-1)} &= L_{dm\_e(IC-1)} + L_{dm\_t} \\ &= \frac{2(N_{e1} + 2N_{e2})^2}{R_{e1} + 2R_{e2} + 2R_a + R_g} + \frac{\mu_o \mu_{dm\_eff} A_t N_t^2}{l_{eff}}. \end{aligned} \tag{6.10}$$

The winding terminal connections of $IC-1$ to experimentally measure the $L_{dm(IC-1)}$ inductance is shown in Figure 6.1(i). Further, the CM and DM flux distribution of IC-1 is validated from ANSYS 3D Maxwell simulations.

6.2.3 Magnetic Flux Density and Saturation Analysis of IC-1

The net flux generated by the i_{cm} and i_{dm} currents in various sections of the ER core is shown in Figure 6.2(a). From Figure 6.1(c), the resultant flux in the ith section, $\phi_{i(IC-1)}$, $i = 1, 2, 3$, is given by

$$\phi_{i(IC-1)} = \begin{cases} \frac{\phi_{dm\_e(IC-1)}}{2} + \phi_{cm\_e(IC-1)}, & \text{i=\{1,2\}} \\ \phi_{dm\_t} + \phi_{dm\_e(IC-1)}, & \text{i=3} \end{cases} \tag{6.11}$$
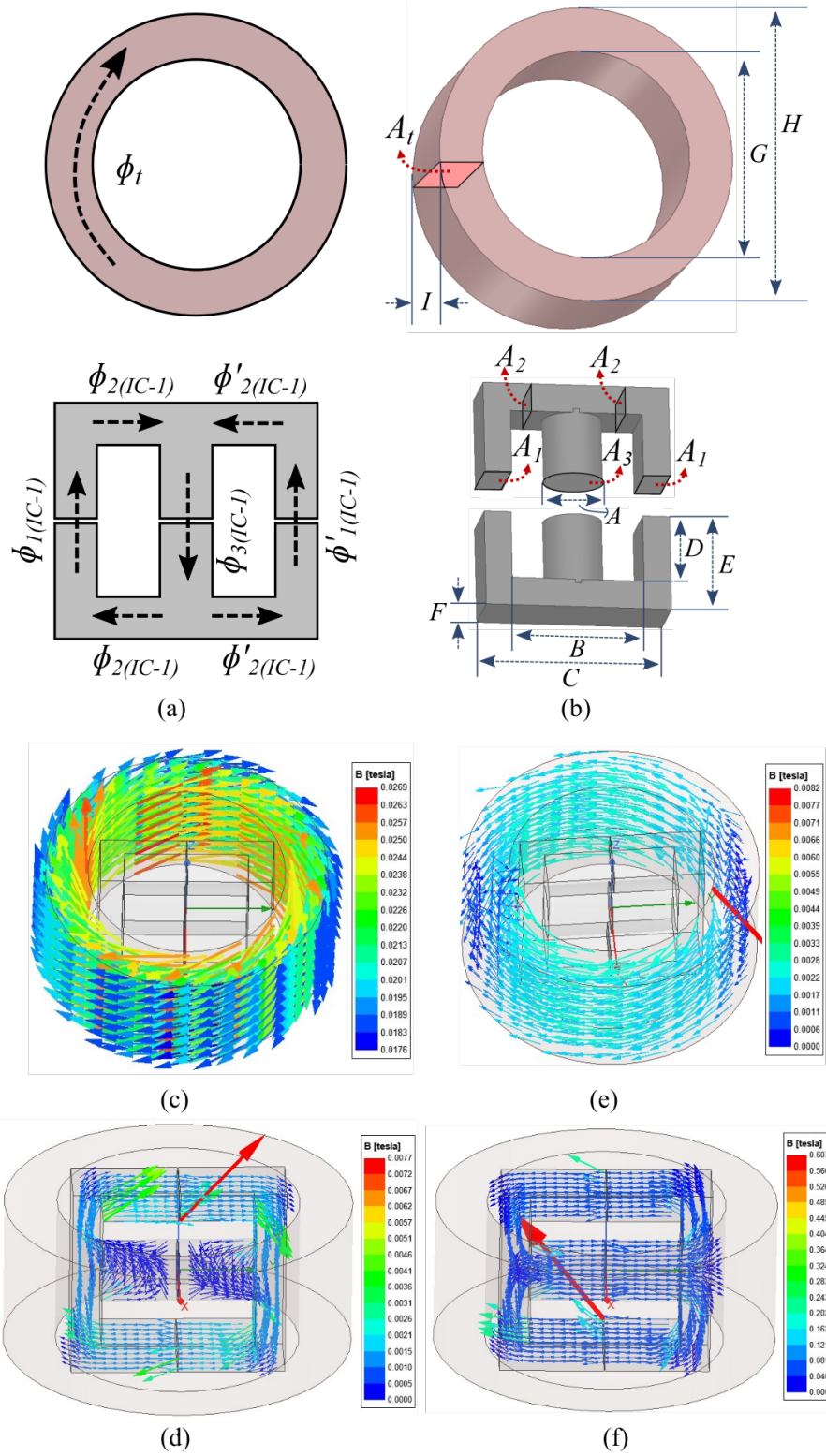
Figure 6.2: (a) Resultant flux in the toroidal and ER cores of IC -1, (b) dimensions of the toroidal and ER cores of IC-1, (c) CM flux distribution in the toroidal core, (d) CM flux distribution in the ER cores, (e) DM flux distribution in the toroidal core, and (f) DM flux distribution in the ER cores.

Similarly, the resultant flux $\phi'_{i(IC-1)}$, $i = \{1, 2\}$, is given by

$$\phi'_{1(IC-1)} = \phi'_{2(IC-1)} = \frac{\phi_{dm\_e(IC-1)}}{2} - \phi_{cm\_e(IC-1)}. \tag{6.12}$$

As evident from Figures 6.2(a) and (b), the $\phi_{1(IC-1)}$ and $\phi'_{1(IC-1)}$ flux flows through the area of cross-section A_1. In addition, $\phi_{2(IC-1)}$ and $\phi'_{2(IC-1)}$ flux flows through the area of cross-section A_2. Hence, from (6.11) and (6.12), the $\phi_{1(IC-1)}$ and $\phi_{2(IC-1)}$ results in higher magnetic flux density than $\phi'_{1(IC-1)}$ and $\phi'_{2(IC-1)}$, respectively. Thus, the magnetic flux density $B_{1(IC-1)}$, $B_{2(IC-1)}$, and $B_{3(IC-1)}$ corresponding to $\phi_{1(IC-1)}$, $\phi_{2(IC-1)}$, and $\phi_{3(IC-1)}$, respectively, can be expressed as

$$
\begin{aligned}
B_{1(IC-1)} =& \frac{\phi_{1(IC-1)}}{A_1} \\
=& \frac{1}{A_1} \left(\frac{L_{cm\_e(IC-1)} i_{cm}}{N_{e1}} + \frac{L_{dm\_e(IC-1)} i_{dm}}{2(N_{e1} + 2N_{e2})} \right),
\end{aligned} \tag{6.13}
$$

$$
\begin{aligned}
B_{2(IC-1)} =& \frac{\phi_{2(IC-1)}}{A_2} \\
=& \frac{1}{A_2} \left(\frac{L_{cm\_e(IC-1)} i_{cm}}{N_{e1}} + \frac{L_{dm\_e(IC-1)} i_{dm}}{2(N_{e1} + 2N_{e2})} \right),
\end{aligned} \tag{6.14}
$$

$$
\begin{aligned}
B_{3(IC-1)} =& \frac{\phi_{3(IC-1)}}{A_3} \\
=& \frac{1}{A_3} \left(\frac{L_{dm\_e(IC-1)} i_{dm}}{(N_{e1} + 2N_{e2})} + \frac{L_{dm\_t} i_{dm}}{N_t} \right),
\end{aligned} \tag{6.15}
$$

were A_1, A_2, and A_3 are the cross-sectional area, as shown in Figure 6.2(b). Thus, the maximum flux density in the ER core, $B_{max\_e(IC-1)}$, is given by

$$B_{max\_e(IC-1)} = max\{B_{1(IC-1)}, B_{2(IC-1)}, B_{3(IC-1)}\}. \tag{6.16}$$

Similarly, the resultant flux in the toroidal core is given by

$$\phi_t = \phi_{cm\_t} + \frac{\phi_{dm\_t}}{2}. \tag{6.17}$$

Thus, the maximum flux density in the toroidal core is given as

$$B_{max\_t} = \frac{1}{A_t N_t} \left(L_{cm\_t} i_{cm} + \frac{L_{dm\_t} i_{dm}}{2} \right). \tag{6.18}$$

Hence, to avoid saturation in ER and the toroidal cores, the $B_{max\_e(IC-1)}$ and B_{max_t} should be less than the saturation flux density, B_{sat}, of the respective cores. To analyze the flux distribution in the toroidal and ER cores of IC-1, the IC-1 is simulated in ANSYS 3D Maxwell. The resultant flux in the toroidal and ER cores with the i_{cm} and i_{dm} current excitation is shown in Figure 6.2(a). The dimensions

A, B, C, D, E, F, G, H, and I in Figure 6.2(b) are 9.4 mm, 21.34 mm, 30 mm, 11.58 mm, 16.18 mm, 9.5 mm, 37 mm, 53 mm, and 23.05 mm, respectively.

The CM flux generated in the toroidal and ER cores with the i_{cm} current of 300 mA is shown in Figures 6.2(c) and (d), respectively. As observed from Figure 6.2(d), the CM flux in the ER core flows through the outer limbs with i_{cm} current excitation, thus validating the magnetic equivalent circuit shown in Figure 6.1(e). Similarly, the DM flux generated in the toroidal and ER cores with the i_{dm} current of 4 A is shown in Figures 6.2(e) and (f), respectively. As observed from Figure 6.2(f), the DM flux path in the ER core is through the center limb with i_{dm} current excitation, thus validating the magnetic equivalent circuit shown in Figure 6.1(g). It is to be noted that, to reduce the simulation burden, the following turns are considered in the ANSYS simulation N_t =1, N_{e1} =1 and N_{e2}=1. However, with N_t =35, N_{e1} =11, and N_{e2}=8 turns, the maximum flux density in the toroidal core is obtained as 1 T, which is less than the B_{sat} = 1.2 T for nanocrystalline core material [3]. Similarly, from Figures 6.2(d) and (f), for the above-mentioned N_t, N_{e1}, and N_{e2} turns, the maximum flux density in the ER cores is obtained as 0.38 T, which is less than the B_{sat} = 0.5 T for ferrite core material [3].

Thus, the following inferences can be made for IC-1.

1. The toroidal core majorly contributes to the CM inductance of the IC-1, therefore the $L_{cm\_e(IC-1)}$ component dominates in the $L_{cm(IC-1)}$ inductance. Hence, the maximum magnetic flux density in the toroidal core is depicted by the CM flux in the core.

2. The combined toroidal and ER cores contribute to the $L_{dm(IC-1)}$ inductance.

6.3   Design of the Integrated Choke, IC-2

For the CM choke with a lesser inner diameter, one-half of the ER core is replaced by the I core, as shown in Figure 6.3(a). The integrated choke IC-2 consists of the combined ER and I core inserted in the window area of the toroidal core. The electrical equivalence of IC-2 is as shown in Figure 6.3(b). The CM and DM inductance offered by IC-2 is denoted by $L_{cm(IC-2)}$ and $L_{dm(IC-2)}$, as shown in Figure 6.3(b). The winding arrangement on the toroidal and the ER cores of IC-2 is shown in Figure 6.3(c). In Figure 6.3(c), N_{e1} and N_{e2} denote the number of turns on the outer limb and the center limbs of the ER core, respectively; N_t denotes half the number of turns on the toroidal core; R_{e1} and R_{e2} are the reluctance of the outer and center limbs of the ER core, respectively; R_a and R_g denote the air gap reluctance of the outer and center limbs of the ER core, respectively; R_t denotes half
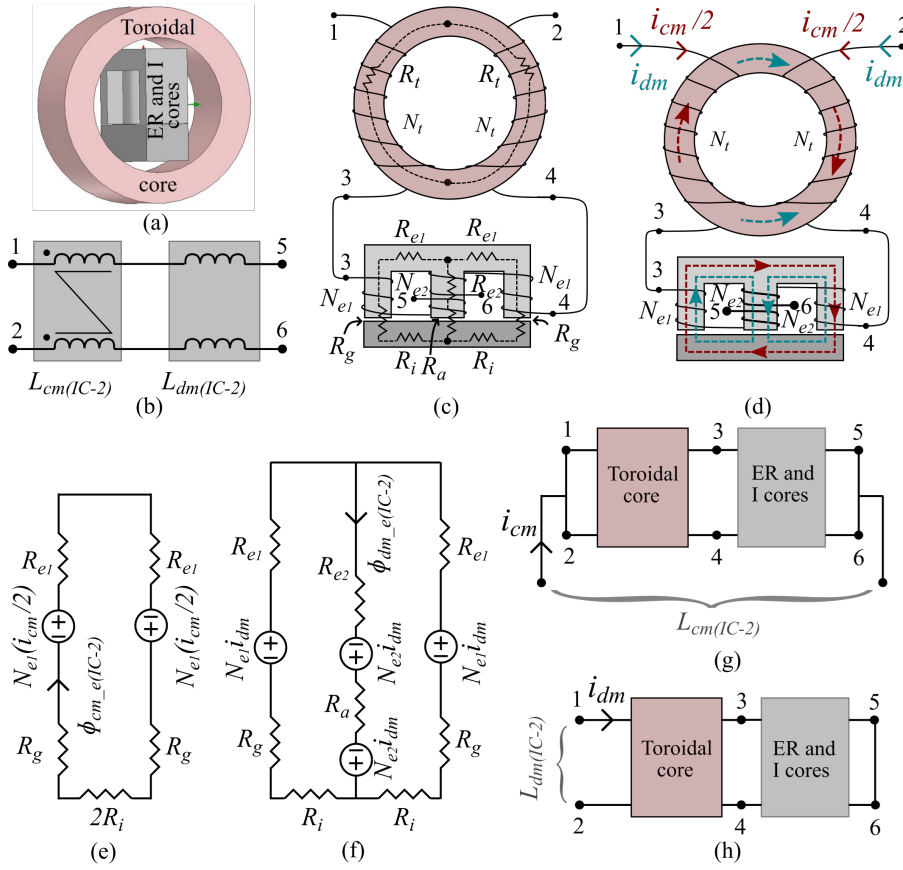
Figure 6.3: (a) Structural arrangement of IC-2, (b) electrical equivalence of IC-2, (c) winding arrangement in toroidal, ER, and I cores of IC-2, (d) CM and DM flux distribution in the cores of IC-2, (e) magnetic equivalent circuit for i_{cm} current excitation of ER and I cores of IC-2, (f) magnetic equivalent circuit for i_{dm} current excitation in ER and I cores of IC-2, (g) winding terminal connections of IC-2 to measure the $L_{cm(IC-2)}$ inductance, and (h) winding terminal connections of IC-2 to measure the $L_{dm(IC-2)}$ inductance.

the reluctance of the toroidal core. The reluctance of each section can be obtained from (6.1).

The theoretical estimation of $L_{cm(IC-2)}$ and $L_{dm(IC-2)}$ inductance of the proposed integrated choke is presented below. In addition, the flux distribution of IC-2 is validated using ANSYS simulations in detail.

6.3.1 Estimation of $L_{cm(IC-2)}$ Inductance

The flux generated in the toroidal, ER, and I core with the i_{cm} excitation is shown in Figure 6.3(d). The corresponding magnetic circuit of the ER and I cores with the i_{cm} current excitation is shown in Figure 6.3(e). In Figure 6.3(e), the R_i denotes half the reluctance of the I core. As indicated in Figure 6.3(e), the flux due to the i_{cm} current in the ER and I cores, $\phi_{cm\_e(IC-2)}$, is given by

$$\phi_{cm\_e(IC-2)} = \frac{N_{e1}i_{cm}}{2(R_{e1} + R_i + R_a)}. \tag{6.19}$$

Therefore, the CM inductance offered by the combined ER and I cores, $L_{cm\_e(IC-2)}$, can be written as

$$L_{cm\_e(IC-2)} = \frac{N_{e1}^2}{2(R_{e1} + R_i + R_g)}. \tag{6.20}$$

Similarly, the CM inductance offered by the toroidal core with the i_{cm} current is given by (6.4). Thus, the total CM inductance offered by IC-2, $L_{cm(IC-2)}$, is the sum of the CM inductance offered by the combined ER and I cores, and the toroidal core. Thus, $L_{cm(IC-2)}$ inductance is obtained from (6.20) and (6.4) as

$$L_{cm(IC-2)} = L_{cm\_e(IC-2)} + L_{cm\_t}$$
$$= \frac{N_{e1}^2}{2(R_{e1} + R_i + R_g)} + \frac{N_t^2}{2R_t}. \tag{6.21}$$

The winding terminal connections of IC-2 to experimentally measure the $L_{cm(IC-2)}$ inductance are shown in Figure 6.3(g).

6.3.2 Estimation of $L_{dm(IC-2)}$ Inductance

The flux generated in the toroidal, ER, and I core with the i_{dm} excitation is shown in Figure 6.3(d). The magnetic circuit of the combined ER and I cores with the i_{dm} current excitation is shown in Figure 6.3(f). As indicated in Figure 6.3(f), the flux due to the i_{dm} current in the ER and I cores, $\phi_{dm\_e((IC-2)}$, is given by

$$\phi_{dm\_e(IC-2)} = \frac{(2N_{e1} + 4N_{e2})i_{dm}}{R_{e1} + 2R_{e2} + 2R_a + R_g + R_i}. \tag{6.22}$$

Therefore, the DM inductance offered by the combined ER and I cores can be written as

$$L_{dm\_e(IC-2)} = \frac{2(N_{e1} + 2N_{e2})^2}{R_{e1} + 2R_{e2} + 2R_a + R_g + R_i}. \tag{6.23}$$

Similarly, the DM inductance offered by the toroidal core with the i_{dm} current excitation is given by (6.8). Thus, the total DM inductance, $L_{dm(IC-2)}$, offered by the proposed choke IC-2 is given from (6.8) and (6.23) as

$$L_{dm(IC-2)} = L_{dm\_e(IC-2)} + L_{dm\_t}$$
$$= \frac{2(N_{e1} + 2N_{e2})^2}{R_{e1} + 2R_{e2} + 2R_a + R_g + R_i} + \frac{\mu_o \mu_{dm\_eff} A_t N_t^2}{l_{eff}}. \tag{6.24}$$

The winding terminal connections of IC-2 to experimentally measure the $L_{dm(IC-2)}$ inductance are shown in Figure 6.3(h). Further, the CM and DM flux distribution

of IC-2 is validated from ANSYS 3D Maxwell simulations.

6.3.3 Magnetic Flux Density and Saturation Analysis of IC-2

The net flux generated by the i_{cm} and i_{dm} currents in various sections of the toroidal, ER, and I core is shown in Figure 6.4(a). From Figure 6.3(c), the resultant flux in the ith section, $\phi_{i(IC-2)}$, $i = 1, 2, 3$, is given by

$$\phi_{i(IC-2)} = \begin{cases} \frac{\phi_{dm\_e(IC-2)}}{2} + \phi_{cm\_e(IC-2)}, & \text{i=\{1,2\}} \\ \phi_{dm\_t} + \phi_{dm\_e(IC-2)}, & \text{i=3} \end{cases} \tag{6.25}$$

Similarly, the resultant flux $\phi'_{i(IC-2)}$, $i = \{1, 2\}$, is given by

$$\phi'_{1(IC-2)} = \phi'_{2(IC-2)} = \frac{\phi_{dm\_e(IC-2)}}{2} - \phi_{cm\_e(IC-2)}. \tag{6.26}$$

As evident from Figures 6.4(a) and (b), the $\phi_{1(IC-2)}$ and $\phi'_{1(IC-2)}$ flux flows through the area of cross-section A_1. In addition, $\phi_{2(IC-2)}$ and $\phi'_{2(IC-2)}$ flux flows through the area of cross-section A_2. Hence, from (6.25) and (6.26), the $\phi_{1(IC-2)}$ and $\phi_{2(IC-2)}$ results in higher magnetic flux density than $\phi'_{1(IC-2)}$ and $\phi'_{2(IC-2)}$, respectively. Thus, the magnetic flux density $B_{1(IC-2)}$, $B_{2(IC-2)}$, and $B_{3(IC-2)}$ corresponding to $\phi_{1(IC-2)}$, $\phi_{2(IC-2)}$, and $\phi_{3(IC-2)}$, respectively, can be expressed as

$$B_{1(IC-2)} = \frac{\phi_{1(IC-2)}}{A_1}$$
$$= \frac{1}{A_1} \left(\frac{L_{cm\_e(IC-2)} i_{cm}}{N_{e1}} + \frac{L_{dm\_e(IC-2)} i_{dm}}{2(N_{e1} + 2N_{e2})} \right), \tag{6.27}$$

$$B_{2(IC-2)} = \frac{\phi_{2(IC-2)}}{A_2}$$
$$= \frac{1}{A_3} \left(\frac{L_{cm\_e(IC-2)} i_{cm}}{N_{e1}} + \frac{L_{dm\_e(IC-2)} i_{dm}}{2(N_{e1} + 2N_{e2})} \right), \tag{6.28}$$

$$B_{3(IC-2)} = \frac{\phi_{3(IC-2)}}{A_3}$$
$$= \frac{1}{A_3} \left(\frac{L_{dm\_e(IC-2)} i_{dm}}{(N_{e1} + 2N_{e2})} + \frac{L_{dm\_t} i_{dm}}{N_t} \right), \tag{6.29}$$

where A_1, A_2, and A_3 are the cross-sectional area, as shown in Figure 6.4(b). Thus, the maximum flux density in the ER core, $B_{max\_e(IC-2)}$, is given by

$$B_{max\_e(IC-2)} = max\{B_{1(IC-2)}, B_{2(IC-2)}, B_{3(IC-2)}\}. \tag{6.30}$$
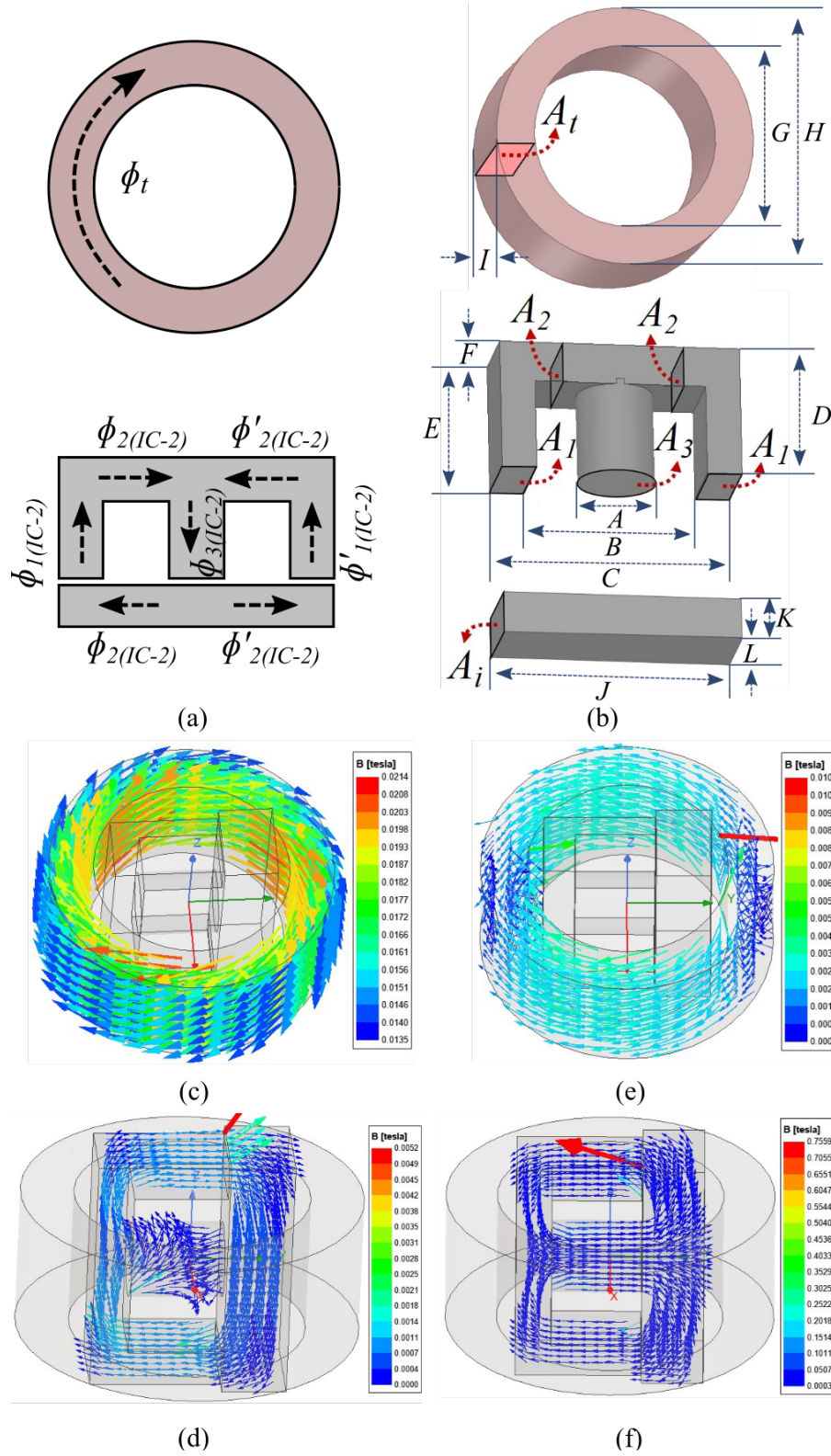
Figure 6.4: (a) Resultant flux in toroidal, ER, and I cores, (b) dimensions of toroidal, ER and I cores, (c) CM flux distribution in the toroidal core, (d) CM flux distribution in the ER and I cores, (e) DM flux distribution in the toroidal core, and (f) DM flux distribution in the ER and I cores.

Similarly, the maximum flux density in the I core is expressed as

$$B_{max\_i(IC-2)} = \frac{\phi_{2(IC-2)}}{A_i} \tag{6.31}$$

$$= \frac{1}{A_i} \left(\frac{L_{cm\_e(IC-2)} i_{cm}}{N_{e1}} + \frac{L_{dm\_e(IC-2)} i_{dm}}{2(N_{e1} + 2N_{e2})} \right), \tag{6.32}$$

where A_i is the cross-sectional area of the I core, as shown in Figure 6.4(b). The maximum flux density in the toroidal core remains the same as given in (6.18). Hence, to avoid saturation in ER, I, and the toroidal cores, the $B_{max\_e(IC-2)}$, $B_{max\_i(IC-2)}$, and B_{max_t} should be less than the saturation flux density, B_{sat}, of the respective cores.

To analyze the flux distribution in the toroidal, ER and I cores of IC-2, the IC-2 is simulated in ANSYS 3D Maxwell. The resultant flux in the toroidal ER and I cores is as given in Figure 6.4(a). The dimensions A, B, C, D, E, F, G, H, I, J, K, and L indicated in Figure 6.4(b) are considered as 9.4 mm, 21.34 mm, 30 mm, 11.58 mm, 16.18 mm, 9.5 mm, 29.35 mm, 42.60 mm, 17.80 mm, 31 mm, and 8 mm, and 11.60 mm respectively. The CM flux generated in the toroidal ER and I cores with the i_{cm} current of 200 mA is shown in Figures 6.4(c) and (d), respectively. As observed from Figure 6.4(d), the CM flux in the ER flows through the outer limbs with i_{cm} current excitation, thus validating the magnetic equivalent circuit shown in Figure 6.3(e). In the same way, the DM flux generated in the toroidal ER and I cores with the i_{dm} current of 3.5 A is shown in Figures 6.4(e) and (f), respectively. As observed from Figure 6.4(f), the DM flux in the ER core flows through the center limb with i_{dm} current excitation, thus validating the magnetic equivalent circuit shown in Figure 6.1(f). It is to be noted that, to reduce the simulation burden, the following turns are considered in the ANSYS simulation $N_t = 1$, $N_{e1} = 1$ and $N_{e2} = 1$. However, for $N_t = 25$, $N_{e1} = 10$, and $N_{e2} = 4$ turns, the maximum flux density in the toroidal core is obtained as 0.5 T, which is less than the $B_{sat} = 1.2$ T for nanocrystalline core material [3]. Similarly, from Figures 6.4(d) and (f), for the above-mentioned N_t, N_{e1}, and N_{e2} turns, the maximum flux density in the ER and I cores is obtained as 0.4 T, which is less than the $B_{sat} = 0.5$ T for ferrite core material [3].

Thus, the following inferences can be made on IC-2.

1. The toroidal core majorly contributes to the CM inductance of the IC-2, therefore the $L_{cm\_e(IC-2)}$ component dominates in the $L_{cm(IC-2))}$ inductance. Hence, the maximum magnetic flux density in the toroidal core is depicted by the CM flux in the core.
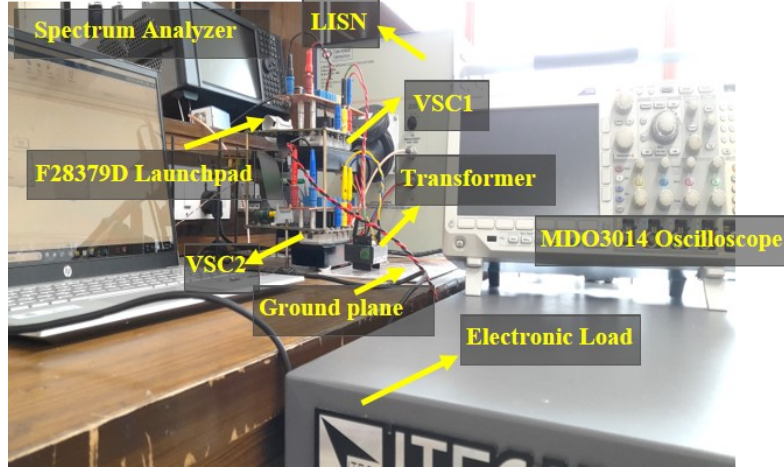
Figure 6.5: Experimental setup of the DAB converter.

2. The combined toroidal, ER, and I cores contribute to the $L_{dm(IC-2)}$ inductance.

Table 6.1: Conventional CM and DM Choke Details

EMI	CM choke			DM choke		
filter	L_{cm}	Core	N*	L_{dm}	Core	N*
EMI Filter-I	23.3 mH (1 No.)	T60006-L2 050-W565	35	100 μH (2 No.)	S130060 215943	42
EMI Filter-II	6.3 mH (1 No.)	T60006-L2 040-W452	25	50 μH (2 No.)	HJS106026 215174	34

* N denotes the number of turns.

6.4 Experimental Verification of IC-1 and IC-2

The presented integrated chokes IC-1 and IC-2 are validated experimentally on a single-phase isolated DAB converter. The experimental setup of the DAB converter is shown in Figure 6.5. The DAB converter is operated with the SPST at a switching frequency of 50 kHz. The LISN (LI-3P-232) is connected at the DC input port to decouple the noise of the main supply and the DAB converter. The i_{cm} and i_{dm} currents of the DAB converter are measured using a high bandwidth current probe (TCP202A).

To validate the performance of IC-1 and IC-2, the DAB converter is operated at 1 kW (DC voltages and currents of 250 V and 4 A, respectively) and 0.5 kW (DC voltages and currents of 150 V and 3.5 A, respectively). The bare i_{cm} and i_{dm} currents for the output power of 1 kW are shown in green in Figures. 6.6(a) and (b), respectively. Similarly, the bare i_{cm} and i_{dm} currents at the output power of 0.5 kW are shown in

Choke	N_e	N_t	R_{e1} (H^{-1})	R_{e2} (H^{-1})	R_a (H^{-1})	R_g (H^{-1})	R_i (H^{-1})	$2R_t$ (H^{-1})
IC-1	$N_{e1} = 11$, $N_{e2} = 8$	35	1004478.8	318320.06	1605360.538	2708361.74	-	50300.53
IC-2	$N_{e1} = 10$, $N_{e2} = 4$	25	502239.4	159160.03	1605360.54	2708361.74	439806.69	50253.29

Table 6.2: Core Properties
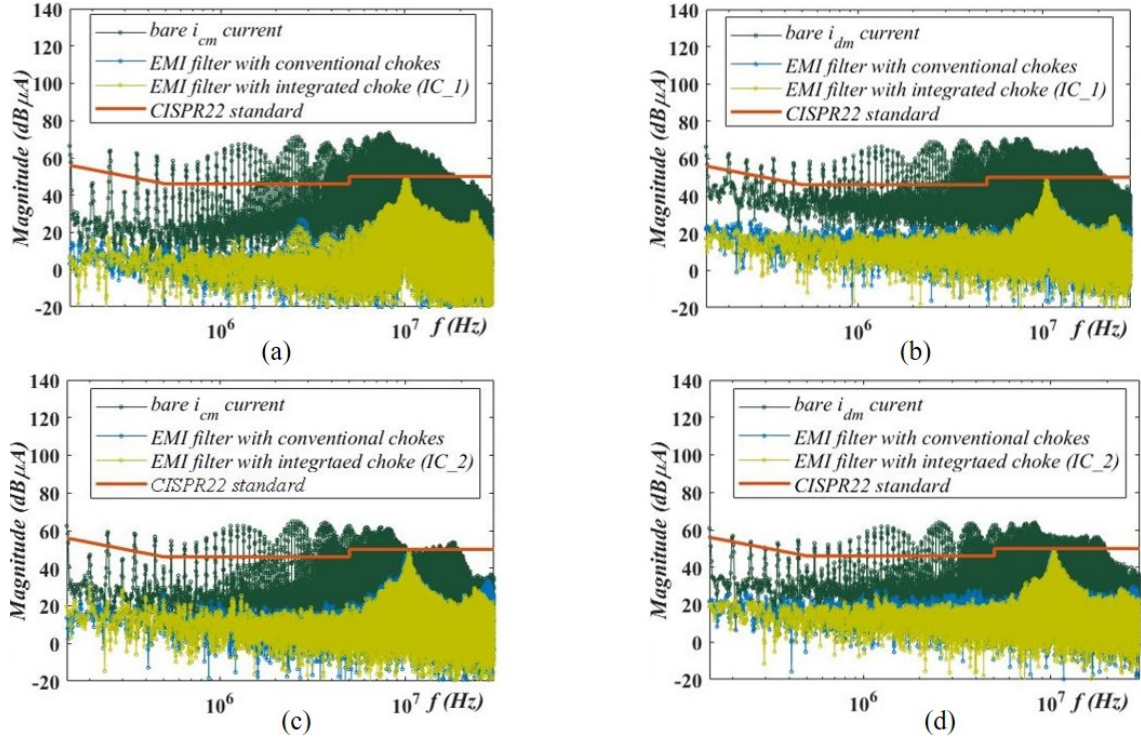
Figure 6.6: (a) CM current with EMI filter incorporating conventional and IC-1 choke, (b) DM current with EMI filter incorporating conventional and IC-1 choke, (c) CM current with EMI filter incorporating conventional and IC-2 choke, and (d) DM current with EMI filter incorporating conventional and IC-2 choke.
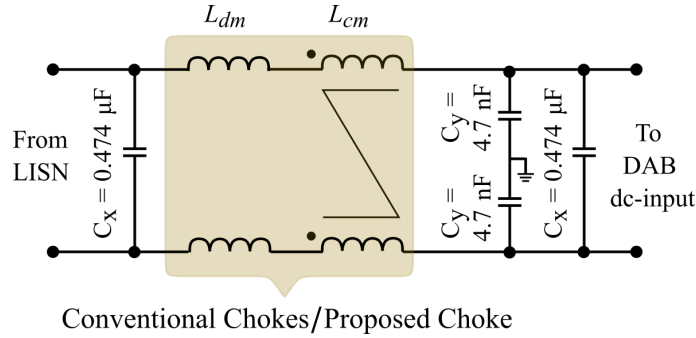
Figure 6.7: Electrical equivalence of single-stage EMI filter.

Table 6.3: Estimated and Measured CM and DM Inductance of IC-1 and IC-2

	$L_{cm(IC-1)}$	$L_{dm(IC-1)}$	$L_{cm(IC-2)}$	$L_{dm(IC-2)}$
Estimated	23.37 mH	333.03 μH	6.23 mH	146.48 μH
Measured	23.30 mH	346.14 μH	5.6 mH	164.5 μH

green in Figures. 6.6(c) and (d), respectively. It is observed from Figure 6.6 that the bare i_{cm} and i_{dm} currents exceed the standard limit line. Hence, a single-stage EMI filter, whose electrical equivalence is shown in Figure 6.7, is employed to mitigate the i_{cm} and i_{dm} currents within the standard. For the DAB converter operating at 1 kW, the EMI filter-I with the conventional chokes is designed to reduce the i_{cm} as
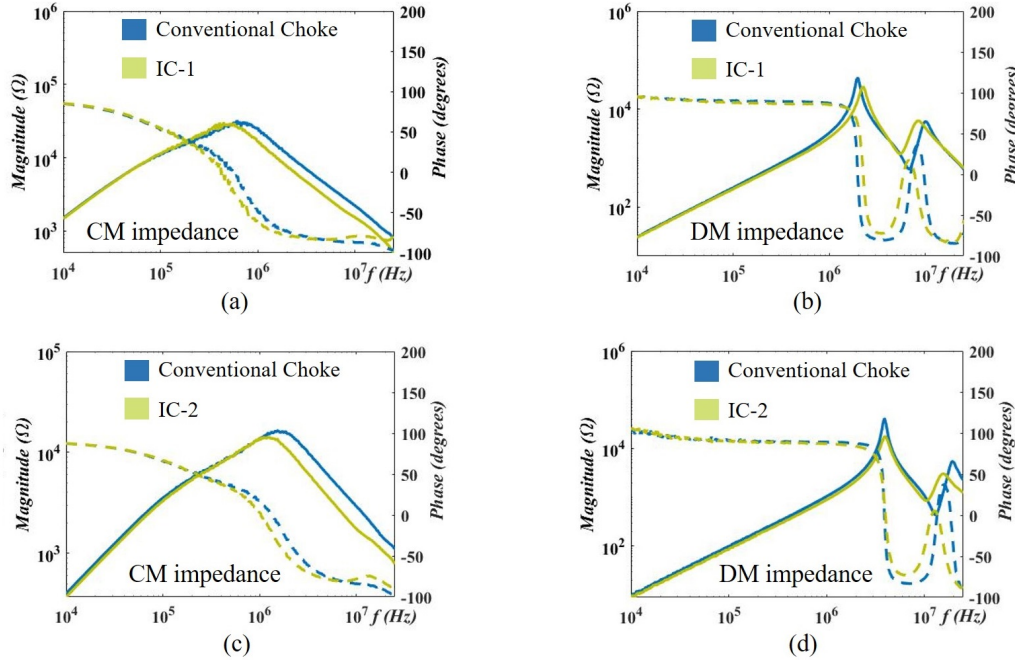
Figure 6.8: Measured impedance (solid line) and phase (dotted line) of the proposed and conventional chokes. (a) CM impedance of IC-1 and the corresponding conventional choke, (b) DM impedance of IC-1 and the corresponding conventional choke, (c) CM impedance of IC-2 and the corresponding conventional choke, and (d) DM impedance of IC-2 and the corresponding conventional choke.
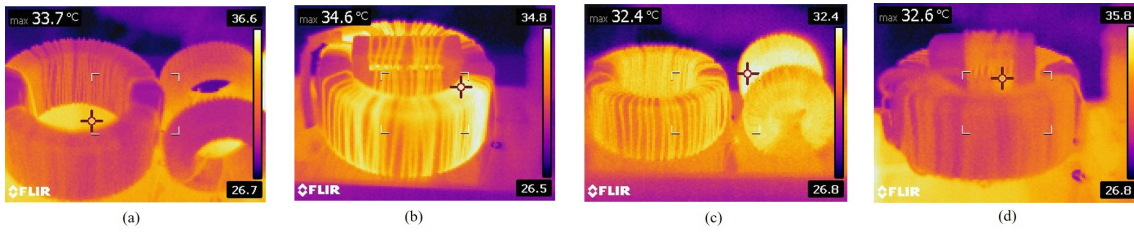
Figure 6.9: Thermal performance of single-stage EMI filter. (a) Conventional chokes of EMI filter-I, (b) IC-1, (c) conventional chokes of EMI filter-II, and (d) IC-2.

Table 6.4: PCB Area and Box Volume of EMI Filters with Conventional and Proposed Chokes

Filter Type	Type of choke	PCB Area (mm^2)	Filter Volume (mm^3)
EMI filter-I	Conventional	8192.5	286737.5
	IC-1	6780	237300
EMI filter-II	Conventional	6658.2	199746
	IC-2	5127.3	179455.5

well as i_{dm} currents within the standard, as shown in blue in Figures. 6.6(a) and (b), respectively. Similarly, for the DAB converter operating at 0.5 kW, the EMI filter-II with the conventional chokes is designed to reduce the i_{cm} as well as i_{dm} currents
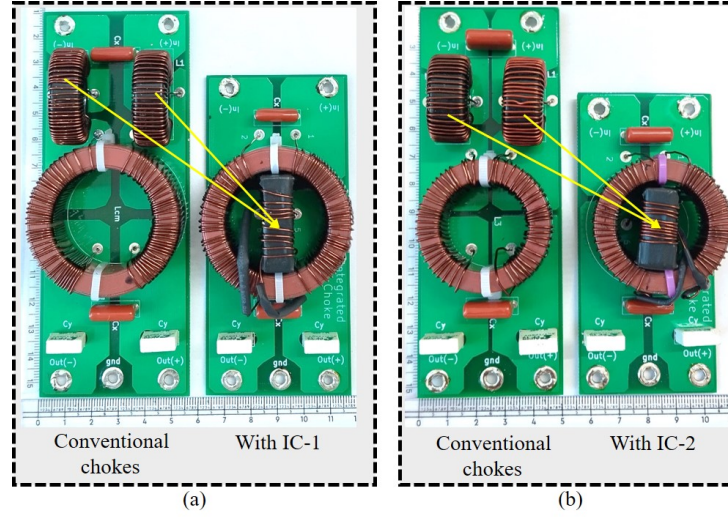
Figure 6.10: Single-stage EMI filters. (a) EMI filter-I and (b) EMI filter-II.

within the standard, as shown in blue in Figures. 6.6(c) and (d), respectively. The core properties of the conventional chokes in EMI filters I and II are listed in Table 6.1. Further, the CM and DM noise incorporating the EMI filters I and II with the IC-1 and IC-2 chokes, respectively, are discussed in detail.

6.4.1   Estimated   and   Experimental   Small   Signal Measurement

The core properties, reluctance, and the number of turns for the designed integrated chokes IC-1 and IC-2 are listed in Table 6.2. The relative permeability of the ER and toroidal cores of IC-1 are 1000 and 12000, respectively. The relative permeability of ER, I, and toroidal cores of IC-2 are 1000, 260, and 7500, respectively.

The inductance $L_{cm(IC-1)}$, $L_{dm(IC-1)}$, $L_{cm(IC-2)}$, and $L_{dm(IC-2)}$ estimated from (6.5), (6.10), (6.21), and (6.24), respectively, and the corresponding measured values are given in Table 6.3. It is observed from Table 6.3 that the estimated and measured $L_{cm(IC-1)}$ and $L_{cm(IC-2)}$ inductance match to a greater extent. The small deviations in the measured and estimated $L_{dm(IC-1)}$ and $L_{dm(IC-2)}$ inductance are due to the increase in the effective permeability of the toroidal core after inserting either the ER cores or ER and I cores into the window area of the toroidal core [71].

The CM and DM impedance of EMI filter I with conventional chokes and IC-1 are shown in Figures. 6.8(a) and (b). Similarly, the CM and DM impedance of EMI filter II with the conventional chokes and IC-2 are shown in Figure 6.8(c) and (d). It is observed from Figures. 6.8(a) and (c) that, the CM impedance of the EMI filters I and II with the conventional and proposed chokes match to a greater extent till 1 MHz. However, the dis-similarities above 1 MHz in Figure 6.8(a) and (c) are due to the effect of equivalent parasitic capacitance (EPC) of the windings [46];

Table 6.5: Comparison Between EMI Filters with Conventional and Proposed Chokes

EMI filter	Type of choke	PCB Area (mm^2)	Filter Volume (mm^3)
EMI Filter-I	Conventional	8192.5	286737.5
	Proposed	6780.0	237300.0
EMI Filter-II	Conventional	6658.2	199746.0
	Proposed	5127.3	179455.5

however, this doesn't significantly impact the CM current attenuation performance. It is observed from Figure 6.8(b) and (d) that the EMI filters I and II with the conventional and proposed chokes offer identical DM impedance.

6.4.2   Attenuation Performance of EMI Filters with Conventional and Proposed Chokes

The attenuated i_{cm} and i_{dm} currents with the EMI filter-I incorporating IC-1 are shown in light green in Figures. 6.6(a) and (b), respectively. Similarly, the attenuated i_{cm} and i_{dm} currents with the EMI filter-II incorporating IC-2 are shown in light green in Figures. 6.6(c) and (d), respectively.

It is observed from Figure 6.6 that EMI filters I and II incorporating the conventional and proposed integrated chokes offer similar CM and DM noise attenuation performance.

In addition, the thermal behavior of the EMI filter-1 with conventional chokes and IC-1, with an output current of 4 A, is shown in Figures 6.9(a) and (b), respectively. Similarly, the thermal behavior of the EMI filter-II with conventional chokes and IC-2, with an output current of 3.5 A, is shown in Figures 6.9(c) and (d), respectively. It is observed from Figure 6.9 that the maximum temperatures of the conventional and the proposed chokes are similar in both the EMI filters I and II. Thus, the EMI filters I and II with the proposed choke provide similar attenuation and thermal performance as compared to the corresponding EMI filters with the conventional chokes. Further, the benefits of the proposed chokes in terms of the PCB area and volume are discussed in detail.

Table 6.6: Comparative Assessment

Feature	[68]	[69]	[70]	IC-1	IC-2
Utilizes commercially available cores	Yes	Yes	Yes	Yes	Yes
Utilizes the whole core area	No	Yes	No	Yes	Yes
Flexibility to adjust the air gap	No	Yes	No	Yes	Yes
Additional DM flux in CM choke core	No	Yes	No	No	No

6.4.3 Comparison of PCB Area and Volume of EMI filters with the Conventional and Proposed Chokes

The designed single-stage EMI filters I and II with the conventional and proposed chokes are shown in Figure 6.10. The PCB footprint area and box volume of the EMI filters, shown in Figure 6.10, are presented in Table 6.5. As evident from Table 6.5, the EMI filter-I incorporating IC-1 reduces the PCB footprint area and box volume by 17.2 %, when compared to the EMI filter-1 with conventional chokes. Similarly, the IC-2 reduces the PCB footprint area and box volume of EMI filter-II by 23 % and 10 %, respectively, when compared to the corresponding conventional chokes. Thus, employing the proposed chokes reduces the PCB footprint area and box volume of the EMI filters.

6.4.4 Comparative assessment

As discussed in Section 2.1, the integrated chokes presented in [68], [69], and [70] utilize the window area of the CM choke to improve the DM inductance. Hence, to validate the benefits of IC-1 and IC-2, the qualitative comparison of IC-1 and IC-2 with the integrated chokes presented in [68], [69], and [70] is formulated in Table 6.6. It is evident from Table 6.6 that, the IC-1 and IC-2 have all the desired features such as (a) utilizing the commercially available core structures, (b) utilizing the core area to a larger extent, (c) providing flexibility to alter the DM inductance by utilizing the air gap, and (d) avoiding the additional DM flux through the high permeability CM choke; thereby avoiding the CM choke core saturation. Thus, IC-1 and IC-2 show improved performance to that reported in the literature.

6.5 Summary

The core arrangements and the winding structures of the two integrated magnetic chokes IC-1 and IC-2 have been discussed in detail in this paper. The theoretically estimated CM and DM inductances offered by IC-1 and IC-2 match to a greater

extent with the experimental measurements. From the ANSYS simulations, the CM and DM flux paths in all the cores of IC-1 and IC-2 match with the analysis. The EMI filter-I with the IC-1 choke and the EMI filter-II with the IC-2 choke are observed to have similar attenuation performance when compared to their equivalent EMI filters with conventional chokes. With the identical CM and DM noise attenuation performance, the PCB area and box volume of the EMI filter with IC-1 are reduced by 17.2 % when compared to the EMI filter with conventional chokes. While, the PCB area and box volume of the EMI filter with IC-2 are reduced by 23 % and 10 %, respectively when compared to the EMI filter with the conventional chokes.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The conducted EMI study plays a vital role in preventing the undesired operational performance of the DAB converter. The considerably large number of the high dv/dt nodes in the DAB converter and their corresponding parasitic capacitance complicate the CM and DM noise propagation paths. However, the CM and DM noise propagation paths are thoroughly analyzed from the CM and DM noise models derived in this thesis.

The experimental approach to measure the CM and DM noise through the transformer's intrawinding parasitic capacitance is presented by employing an impedance-match circuit. The sensitivity of the DM noise measurement incorporating the impedance-match circuit is discussed in detail. In addition, the estimated and measured MMDM noise match significantly.

Further, the thesis focuses on analyzing the DAB converter's CM and DM noise propagation paths in the presence of the first and second-order DC-input CM filter. It is observed that, with either the DC-input CM choke or CM LC filter, the CM noise at the DC-input side is diverted to flow through the existing lower impedance paths. This diversion in the flow of CM noise within the converter instead of getting attenuated resulted in CCMC. The coupled-inductor-based approach presented in this thesis, to address the CCMC, provides the below functionalities.

1. It provides the required inductance for the desired power transfer in the DAB converter.

2. It provides the required CM inductance to attenuate the CCMC.

In addition to the coupled-inductor-based integrated magnetic structure, the work in the thesis presents a concentric CM choke structure that can be incorporated into the DC-side CM filters. It is observed that, with identical CM noise attenuation performance, the concentric CM choke occupies a substantially lower volume than the conventional toroidal CM choke. Thus, the concentric CM choke reduces the volume occupancy of the CM filters. Therefore, the concentric common-mode choke serves as an effective substitute for conventional toroidal CM chokes in CM EMI

filters. Moreover, the CM noise of the DAB converter incorporating the integrated transformer is analyzed in detail. It is observed that the CM noise significantly reduces with the integrated transformer due to the elimination of the unwanted resonances in the CM impedance of the DAB converter. Thus employing the integrated transformer reduces the CM noise of the DAB converter, thereby reducing the CM choke inductance requirement.

Similarly, the presented CTI and the CTDMC configurations improve the DM inductance within the box volume of the inductor. Hence, incorporating the CTI and CTDMC provides the benefit of achieving higher DM inductance when compared to their equivalent conventional toroidal inductors without an increase in volume occupancy.

Along with the above-mentioned CM and DM integrated structures, the thesis presents the two integrated choke structures for single-stage passive EMI filters. The presented integrated chokes offer higher DM inductance when compared to its equivalent conventional CM choke structure, thereby reducing the external DM inductance requirement in the conducted EMI filters. As the designed integrated chokes offer higher DM inductance, it eliminates the requirement of additional inductors in the EMI filters, thus reducing the volume of the passive EMI filters.

Thus, the conclusions can be made from the thesis.

1. The external-matched impedance approach effectively estimates the conducted EMI noise through the transformer's primary to secondary winding capacitive coupling.

2. The coupled-inductor-based approach reduces the CCMC in the DAB converter.

3. The concentric CM choke structure reduces the volume occupancy of the CM filters.

4. Incorporating an integrated transformer reduces the CM noise of the DAB converter, thereby reducing the CM filter requirement.

5. The integrated DM inductors improve the DM impedance without increasing the volume occupancy.

6. The integrated choke with higher DM impedance effectively reduces the volume of the single-stage passive EMI filters.

7.2   Future work

The future scope of the work includes,

1. Exploring the mitigation techniques to reduce the CCMC in isolated phase-shift full-bridge dc-dc converter topologies.

2. Investigating the radiated emissions due to the integrated structures and exploring the winding or core configurations that effectively eliminate the radiated noise.

3. Incorporating various parasitic capacitance cancellation techniques to improve the frequency response of the passive EMI filters with the presented integrated chokes.

4. Investigating the conducted as well as radiated EMI noise in the solid state transformer that incorporates the isolated DAB converters.

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List of Publications

Journals

Article 1: B. Dwiza, K. Jayaraman, N. B. Y. Gorla and J. Pou, "Analysis of Common-Mode Noise and Mixed-Mode Differential-Mode Noise in Dual Active Bridge Converter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022.

Article 2: B. Dwiza, K. Jayaraman, N. B. Y. Gorla and J. Pou, "Analysis of Common-Mode Noise and Design of a Reduced-Volume Concentric Choke for Dual Active Bridge dc-dc Converter with Integrated Magnetics," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2023.

Article 3: B. Dwiza, Samarjeet Singh, K. Jayaraman, N. B. Y. Gorla, and J. Pou, "Novel Integrated Common-mode Choke with improved DM inductance for dc-side EMI filters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2023 - Submitted.

Conference Proceedings

Article 1: B. Dwiza and J. Kalaiselvi, "Analytical Approach for Common Mode EMI Noise Analysis in Dual Active Bridge Converter," The 46th Annual Conference of the IEEE Industrial Electronics Society, IECON, pp. 1279-1284, 2020, DOI: 0.1109/IECON43393.2020.9254895.

Article 2: B. Dwiza, Samarjeet Singh, K. Jayaraman, and N. B. Y. Gorla, "New Toroidal Inductor Configurations for Improved Inductance," ONCON, 2022.

Article 3: B. Dwiza, S. Singh, J. Kalaiselvi and N. B. Gorla, "Analytical Modeling of Three-Winding Tunable Common-Mode Choke," IEEE IAS Global Conference on Renewable Energy and Hydrogen Technologies (GlobConHT), Maldives, 2023, pp. 1-5, 2023, doi: 10.1109/GlobConHT56829.2023.10087480.

Article 4: B. Dwiza and J. Kalaiselvi, "Analysis and Mitigation of Circulating Common-Mode Current in Isolated Dual Active Bridge Converter", Annual Conference of the IEEE Industrial Electronics Society, IECON, 2023.