Analysis and Minimization of DC Link Ripple in Voltage Source Inverters

A Thesis Submitted

in Partial Fulfilment of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

by

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(2019EEZ0012)

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY ROPAR

July 26, 2024

To Dr. Babasaheb Ambedkar

I would like to dedicate this thesis to my father, Dr. Babasaheb Ambedkar. While my biological father gave me life, it is Babasaheb who has given me the right to live with dignity.

Declaration of Originality

I hereby declare that the work which is being presented in the thesis entitled **"Analysis and Minimization of DC Link Ripple in Voltage Source Inverters"** has been solely authored by me. It presents the result of my own independent investigation/research conducted during the time period from 25^{th} July 2019 to 29^{th} April 2024 under the supervision of **Dr. K. Ramachandra Sekhar, Assistant professor, Indian Institute of Technology Ropar**. To the best of my knowledge, it is an original work, both in terms of research content and narrative, and has not been submitted or accepted elsewhere, in part or in full, for the award of any degree, diploma, fellowship, associateship, or similar title of any university or institution. I also declare that any idea/data/fact/source stated in my thesis has not been fabricated/ falsified/ misrepresented. All the principles of academic honesty and integrity have been followed. I fully understand that if the thesis is found to be unoriginal, fabricated, or plagiarized, the Institute reserves the right to withdraw the thesis from its archive and revoke the associated Degree conferred. Additionally, the Institute also reserves the right to appraise all concerned sections of society of the matter for their information and necessary action (if any). If accepted, I hereby consent for my thesis to be available online in the Institute's Open Access repository, inter-library loan, and the title & abstract to be made available to outside organizations.

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Acknowledgement

I take this opportunity to acknowledge my heartfelt gratitude to all those people who directly or indirectly helped me to carry out this research work successfully. I am heartily thankful to my supervisor, Dr.K. Ramachandra Sekhar, whose encouragement, guidance and support through out my research work enabled me to develop an understanding of the subject. I appreciate his sincere help in terms of contributions of time, ideas so as to make my Ph.D. experience stimulating and productive.The joy and enthusiasm that he has for his research was contagious and motivational for me, even during tough times in the Ph.D. pursuit. I express my gratitude for his willingness to help and timely advices on issues, even beyond the scope of doctoral studies.

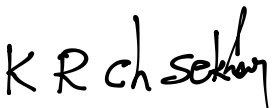
I would like to acknowledge the financial, academic and technical support of the Indian Institute of Technology Ropar for this research. I am sincerely grateful to Dr. J. Kalaiselvi, Dr. Bibhu Prasad Padhy and Dr. Prabir Sarkar for assessing the work and giving invaluable suggestions as members of the Doctoral committee.

The members of the Power Group have contributed immensely to my personal and professional time during my stay at the institute. The group has been a source of friendships as well as good advice and collaboration. I especially thank Mr. Baibhav Kumar Gupta, Mr. Mahesh Reddy Pundru, Mr. Aashish Kumar, Mr. Nikhil Kumar, Mr. A. Suryakiran, Mr. Digamber Kumar, Mr. Mahetab Alam, Mr. Manish Kumar, Mr. Ashwani Rana and Mr. Ankan Bhuniya for their valuable advice during my course of research and personal life. I would like to express gratitude to the services being offered by Mr.Devendra, Mr. Dilbag, and Mr.Jaspreet staff of the power electronics and Machine laboratory of the Electrical Engineering department. Last but not least I would like to thank my family, my parents who educated me, for always believing in my capabilities and for encouraging me to pursue my dreams. Especially my father, for unconditional support and encouragement, for listening to all my problems and frustrations very patiently and for always being there for me during good and bad times.

Certificate

This is to certify that the thesis entitled **"Analysis and Minimization of DC Link Ripple in Voltage Source Inverters"**, submitted by **Amol Ishwarrao Gedam (2019EEZ0012)** for the award of the degree of **Doctor of Philosophy** of Indian Institute of Technology Ropar, is a record of bonafide research work carried out under my guidance and supervision. To the best of my knowledge and belief, the work presented in this thesis is original and has not been submitted, either in part or full, for the award of any other degree, diploma, fellowship, associateship or similar title of any university or institution.

In my opinion, the thesis has reached the standard fulfilling the requirements of the regulations relating to the Degree.



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Abstract

In voltage source inverters (VSIs), pulse width modulation(PWM) techniques are employed to convert the available DC voltage into AC voltage at a high switching frequency. In PWM techniques, the fundamental space vector is generated using the instantaneous volt-sec balance of the switching states. The difference between the fundamental space vector and instantaneous switching states creates the error voltage. This error voltage influences the DC bus current and load current ripple. The instantaneous projection of error voltage onto the DC bus gives the DC current ripple pattern. This current ripple pattern defines the DC bus voltage ripple. A novel minimum DC voltage ripple generating PWM selection algorithm is proposed in this work for a three-phase two-level voltage source inverter. To elicit the minimum DC voltage ripple, firstly, the DC capacitor current, DC voltage ripple, and DC source current ripple are mathematically modeled for a three-phase two-level VSI using an error voltage vector approach. Based on mathematical modeling, different continuous PWMs (CPWMs) and discontinuous PWMs (DPWMs) are compared to derive the minimum DC voltage ripple. After comparison, the minimum DC voltage ripple regions are identified for CPWMs and DPWMs in the modulation index (m_a) and load angle (δ) plane. Based on the identified regions, an adaptive switching PWM selection algorithm is proposed to ensure the minimum DC voltage ripple irrespective of the load operating conditions. Further, by exploiting the concept of instantaneous mapping of AC error voltage onto the DC bus through power factor axis coordinates, in this research work, the unprecedented DC voltage ripple is modeled in the synchronous power factor reference frame for the dual inverter with common DC link. With the computed DC bus voltage ripple model, in this research work, the minimum DC voltage ripple yield PWM switching sequence is proposed for dual inverter with common DC link to minimize the DC bus voltage ripple for VSIs at different loading conditions. The effectiveness of the proposed work is demonstrated experimentally on a dual inverter setup in terms of optimum switching sequence elicitation. Further, the analysis of DC voltage ripple and DC source current ripple and its minimization is done on the dual inverter with a separate DC link. This work thoroughly analyzes the switching state correlation to minimize the DC voltage ripple without affecting the AC load current ripple. The analysis revealed that the switching algorithms must act to place the switching states by computing instantaneous DC capacitor current polarity. Using the polarity information, this work proposes the novel PWM dynamic sequencing mechanism that independently places the null and active vector in the sampling time interval to accomplish the minimum DC voltage ripple. Unlike conventional PWM methodologies, a prior capacitor current polarity computation makes the proposed algorithm dynamic in realizing the optimum switching sequence at any load condition without influencing the load current ripple. Further, the proposed method identifies the dwell times from the instantaneous phase reference voltages, freeing the algorithm from complex dwell time computations and sector identification. Therefore, the proposed methodology is simple in realizing variations in PWMs by simply

shifting/segregating the null time. Further, it is demonstrated that discontinuous PWMs having low current ripple can yield the lowest voltage ripple with the proposed sequence; otherwise, it is the highest among all other PWM variants.

Keywords: Capacitor stress, Common mode voltage elimination, DC Capacitor, DC current ripple, Dual two-level inverter, Load impedance, Pulse-Width Modulated (PWM) Inverters, Solar inverter, Space Vector PWM,

List of Publications

Journals

1. A. I. Gedam and K. R. Sekhar, **"Minimum DC Voltage Ripple Switching Sequence Elicitation for Dual Inverter Through AC Load Error Volt-Sec Computation,"** in IEEE Transactions on Power Electronics, vol. 37, no. 12, pp. 15654-15665, Dec. 2022, doi: 10.1109/TPEL.2022.3193886 (**Objective-1**).

2. Gedam, Amol Ishwarrao, and Kondapalli Ramachandra Sekhar. **"A Novel Switching Vector Sequencing Method to Optimize DC Voltage Ripple in Dual Inverter Drive Without Affecting Load Current Ripple."** IEEE Transactions on Industrial Electronics (2024) (**Objective-2**).

3. Amol Ishwarrao Gedam, K. Ramachandra Sekhar and Nikhil Kumar. **"Minimum DC Voltage Ripple Region Investigation for Discontinuous and Continuous PWM Techniques for 3-Phase 2-Level Voltage Source Inverter"** submitted in IEEE Journal of Emerging and Selected Topics in Power Electronics (**Objective-3**).

4. P. M. Reddy, A. I. Gedam and K. R. Sekhar, **"A Solar Series Grid Following Harmonic Compensator with Enhanced Grid Current Shaping and Active Power Injection Capability,"** in IEEE Transactions on Power Delivery, doi: 10.1109/TPWRD.2024.3369098.

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Patents

1. Amol Ishwarrao Gedam, Baibhav Kumar Gupta and K. Ramachandra Sekhar **"A single-stage voltage rectifier circuit for battery charging and a method of operating thereof"** (Registered at Indian Patent Office with Application number-202111016095).

2. Baibhav Kumar Gupta, Amol Ishwarrao Gedam and K. Ramachandra Sekhar **"suppressing circulating current through sequential switching of modular inverters in grid applications"** (Patent No: 464017).

3. Baibhav Kumar Gupta, Amol Ishwarrao Gedam and K. Ramachandra Sekhar **A method and system for performing adaptive gain adjustment in a solar inverter"** (Registered at Indian Patent Office with application no: 202311045914).

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3. A. H. Lone, A. I. Gedam and K. R. Sekhar, **"Voltage Support and Imbalance Mitigation during Voltage Sags by Renewable Energy Fed Grid-Connected Inverters,"** 2023 IEEE IAS Global Conference on Renewable Energy and Hydrogen Technologies (GlobConHT), Male, Maldives, 2023, pp. 1-6, doi: 10.1109/GlobConHT56829.2023.10087647.

4. A. H. Lone, A. Ishwarrao Gedam and K. R. Sekhar, **"Fault Ride Through with Conformance to Grid Voltage Limits in Photovoltaic Grid Connected Inverters.,"** 2023 IEEE IAS Global Conference on Emerging Technologies (GlobConET), London, United Kingdom, 2023, pp. 1-6, doi: 10.1109/GlobConET56651.2023.10150098.

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6. B. K. Gupta, A. I. Gedam and K. R. Sekhar, **"A Dual Inverter Based Grid Connected Solar Power Conditioning System With Coordinated Closed Loop Control,"** 2019 IEEE Innovative Smart Grid Technologies-Asia (ISGT Asia), 2019, pp.2178-2183, doi:10.1109/ISGT-Asia.2019.8880886

7. B. K. Gupta, K. R. Sekhar and A. I. Gedam, **"Balanced Per-Phase Sequential Switching to Suppress Circulating Current in Grid Connected Modular Solar Inverters,"** 2019 8th International Conference on Renewable Energy Research and Applications (ICRERA), 2019, pp. 686-691, doi: 10.1109/ICRERA47325.2019.8996838

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Chapter 1

Introduction

1.1 Environmental Imperatives: Rethinking Energy Sources and Transportation for a Sustainable Future

Conventional energy resources, such as fossil fuels (coal, oil, and natural gas), exert significant environmental impacts across their entire life cycle, encompassing extraction, processing, transportation, combustion, and waste disposal. These impacts include air pollution, greenhouse gas emissions, water pollution and consumption, land degradation, resource depletion, health implications, and waste generation. These environmental ramifications contribute to global warming and glacier depletion, necessitating prompt action. Both developed and developing nations are taking proactive measures to address the impacts of global warming by curtailing carbon emissions. The primary contributors to global warming include energy generation from conventional resources (coal, oil, and gas) and conventional transportation systems (petrol or diesel-based). An overview of energy generation from various sources and the adoption of eco-friendly transportation systems is crucial, considering both global and Indian perspectives.

1.1.1 Energy utilization from different resources

The Fig. 1.1 gives a visualization of global energy consumption until 2023 [1]. The data clearly illustrates that oil stands as the primary source of energy consumption worldwide, closely followed by coal, gas, and hydroelectric power. Collectively, energy consumption from gas, coal, and oil falls within the range of 40,000 TWh, showcasing their significant dominance in the energy landscape. In contrast, renewable energy sources like solar and wind contribute a mere 2,000 TWh to 4,000 TWh, indicating their comparatively lower share in the global energy mix. In India, energy consumption from sources such as coal and oil ranges from 4,000 TWh to 2,000 TWh as shown in Fig. 1.2. In contrast, renewable energy sources like solar and wind contribute only between 150 TWh to 200 TWh. This stark contrast underscores the need for increased investment and adoption of renewable energy sources to diversify India's energy portfolio and promote sustainability.

In Fig. 1.3, a visual representation of per capita energy consumption from different sources is presented for the top economies worldwide. The figure clearly illustrates that per capita energy consumption from renewable energy sources lags considerably behind other sources. This observation highlights the disparity in energy utilization patterns and underscores

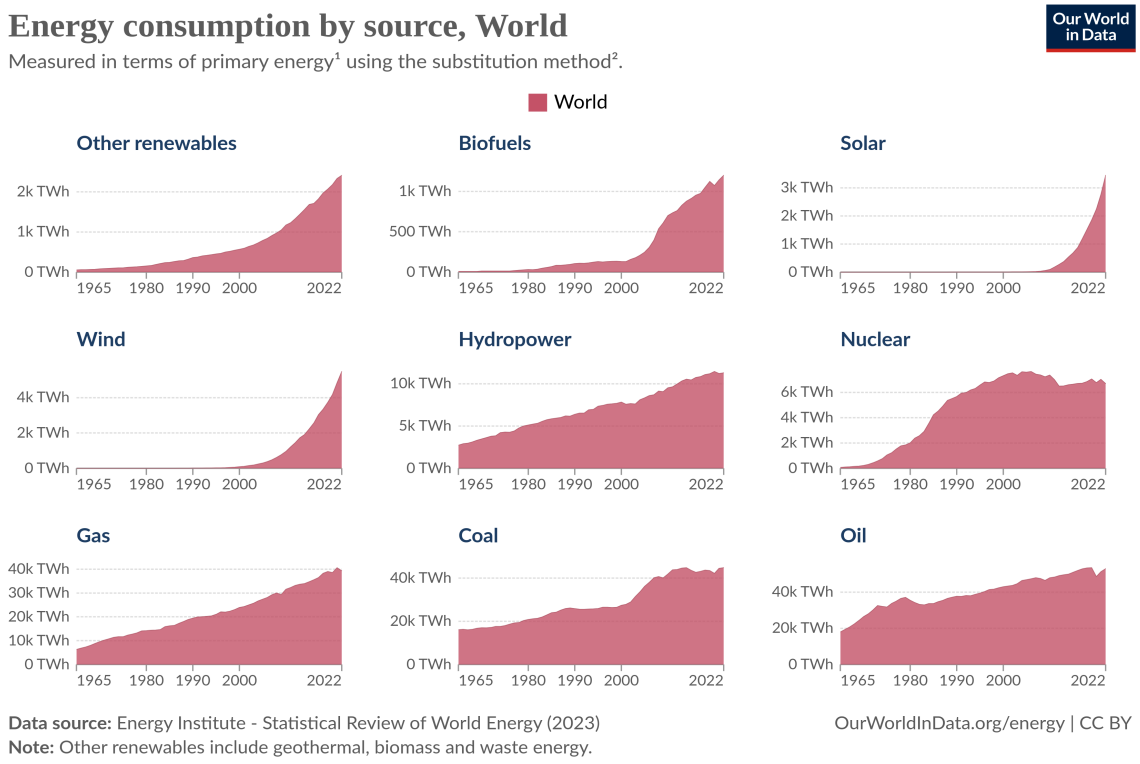


Figure 1.1: Energy consumption by source, Global [1]

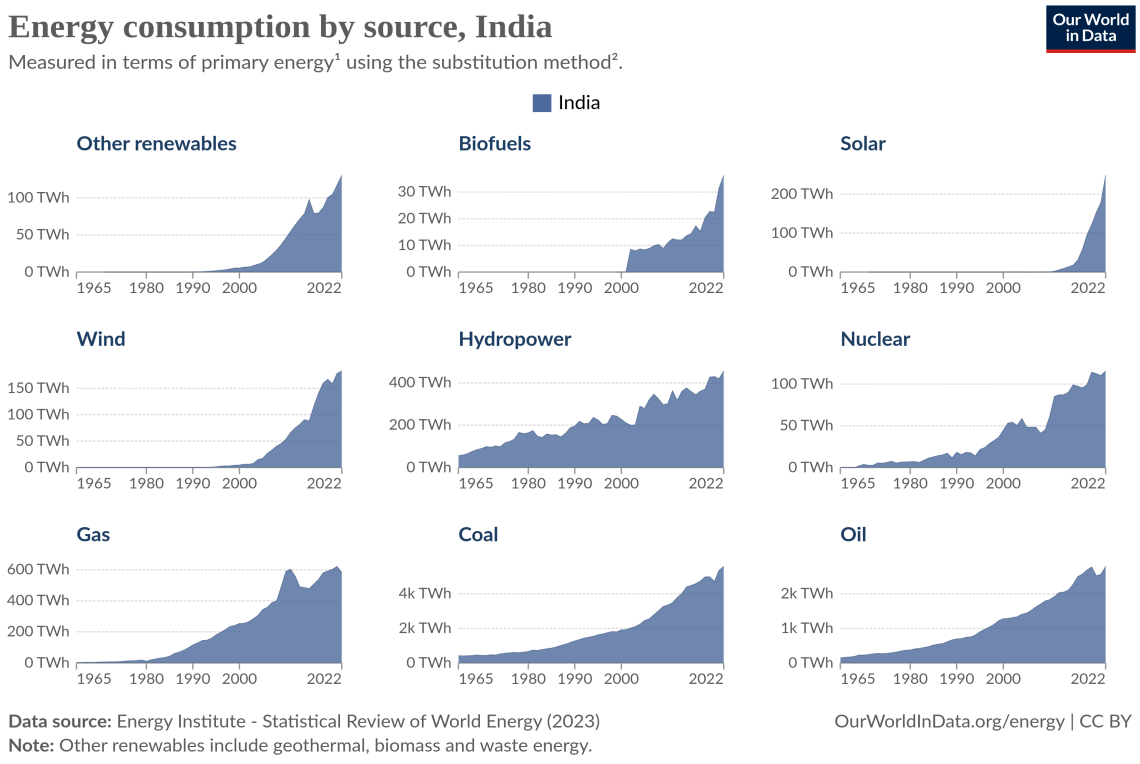


Figure 1.2: Energy consumption by source, India [1]

the potential for advancement and wider adoption of renewable energy technologies to tackle sustainability challenges. Similarly, the subsequent subsection will delve into data pertaining to the adoption of eco-friendly vehicular systems.

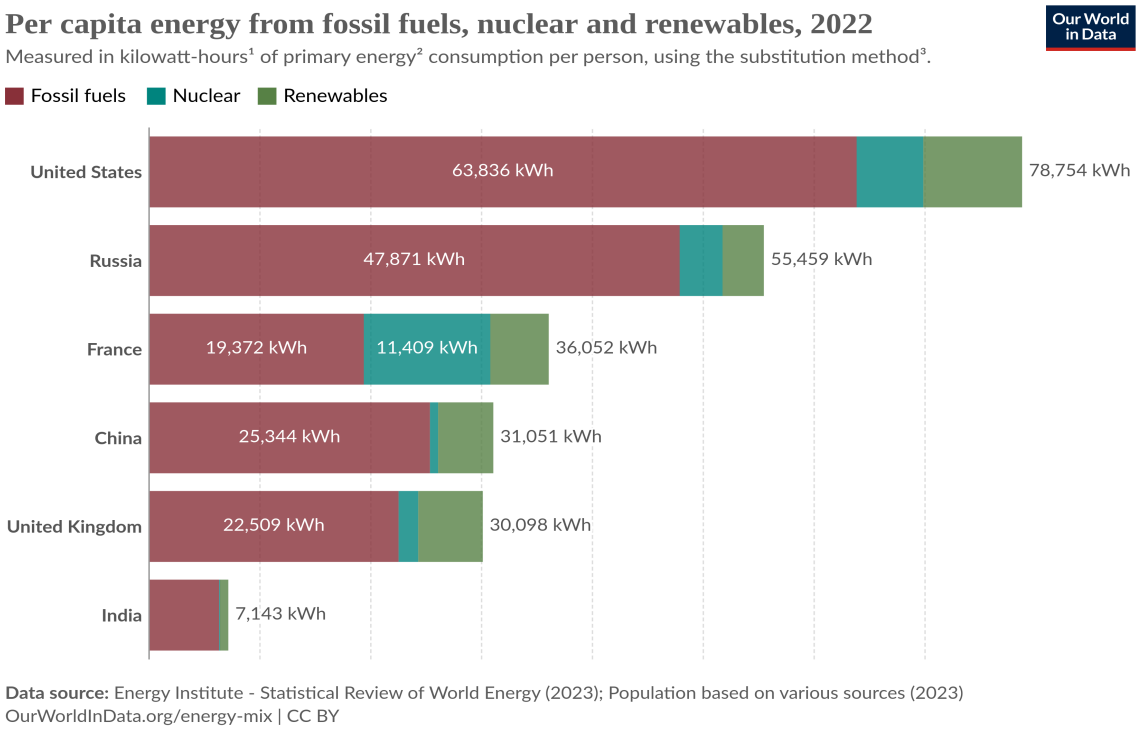


Figure 1.3: Per capita energy consumption by source, India [1]

1.1.2 Adoption of eco-friendly vehicles for the transportation system

The conventional vehicular system relies on petrol or diesel as fuel, contributing to environmental degradation through the emission of greenhouse gases, thereby exacerbating global warming. In contrast, electric or hybrid electric vehicles present an eco-friendly alternative. These vehicles utilize batteries in conjunction with another power source to propel the vehicle, offering reduced emissions and a more sustainable mode of transportation.

In Fig. 1.4, data pertaining to the sales of new cars categorized as battery-electric and plug-in hybrid is presented. The figures reveal that Norway boasts the highest number of such cars sold, while the percentage of sales in India remains notably low [2]. This discrepancy underscores varying adoption rates of electric and plug-in hybrid vehicles across different regions, highlighting the need for further analysis and initiatives to promote their uptake in countries with lower adoption rates. In Fig. 1.5, the global sales data for electric cars is depicted. The figures highlight China as the leader in electric car sales, while India's electric car sales remain comparatively lower. This data underscores the prevalent use of petrol and diesel-fueled vehicles in India. This data also shows that India should adopt eco-friendly (Electric or hybrid electric) vehicles to promote clean energy.

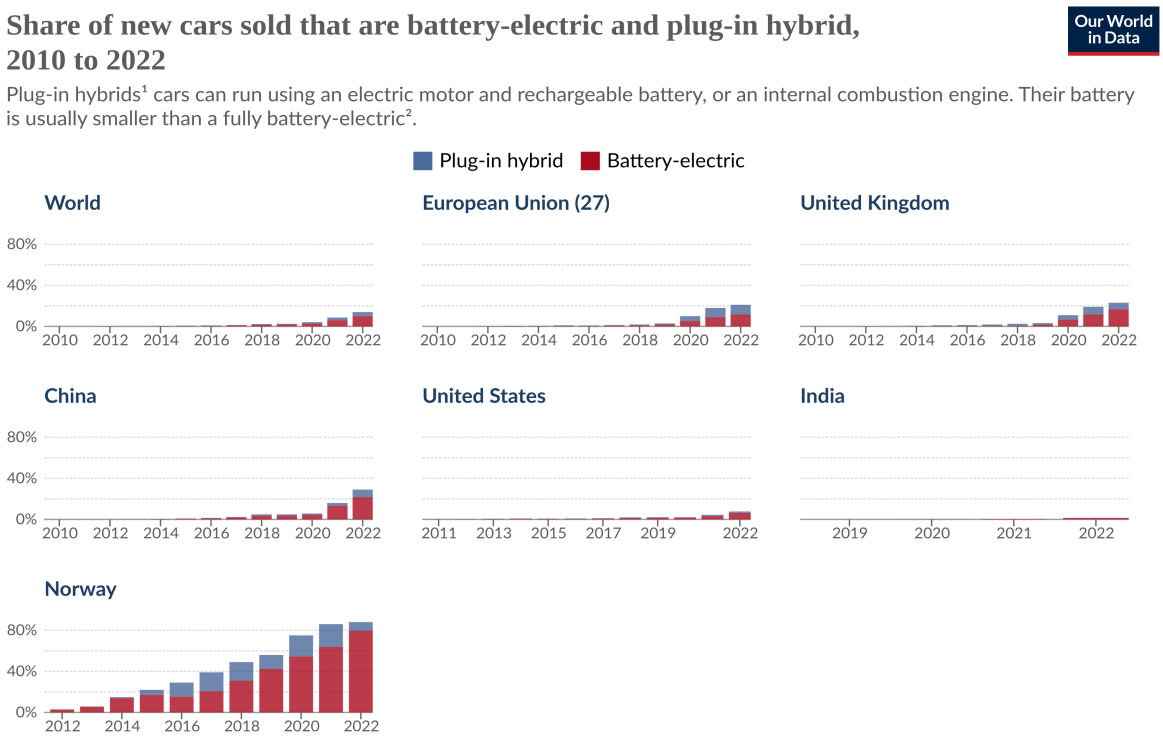


Figure 1.4: Share of battery-electric and plug-in hybrid new cars sold [2]

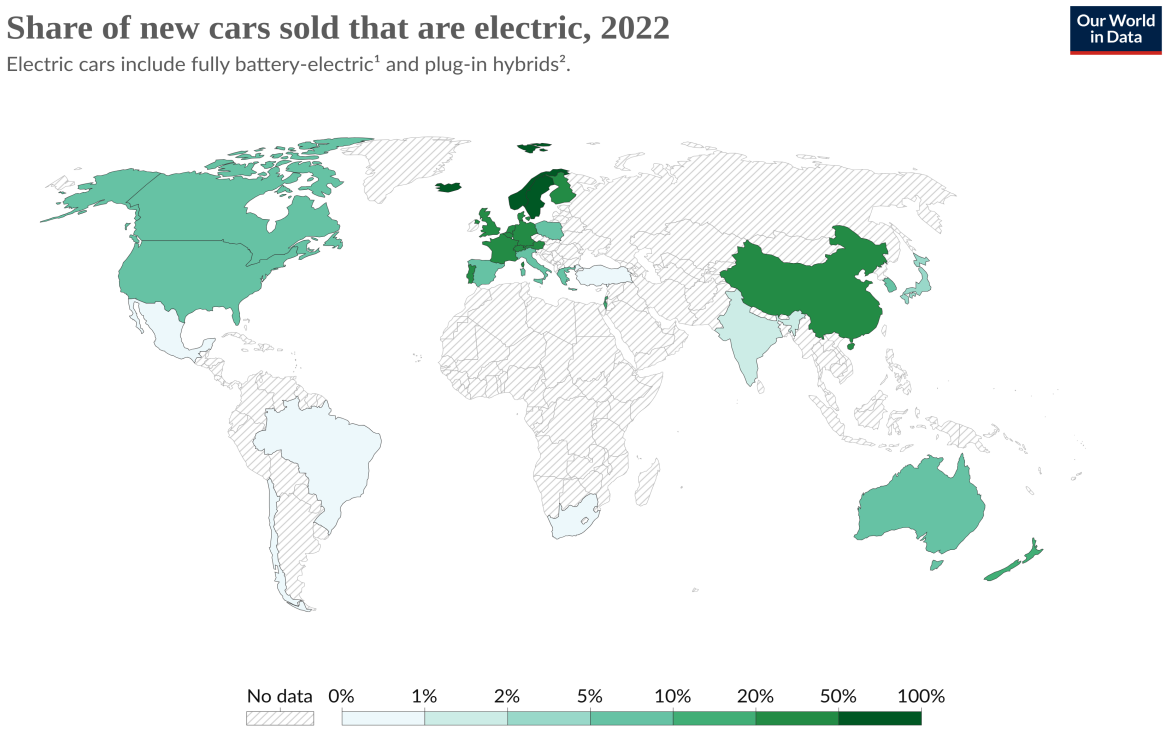


Figure 1.5: Electric car sold share [2]

1.2 Motivation

In pursuit of increasing energy generation from renewable resources and transitioning towards an eco-friendly transportation system, India has unveiled its 2030 mission. During COP26, India unveiled ambitious targets aimed at decarbonizing its energy sector by 50% and attaining 500 GW of energy generation from renewable sources by 2030. To facilitate cleaner energy generation from renewable sources and promote the adoption of electric vehicles in the transportation sector, the Government of India has rolled out several schemes designed to incentivize and support these initiatives [3]. Notable schemes include:

- **Solar Park Scheme**: Intends to construct multiple solar parks, each boasting an approximate capacity of 500 MW.
- **Rooftop Solar Scheme**: Aspires to leverage solar energy through the installation of solar panels on residential rooftops.
- **SRISTI Scheme**: To advance rooftop solar power initiatives across India.
- **International Solar Alliance**: Collaborative platform for increased deployment of solar energy technologies.
- **Kisan Urja Suraksha evam Utthaan Mahabhiyan (PM-KUSUM)**: Initiated by the Ministry of New and Renewable Energy (MNRE) to bolster the deployment of off-grid solar pumps in rural regions and diminish reliance on the grid in connected areas.
- **UDAN**: (Airport runway lighting system, Solar integrated technologies for railways, Battery charging station)
- **DDUGJY** (Rural electrification, Micro-grid solutions)
- **FAME** (Faster Adoption and Manufacturing of Electric Vehicles)

This scheme accelerates the integration of renewable energy with the grid by utilizing advanced grid-connected inverters and variable frequency drive technology. It enables the seamless transfer of renewable energy to the grid while also powering electric or hybrid electric vehicles (EVs). The renewable energy grid-connected inverter technology uses VSIs to efficiently channel available active power into the grid at unity power factor. On the other hand, variable frequency drives utilize VSIs to precisely control output voltage,This ripple pattern defines the DC bus voltage ripple. frequency and magnitude, thereby ensuring EVs achieve the desired speed and torque.
Various VSI topologies have been proposed in the literature to enhance power quality, increase efficiency, offer flexible control, and reduce DC bus voltage. VSIs utilize pulse width modulation (PWM) techniques to convert available DC voltage into AC voltage efficiently. These PWM techniques are crucial for switching the inverter to produce a

fundamental voltage across the load with minimal distortion. In VSIs, PWM techniques are essential for converting DC voltage to AC voltage at high switching frequencies. During this conversion process, the current in the DC link switches at the same frequency, resulting in a pulsating current in the DC link. The harmonics of this pulsating current are absorbed by the DC capacitor. The RMS current flowing through the DC capacitor determines its overall lifespan. Similarly, the instantaneous current flowing through the capacitor generates both DC voltage ripple and DC source current ripple. The DC voltage ripple dictates the DC capacitor value—higher DC voltage ripple necessitates higher DC capacitance to keep it within permissible limits. The magnitude of the DC voltage ripple also depends on the switching pattern of the PWM. Each PWM has a specific switching pattern, resulting in different magnitudes of DC voltage ripple. Therefore, it is essential to conduct a thorough analysis of DC link ripple, considering the different PWM technique and VSI topology, to properly size the DC capacitor for dedicated inverter and PWM. For a comprehensive understanding, the following section delves into an extensive literature survey on various VSI topologies, PWM techniques, and DC link ripple.

1.3 Types of voltage source inverters

VSIs are essential components in power electronic systems for converting DC voltage to AC voltage. Various VSI topologies have been developed to meet different application requirements, considering factors such as efficiency, voltage levels, harmonic distortion, and scalability. The conventional two-level VSI is the simplest topology, consisting of switches arranged in a bridge configuration, typically an H-bridge. While simple and cost-effective, it suffers from high voltage stress on the switches and limited voltage levels [4]. To reduce the voltage stress on the switches and increase the voltage levels, multilevel inverter topologies are came into existence which are followed as:

- **Neutral-Point Clamped (NPC) VSIs**: Neutral-Point Clamped VSIs utilize additional clamping diodes and capacitors to achieve multiple voltage levels, reducing voltage stress on switches and improving waveform quality. They are commonly used in medium to high-power applications [5].

- **Flying Capacitor (FC) VSIs:** Flying Capacitor VSIs employ flying capacitors to generate multiple voltage levels, enabling improved efficiency and reduced harmonic distortion compared to conventional two-level VSIs. They find applications in medium-voltage motor drives and renewable energy systems [6].

- **Cascaded H-Bridge (CHB) VSIs:** Cascaded H-Bridge VSIs consist of multiple H-bridge cells stacked in series to achieve higher voltage levels with improved waveform quality and reduced harmonic distortion. They are extensively used in high-power applications such as grid-connected renewable energy systems and high-voltage motor drives [7].

The realm of advanced voltage source inverter (VSI), research has been actively engaged in pioneering new topologies to effectively tackle specific challenges such as enhancing efficiency, ensuring fault tolerance, and promoting modularity. Noteworthy among these innovations are the emergence of Hybrid VSIs, T-type VSIs, Modular Multilevel Converters (MMC), and Soft-Switching VSIs [8]-[9]. In recent years, the dual inverter configuration has garnered significant attention, finding applications in both motor drives and grid-connected solar inverters. This configuration stands out for its ability to synthesize the required AC voltage while maintaining reduced DC bus potentials in comparison to conventional setups. It is worth noting, however, that the dual inverter configuration entails a higher count of switching devices when contrasted with traditional inverter circuits [10]. Nevertheless, this surplus of switching devices enables the elimination of common-mode voltage through CMV-eliminated PWM techniques, thereby enhancing operational flexibility, especially in scenarios where a common DC bus is employed [11]-[12]. The dual two-level inverter-fed open-end winding drive configurations have gained researchers' attention in variable frequency and aircraft drives. The performance characteristics of the dual inverter in terms of common mode voltage, DC bus utilization, phase voltage profile, and switching losses are analyzed in [13]. The closed-loop control of dual inverter operated OEWIM drive with model predictive control (MPC) is done to eliminate the dead time effect on common mode voltage in [14], scalar-control of dual inverter operated OEWIM for speed range extension in [15], predictive control to balance the SoC of batteries in [16] and decoupled floating capacitor voltage control in [17]. In recent literature, the dual inverter is used in controlling the open-end winded permanent magnet synchronous motor (OEWPMSM) drives [18]-[19]. In [18], an advanced discontinuous PWM is proposed to reduce the switching losses in OEWPMSM. In [19], the dual inverter is used to suppress the zero sequence current with common mode voltage control while in [20], the dual inverter is used to reduce the leakage current and common mode voltage. The weighting-factor less predictive torque control scheme is proposed in [21] for OEWPMSM. In a recent scenario, the dual inverter is popularly used in the area of aircraft drives. A dual inverter topology along with the quasi network feeding to electric aircraft is proposed in [22] along with the common mode voltage minimization in [23].

VSIs employ PWM techniques to convert available DC voltage into AC voltage. PWM techniques offer the advantage of switching VSIs at higher frequencies, resulting in reduced harmonic distortion in the output voltage. Consequently, the need for filtering to attenuate harmonics is reduced as compared to systems without PWM techniques. The subsequent sections provide a comprehensive literature review of various PWM techniques, elucidating their applications and benefits in power electronic systems.

1.4 Pulse width Modulation Techniques

Pulse width modulation techniques are employed in VSIs to switch the inverter efficiently to ensure the production of fundamental voltage across the load with minimal distortion. The recent literature emphasizes PWM designs that account for load current ripple. For instance, a random PWM selective harmonic elimination technique is proposed in [24] to eliminate specific harmonics in the output voltage. In [25], a modified SVPWM is introduced to reduce switch overlap time for improved output waveform quality. A staggered PWM scheme is proposed in [26] to minimize peak AC common-mode current in three-level inverters. Meanwhile, [27] presents a level-shifted multi-carrier PWM technique to curtail switching losses. A discontinuous space vector PWM (DSVPWM) technique is introduced in [28] for three-level inverters to arrest output harmonics, enhance the linear region of the modulation index, and curtail switching losses. A hybrid space vector PWM is proposed in [29] for multi-phase 2-level VSIs, reducing computational effort and memory usage. Additionally, [30] introduces a novel SVPWM that utilizes smaller vectors with lower common-mode voltage (CMV) magnitudes for T-type active impedance source inverters. In [31], an improved multi-carrier PWM (MCPWM) is proposed for a five-level cascaded H-bridge inverter to reduce low-frequency harmonic magnitudes from output voltages. Similarly, [32] proposes an optimal current ripple PWM (OCR-PWM) to minimize common-mode voltage and output current ripple for three-level inverters.

In the dual inverter segment, numerous PWM techniques have been proposed to enhance the parameter performance for open-end winded induction motor (OEWIM) and open-end winded permanent magnet synchronous motor (OEW-PMSM). Considering the common mode voltage as a parameter, [33] presents a PWM technique to eliminate common mode voltage, [34] presents the hybrid PWM technique for decreasing the common mode voltage, [35] presents the CMV elimination PWM for the dual inverter operating asymmetric six-phase PMSM, [36] presents the common mode voltage reduction strategy for dual inverter-operated asymmetric OEWIM, [37] presents the CMV minimization scheme for dual inverter-fed aircraft stator generators and [38] introduces two contemporary balanced-mode unified common-mode voltage elimination (CMVE) PWM techniques, offering flexibility with reference voltages and angular displacement between dual sets of three-phase windings. Considering the power loss perspective, An advanced CMV elimination technique is proposed in [39] to reduce the switching losses in dual inverter by clamping one inverter and switching another inverter, An improved PWM switching scheme is proposed in [40] to reduce the switching commutation for dual inverter-operated OEWIM. An angular modulation scheme is proposed in [41] aimed at reducing the switching losses in dual inverters. A clamping PWM technique is proposed in [42] to reduce and balance the power losses in open-end winded PMSM. In [43], an advanced discontinuous PWM technique is proposed for reducing the switching

losses in open-end winded PMSM. A simple DPWM technique is proposed in [44] for loss reduction in OEWIM. Other than the common mode voltage and power loss, the PWM scheme is proposed in [45] for the dual inverter to reduce the voltage space vector fluctuations. Similarly, in [46], the performance of the OEWIM is analyzed in terms of the common mode voltage, DC bus utilization, phase voltage profile, and switching losses for sub-hexagonal centered PWM. The equal and proportional duty SVPWM is proposed in [47] to generate the four-level waveform across the OEWIM. In [48], the hybrid over-modulation PWM technique is proposed to generate the 12-step operation. It improves the output voltage waveform quality and reduces the harmonic distortion. An advanced carrier phase shift modulation strategy is proposed in [49] to suppress the high frequency current harmonics. In [50], an alternative switching PWM technique is proposed for medium and high-speed regions of dual inverter-operated open-end winded PMSM. A hybrid seven-level scheme is proposed for dual inverter in [51] to reduce the number of switches and to increase the linear modulation region. A novel switching sequence is proposed for dual inverter operated open-end winded motor in [52] to reduce the computation burden of PWM. In [53], a carrier-based PWM technique is proposed for low-speed operation. In [54], a dual-space vector control strategy is presented for the open-end winding permanent magnet synchronous motor (OEW-PMSM) drive, powered by a dual inverter using a solitary DC source. The three new PWM techniques are proposed in [55] for dual inverter feeding an open-end winding induction motor (OEWIM) to reduce the voltage harmonic distortion in inverter output voltage. While existing PWM techniques primarily concentrate on parameters like reducing AC current ripple, minimizing or reducing or eliminating the common-mode voltage and power loss ongoing research continues to refine these methods.

VSIs function by delivering output voltage to the load through the utilization of PWM techniques [56]. This method involves controlling the average output voltage across the load. Any discrepancy between the average space vector and the instantaneous output voltage results in the generation of an error voltage across the load [57]-[58]. The magnitude and direction of this error voltage vector plays a pivotal role in determining both load current ripple and DC bus current ripple. A comprehensive investigation into the DC bus parameters and DC bus ripple will be elaborated upon in the subsequent section of this literature review.

1.5 DC capacitance and DC link Ripple

In VSIs, the DC capacitor restrains the DC bus voltage by absorbing the DC link current ripple. The high-frequency current ripple is detrimental to the life of the capacitor due to ESR [59]-[60]. Thus the DC capacitor not only acts as the weak link in deciding the overall reliability of the converter circuits but also contributes significantly towards the overall size and cost of inverter circuits. Among DC link capacitors, aluminum electrolytic

capacitors are used widely in industries for high power processing converters considering the capacitance value to form factor ratio [61]. Nevertheless, the offered capacitance at higher voltage negatively impacts the DC capacitor's overall life expectancy, size and volume. As per the literature [62], the electrolytic capacitor failure rate is 30% higher than the non-electrolytic capacitor. As mentioned in [63], the prolonged switching stress is the root cause of the capacitance value diminution and eventual increment in the capacitor's equivalent series resistance (ESR). The rise in ESR cascaded to thermal runaway issues and eventual failure of the capacitor [64]-[65]. Therefore researchers have attempted to reduce the demanded capacitance value using various techniques for improved reliability of inverter circuits. However, the trade-off between the capacitance value and the allowable voltage ripple in the inverter's DC link demands extensive design evaluation to size the appropriate capacitor bank considering the DC source performance and energy conversion efficiency [66]. Aligning with the requirement, it is recommended to reduce the DC capacitance value without compromising the allowable DC ripple percentage.

In attempts to model the DC bus parameters, the researchers have computed DC capacitor RMS current switching stress using time-domain [67]-[68] and harmonic spectrum approach [69]-[70]. The demonstrated methods used so far to compute the current stress of the DC capacitor demands the instantaneous AC load current information sensed at the output terminals of the load. The existing DC ripple stress computational models defined as $S_a i_a + S_b i_b + S_c i_c$ utilizes the sensed phase currents (i_a, i_b and i_c) and instantaneous switching states (S_a, S_b and S_c) used to evaluate the DC capacitor switching stress. But no attempts made so far to realize the optimum switching states for minimum DC voltage ripple. Since the inverter's switching instances influence the current ripple, the elicitation of instantaneous error volt-sec magnitudes for VSI is demonstrated in [71] while computing the torque ripple of the induction motor. With the help of the instantaneous phase current sensing model, the DC capacitor current stress for different two-level voltage source inverter configurations is evaluated by computing the aggregate RMS value over a fundamental cycle [67]-[72]. In [73], the anti-parallel diode reverses recovery characteristics are considered for computing the DC ripple current stress. The research reported in [74] concentrated on DC capacitor evaluation for the power factor correction converter. Further, the same instantaneous current information method is extended to compute the RMS current stress for multi-level inverters like cascaded H-bridge inverters [75], and diode clamped inverter circuits [76]. In [77], the lifetime of the DC capacitor is predicted for multiple drive systems by modeling the RMS current flowing through it. To reduce the common mode voltage (CMV) and DC link capacitor current, several PWM methods are proposed in [78] & [79]. The DC ripple analysis mentioned in [67]-[79] mainly focused on deriving the aggregate RMS ripple stress on the capacitor and addressed neither DC voltage ripple instantaneous variations nor its minimization.

Apart from computing DC RMS current, the researchers have used voltage ripple analysis

to size the DC capacitor at balanced [72] & [80] and unbalanced loading conditions [81] & [82]. Further, the voltage and current stress on the DC link are extensively examined in [83] for two-level six-phase VSIs for the symmetric and asymmetric distribution of load configuration. In [84] provides an analytical model for the characterization of DC link oscillations induced by harmonic injection into the grid. However, added switching instances and switching devices elevate the switching stress across the DC bus capacitor. Thus, the switching stress across the DC bus needs to be evaluated carefully to choose the appropriate DC capacitor to limit the DC bus voltage ripple within the permissible limit. By using the concept of computing instantaneous error volt-seconds within the synchronous power factor reference frame, it can effectively map AC error volt-seconds onto the DC circuit. This innovative approach lays the foundation for developing novel PWM techniques aimed at minimizing DC voltage ripple and DC source current ripple in voltage source inverters. Considering the significant impact of switching PWMs on DC voltage ripple, it becomes evident that varying switching patterns can alter DC voltage ripple and DC source current ripple signatures without disrupting the motor's rotating magnetic field. However, despite this understanding, there has been limited focus on devising PWM strategies to minimize DC bus voltage ripple in existing literature. This scarcity of research serves as the primary motivation behind the work presented in this thesis, which seeks to address the minimization of DC bus voltage ripple through advanced PWM techniques.

1.6 Objectives

Building upon an extensive review of existing literature, the objectives of this thesis are outlined as follows:

1. Minimum DC voltage ripple region investigation for discontinuous and continuous PWM techniques for 3-phase 2-level voltage source inverter.

2. Minimum DC voltage ripple switching sequence elicitation for dual inverter through AC load error volt-sec computation.

3. A novel switching vector sequencing method to minimize DC voltage ripple in dual inverter drive without affecting load current ripple.

1.7 Organisation of Thesis

1. **Chapter 1** provides a comprehensive review of renewable energy grid-connected inverters and variable frequency drives. It underscores the significance of VSIs along with PWM techniques and their influence on DC bus parameters and DC bus ripple. Additionally, it highlights the critical functions of DC link capacitors and addresses the effects of DC voltage and source current ripple in VSI technologies. Subsequently,

the chapter articulates the motivation and objectives of the thesis, followed by a structured outline of its organization.

2. **Chapter 2:** In this chapter, the DC bus voltage ripple modeling is established as a function of inverter switching and the load angle. The ripple model is derived by computing the instantaneous error vector on the load reference frame. Based on the analysis, it is identified that the ripple behaviors with the switching vary depending on the modulation and the load characteristics; thus, it is necessary to investigate appropriate switching to realize minimum DC voltage ripple at a given modulation and load characteristics. Considering the requirement, different PWM techniques, including continuous and discontinuous PWMs, are analyzed to identify the region of PWM operation to minimize the DC voltage ripple. Using the region of PWM operation, an adaptive algorithm is proposed in this work to select the PWM technique for minimizing the DC voltage ripple. The efficacy of the proposed algorithm is validated experimentally by evaluating the DC bus voltage ripple.

3. **Chapter 3:** In this chapter, a mathematical model designed to assess both the DC capacitor current and DC voltage ripple is introduced. This innovative model captures instantaneous AC error volt-sec reflections resulting from instantaneous switching on the DC bus via the load power factor axis. By replicating the exact DC capacitor current, derived from AC load error volt-sec reflections, it facilitates the derivation of an instantaneous voltage ripple model. Unlike conventional methods, the proposed model leverages load power factor information for AC to DC translation, eliminating the need for actual current sensing at load AC terminals, and rendering it an offline computational method. Moreover, the proposed model, developed in a synchronous reference frame, inherently maps AC fundamental current to DC average current, simplifying DC ripple segregation from computed DC bus current effectively. Leveraging these advantages, the proposed model is ideal for devising PWM techniques to achieve minimum DC voltage ripple performance across the DC bus of the inverter. The efficacy of the proposed model is validated on the dual inverter operated with a common DC bus, considering the heightened switching stress across the DC bus compared to other multi-level inverter configurations. Furthermore, it is shown that the switching instances with alternative error volt sequencing yield minimal DC voltage ripple within a sampling time interval in the dual inverter configuration. These findings are experimentally verified across various modulation and loading conditions, reaffirming the robustness of our proposed approach.

4. **Chapter 4:** This chapter introduces a novel dynamic switching sequence mechanism aimed at independently positioning the active and null switching vectors within a sampling time interval to minimize the DC side ripple performance in OEWIM. To achieve online dynamic sequencing, instantaneous capacitor current is mathematically modeled and demonstrates that the polarity of the capacitor current

alone is sufficient to dynamically determine the optimal switching sequence. Thus, the proposed polarity-based sequencing method is straightforward yet effective in deriving the minimum DC bus voltage and DC source current ripple under varying loading conditions (power factor angle) and modulation indices of the dual inverter drive. While reported work focuses solely on the influence of switching sequences on voltage ripple, the proposed sequencing methodology can be extended to PWMs (both continuous and discontinuous) utilized for minimizing the DC voltage and DC source current ripple performance. To showcase the effectiveness of the proposed dynamic sequencing methodology, the AC current minimization PWMs are selected and demonstrate that the proposed method can minimize the DC bus voltage and DC source current ripple without compromising drive AC current ripple performance.

5. **Chapter 5** presents the conclusion and future scope of the research.

Chapter 2

Minimum DC Voltage Ripple Region Investigation for Three-Phase Two- Level Inverter

In VSIs, Pulse Width Modulation techniques are essential for converting DC voltage to AC voltage at high switching frequency. During this conversion process, the current in the DC link is switched at the same frequency, resulting in a pulsating current in the DC link. This pulsating current comprises two main components: the average DC component supplied by the DC source, and harmonic currents at the switching frequency supplied by the DC capacitor. The DC link capacitor supplies harmonic currents, leading to DC voltage ripple generation. This ripple's magnitude depends on the DC capacitance value. A higher DC voltage ripple necessitates a larger capacitor to maintain ripple within permissible limits. Additionally, the peak-to-peak magnitude of the DC voltage ripple is influenced by the placement of switching states in the PWM within each sampling interval. Each PWM has its own dedicated switching placement pattern. This chapter focuses on analyzing the correlation between switching states and the peak-to-peak magnitude of DC voltage ripple, exploring various PWM techniques for three-phase, two-level inverters as follows.

2.1 Circuit configuration of three-phase, two-level inverter

The basic circuit configuration of a three-phase, two-level voltage source inverter (VSI) feeding a load having impedance Z is shown in Fig. 2.1. The three-phase inverter is powered from the DC source with voltage v_{dc}. The DC link capacitor with capacitance C_{dc} is connected at DC link to provide the alternative path to the DC ripple current. i_a, i_b, i_c denotes the load phase current corresponding to leg a, b, and c. S_a, S_b, S_c are the top switch switching function of the inverter. The top and bottom switches of the corresponding leg of the inverter are complementary to each other. i_s, i_{dc}, and i_c are the DC source current, DC link current, and DC capacitor current.

The three-phase, two-level inverter possesses 8 (2^3) switching states having six active states and two null switching states making the hexagon as shown in Fig. 2.2(a). Here 1(100), 2(110), 3(010), 4(011), 5(001) and 6(101) are the active states, while 0(000) and 7(111) are the null switching states [85]. The switching states divide the hexagon into six sectors as shown in Fig. 2.2(a). Considering the reference space vector lies in sector-I, the switching states 1(100), 2(110) and 0/7(000/111) are applied for the time T_1, T_2 and T_O to generate

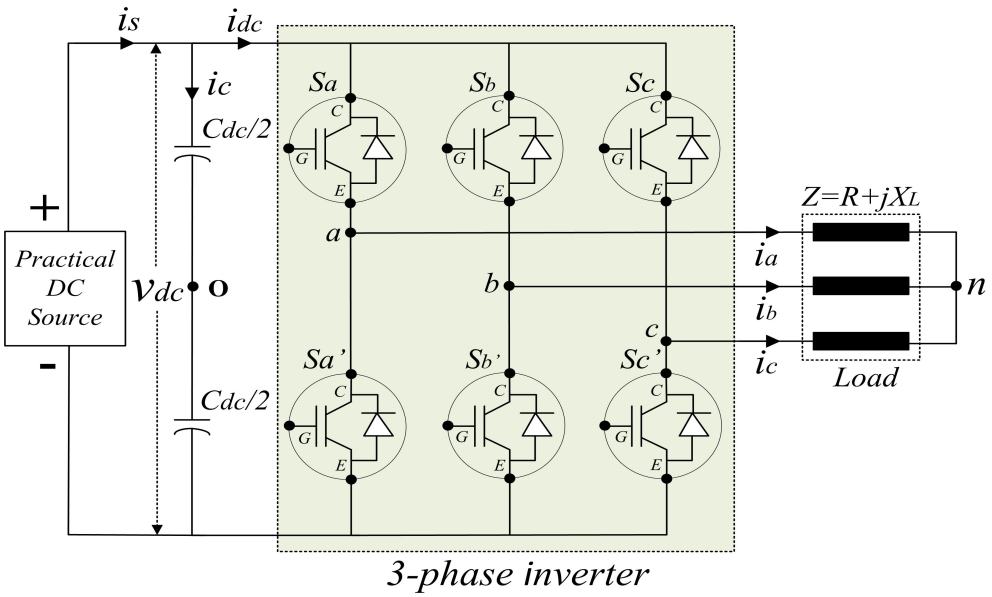


Figure 2.1: Basic circuit configuration of three-phase, two-level inverter

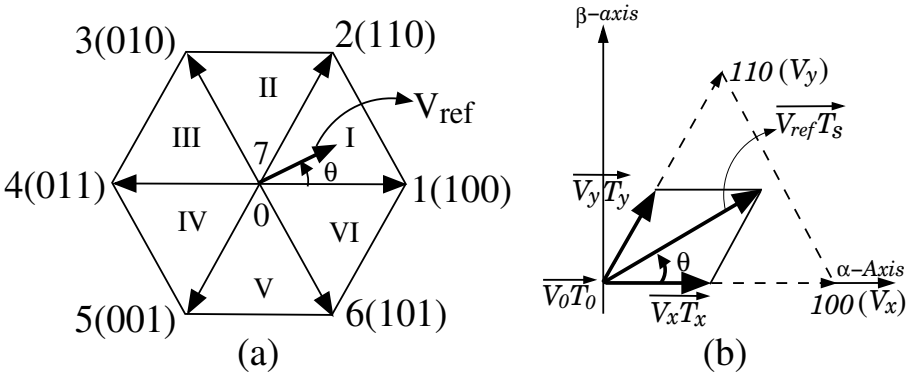


Figure 2.2: Switching states of the three-phase, two-level inverter

the reference space vector V_{ref} at position θ. In order to place the V_{ref} at a particular position, it is necessary to compute the dwell times of the switching states. The dwell times of the switching states can be obtained by applying the volt-sec principle on α and β axes as

$$V_{ref}T_s\cos(\theta) = V_xT_x + V_yT_y\cos(60^o) \tag{2.1}$$

$$V_{ref}T_s\sin(\theta) = V_yT_y\sin(60^o) \tag{2.2}$$

Where θ is the space vector angle and T_s is the sampling time interval ($T_s = 1/F_s$). In sector-I, T_x corresponds to T_1, T_y corresponds to T_2 and T_O corresponds to T_0/T_7. Similarly, in sector-II T_x corresponds to T_2, T_y corresponds to T_3 and T_O corresponds to T_0/T_7. The sum of active and null switching times is equal to T_s and can be expressed as

$$T_s = T_x + T_y + T_O \tag{2.3}$$

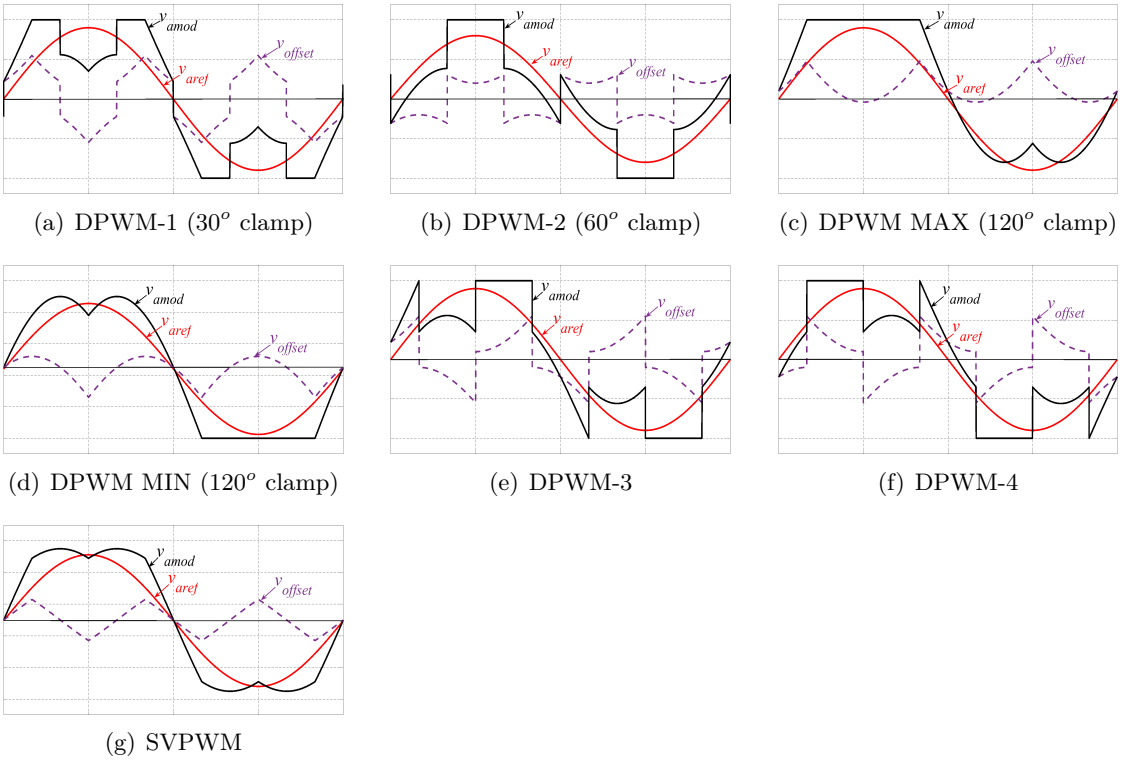
Using (2.1), (2.2) and (2.3), the switching dwell times can be obtained in sector-1 as

$$T_x = T_1 = m_a \sin(60^o - \theta) T_s = T_{max} - T_{int} \tag{2.4}$$

$$T_y = T_2 = m_a \sin(\theta) T_s = T_{int} - T_{min} \tag{2.5}$$

$$T_O = (1 - m_a \cos(30^o - \theta))\, T_s = T_s - (T_{max} - T_{min}) \tag{2.6}$$

Where m_a is the modulation index. T_{max}, T_{min} and T_{int} are the maximum, minimum,



(a) DPWM-1 (30^o clamp) (b) DPWM-2 (60^o clamp) (c) DPWM MAX (120^o clamp)

(d) DPWM MIN (120^o clamp) (e) DPWM-3 (f) DPWM-4

(g) SVPWM

Figure 2.3: Modulating wave (v_{amod}), Reference waves (v_{aref}) and offset wave (v_{offset}) for different discontinuous PWMs and SVPWM

and intermediate time in a sampling time interval expressed as

$$T_{max} = \frac{2T_s}{V_{dc}} MAX(v_{a_{ref}}, v_{b_{ref}}, v_{c_{ref}}) \tag{2.7}$$

$$T_{min} = \frac{2T_s}{V_{dc}} MIN(v_{a_{ref}}, v_{b_{ref}}, v_{c_{ref}}) \tag{2.8}$$

$$T_{int} = -(T_{max} + T_{min}) \tag{2.9}$$

where $v_{a_{ref}}$, $v_{b_{ref}}$, $v_{c_{ref}}$ are the reference voltages corresponding to leg a, b and c of the inverter. The placement of active and null vectors correspond to T_1, T_2, and T_O in a sampling time interval, generating the continuous and discontinuous PWMs. Considering the null vector displacement within a sampling time interval, in this work, six DPWM techniques and one CPWM are realized as mentioned in Table-2.1 for DC voltage ripple analysis. For realized PWMs, the corresponding reference wave variation is shown in Fig. 2.3. The difference between the reference voltage (the average fundamental voltage across the load) and the inverter instantaneous switching voltage generates the error voltage, which decides the DC capacitor current and DC voltage ripple. The DC voltage ripple is

modeled in further sections to understand the effect of the above PWM techniques on the DC bus.

Table 2.1: Switching voltage vectors applied in six sectors for the discontinuous and continuous PWM techniques

Sector		I	II	III	IV	V	VI
DPWM-1	$0^o - 30^0$	012	723	034	745	056	761
	$30^o - 60^0$	721	032	743	054	765	016
DPWM-2	$0^o - 30^0$	721	032	743	054	765	016
	$30^o - 60^0$	012	723	034	745	056	761
DPWM MAX	$0^o - 60^0$	721	723	743	745	765	761
DPWM MIN	$0^o - 60^0$	012	032	034	054	056	016
DPWM-3	$0^o - 60^0$	721	032	743	054	765	016
DPWM-4	$0^o - 60^0$	012	723	034	745	056	761
SVPWM	$0^o - 60^0$	0127	7230	0347	7450	0567	7610

2.2 Mathematical modeling of instantaneous DC capacitor current and DC voltage ripple

In sector-1, the switching states T_1, T_2 and T_0/T_7 are dedicatedly used to synthesize the V_{ref} at the position of θ. In this work, the direct axis (d-axis) is aligned to the V_{ref} while the quadrature axis (q-axis) is 90^o lagging to the V_{ref} as shown in Fig. 2.4.

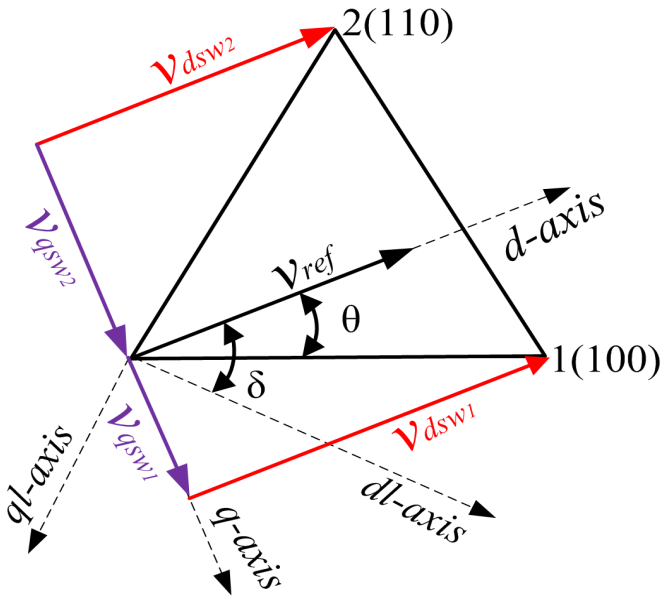


Figure 2.4: Instantaneous projection of switching states on d and q axis

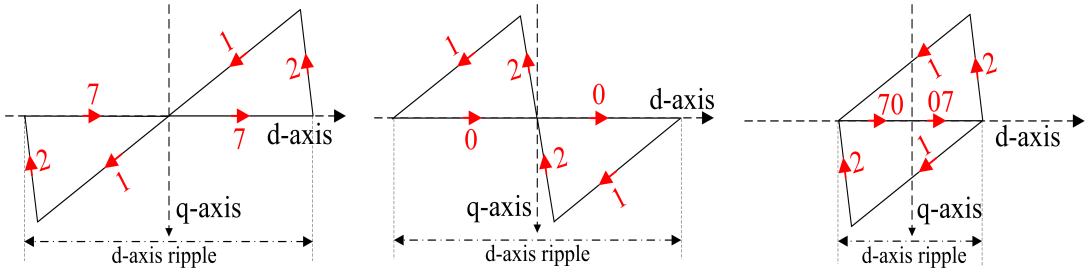
The projection of instantaneous switching states on the d and q axes can be expressed as

$$v_{d_{sw}} = \frac{2}{3}V_{dc}(S_a.\cos(\theta) + S_b\cos(\theta - 120^\circ) + S_c\cos(\theta + 120^\circ)) \tag{2.10}$$

$$v_{q_{sw}} = \frac{2}{3}V_{dc}(S_a.\sin(\theta) + S_b\sin(\theta - 120^\circ) + S_c\sin(\theta + 120^\circ)) \tag{2.11}$$

Where $v_{d_{sw}}$ and $v_{q_{sw}}$ are the instantaneous projection of switching states on the d and q axes. S_a, S_b and S_c are the instantaneous switching states corresponding to inverter legs a, b and c. The projection of switching state 1(100) on the d and q axis can be referred as v_{dsw_1} and v_{qsw_1} while the projection of switching state 2(110) on the d and q axis can be referred as v_{dsw_2} and v_{qsw_2} as shown in Fig. 2.4. The projection of null switching states (0(000)/7(111)) on the d-q axes is zero as the null state is not contributing in generating the output voltages. Similarly, the projection of the fundamental space vector (v_{ref}) on the d and q axes can be expressed as

$$v_{d_{ref}} = v_{ref} = m_a \frac{V_{dc}}{2}; v_{q_{ref}} = 0 \tag{2.12}$$



(a) DPWM-2, DPWM MAX and DPWM-3

(b) DPWM-1, DPWM MIN and DPWM-4

(c) SVPWM

Figure 2.5: Error voltage vector trajectory in d-q plane for different DPWMs and CPWM (SVPWM)

In the case of space vector-based advanced PWM techniques, the linear range of the modulation index (m_a) is 0.866 ($\sqrt{3}/2$). To consider the effect of linear modulation range, the (2.12) can be modified as

$$v_{d_{ref}} = \frac{m_a}{\sqrt{3}/2} \frac{V_{dc}}{2} = \frac{m_a V_{dc}}{\sqrt{3}} \tag{2.13}$$

The error vector is defined as the disparity between the reference space vector and the instantaneous switching vector [10]. The projection of this error vector onto the d and q axes can be formulated as:

$$v_{d_{err}} = v_{d_{ref}} - v_{d_{sw}}; v_{q_{err}} = v_{q_{ref}} - v_{q_{sw}} \tag{2.14}$$

Where $v_{d_{err}}$ and $v_{q_{err}}$ are the d and q axis error voltages. By computing the error voltages on the d and q axes, the error volt-sec trajectory is drawn for DPWM-1, DPWM-2, DPWM MAX, DPWM MIN, DPWM-3, DPWM-4, and SVPWM as shown in Fig. 2.5. From Fig. 2.5 it is observed that the d-axis ripple is lesser in SVPWM while it is higher in all the derived DPWMs in this work. Now, in order to understand the effect of varying loads on

the DC bus voltage ripple, it is necessary to define the length of the load axis (Z) and its deviation from the fundamental reference space vector (θ). The length of the load axis and its deviation can be expressed in the form of load resistance and reactance as

$$Z = r\cos(\delta) + x_l \sin(\delta); \delta = \tan^{-1}\left(\frac{x_l}{r}\right) \tag{2.15}$$

Where Z, r and x_l are the per-phase output impedance, resistance, and reactance. δ denotes the load impedance angle. The equivalent AC impedance reflection on the DC side can be represented as

$$Z_{dc} = (r/m_a)\cos(\delta) + (x_l/m_a)\sin(\delta) \tag{2.16}$$

Where Z_{dc} denotes the equivalent AC impedance seen by the DC bus. From (4.19), it can be observed that when $m_a = 0$, the load isolates itself from the source, and no current flows from the source to load. In this scenario, Z_{dc} is infinite. Similarly, when $m_a = 1$, the AC load directly connected to the DC bus shows AC per phase impedance equal to DC impedance. The projection of the d-axis error and q-axis error on the load-axis gives the idea of analyzing the effect of AC side quantities on the DC domain. To do the DC voltage ripple analysis, two more axis defined as dl and ql. Here "l" specified with the load reference frame. dl-axis is coinciding with the active power consumed by the load while ql axis is coinciding with the reactive power consumed by the load. The projection of instantaneous error on $dl - ql$ axis can be mathematically represented as

$$\begin{bmatrix} v_{dl_{err}} \\ v_{ql_{err}} \end{bmatrix} = \begin{bmatrix} \cos(\delta) & \sin(\delta) \\ -\sin(\delta) & \cos(\delta) \end{bmatrix} \begin{bmatrix} v_{d_{err}} \\ v_{q_{err}} \end{bmatrix} \tag{2.17}$$

Where $v_{dl_{err}}$ and $v_{ql_{err}}$ are the error voltage projection on dl and ql axis. Using (2.10), (2.11), (2.13), (2.14) and (2.17), the error voltages on dl and ql axis can be expanded as

$$\begin{aligned} v_{dl_{err}} &= \frac{m_a V_{dc}}{\sqrt{3}}\cos(\delta) - \frac{2}{3}V_{dc}(S_a\cos(\theta-\delta) + S_b\cos(\theta-\delta-120^o) \\ &\quad + S_c\cos(\theta-\delta-240^o)) \end{aligned} \tag{2.18}$$

$$\begin{aligned} v_{ql_{err}} &= \frac{m_a V_{dc}}{\sqrt{3}}\sin(\delta) - \frac{2}{3}V_{dc}(S_a\sin(\theta-\delta) + S_b\sin(\theta-\delta-120^o) \\ &\quad + S_c\sin(\theta-\delta-240^o)) \end{aligned} \tag{2.19}$$

Using (4.19) and (2.17), the DC capacitor current on dl and ql axis can be expressed as

$$i_{c_{dl}} = \frac{v_{dl_{err}}}{Z_{dc}}; i_{c_{ql}} = \frac{v_{ql_{err}}}{Z_{dc}} \tag{2.20}$$

Expanding (2.20) using (4.19), (2.18) and (2.19) as

$$i_{c_{dl}} = i_c = \frac{\sqrt{3}}{2}\frac{m_a V_{dc}}{\sqrt{r^2 + x_l^2}}(\frac{m_a}{\sqrt{3}}\cos(\delta) - \frac{2}{3}(S_a\cos(\theta-\delta) + S_b\cos(\theta-\delta-120^o) + S_c\cos(\theta-\delta-240^o))) \tag{2.21}$$

$$i_{c_{ql}} = \frac{\sqrt{3}}{2}\frac{m_a V_{dc}}{\sqrt{r^2 + x_l^2}}(\frac{m_a}{\sqrt{3}}\sin(\delta) - \frac{2}{3}(S_a\sin(\theta-\delta) + S_b\sin(\theta-\delta-120^o) + S_c\sin(\theta-\delta-240^o))) \tag{2.22}$$

Where $i_{c_{dl}}$ and $i_{c_{ql}}$ are the dl and ql axis component of DC capacitor current. In real-time, only $i_{c_{dl}}$ component is the actual current flowing through the DC capacitor. Using (2.21), the instantaneous variation of DC bus voltage ripple can be mathematically modeled as

$$\Delta V_{dc} = \frac{1}{C_{dc}}\int i_{c_{dl}}.dt \tag{2.23}$$

$$= \frac{\sqrt{3}}{2C_{dc}}\frac{m_a V_{dc}}{\sqrt{r^2 + x_l^2}}\int(\frac{m_a}{\sqrt{3}}\cos(\delta) - (2/3)[S_a\cos(\theta-\delta) + S_b\cos(\theta-\delta-120^o) + S_c\cos(\theta-\delta-240^o)]).dt \tag{2.24}$$

Where ΔV_{dc} is the instantaneous DC bus voltage ripple corresponding to each switching state. The DC voltage ripple corresponding to timings T_1, T_2 and T_0 can be written as

$$\Delta V_{dc(T_1)} = \frac{\sqrt{3}}{2C_{dc}}\frac{m_a^2 V_{dc}}{\sqrt{r^2 + x_l^2}}(\frac{m_a}{\sqrt{3}}\cos(\delta) - (2/3)[\cos(\theta-\delta)]).\sin(60^o-\theta)\,T_s \tag{2.25}$$

$$\Delta V_{dc(T_2)} = \frac{\sqrt{3}}{2C_{dc}}\frac{m_a^2 V_{dc}}{\sqrt{r^2 + x_l^2}}(\frac{m_a}{\sqrt{3}}\cos(\delta) - (2/3)[\cos(\theta-\delta) + \cos(\theta-\delta-120^o)])\sin(\theta)\,T_s \tag{2.26}$$

$$\Delta V_{dc(T_O)} = \frac{1}{2C_{dc}}\frac{m_a^2 V_{dc}}{\sqrt{r^2 + x_l^2}}(1 - m_a\cos(30^o-\theta)).\cos(\delta)T_s \tag{2.27}$$

With the above-mentioned voltage ripple slopes, the peak-to-peak DC bus voltage ripple can be obtained as

$$\Delta V_{pp} = max(|\Delta V_{dc(T_1)}|, |\Delta V_{dc(T_2)}|, |\Delta V_{dc(T_O)}|) \tag{2.28}$$

where ΔV_{pp} is the peak to peak DC bus voltage ripple in a sapling time interval (T_s). From

(2.24), it is observed that the DC voltage ripple has a strong dependency on the modulation index (m_a) and load impedance angle (δ). To understand the effect of different PWMs on the DC voltage ripple, two conditions are considered where $\delta = 30^o$ (resistance dominant load) and $\delta = 60^o$ (inductor dominant load) as mentioned in a subsequent section.

2.3 Comparison of Different PWM techniques with respect to DC bus voltage ripple

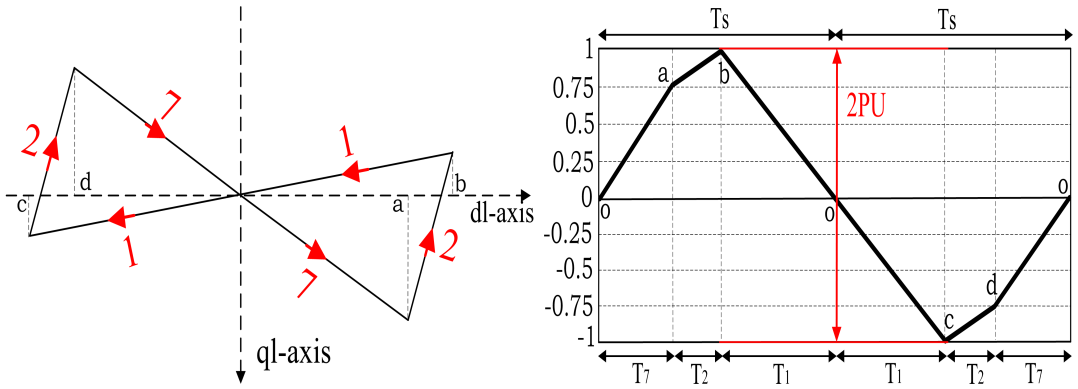
The instantaneous variation of DC capacitor current on $dl-$axis gives the actual DC bus voltage ripple for any inverter topology. As observed from the (2.24), the instantaneous variation of DC voltage ripple is the function of the switching states. The placement of switching states decides the peak-to-peak DC bus voltage ripple. For analyzing the DC voltage ripple, two load compositions are considered. The first load composition is adjusted towards the resistance dominating load, and the load angle is kept at 30^o.

2.3.1 At $\delta = 30^o$ (Resistance dominating load)

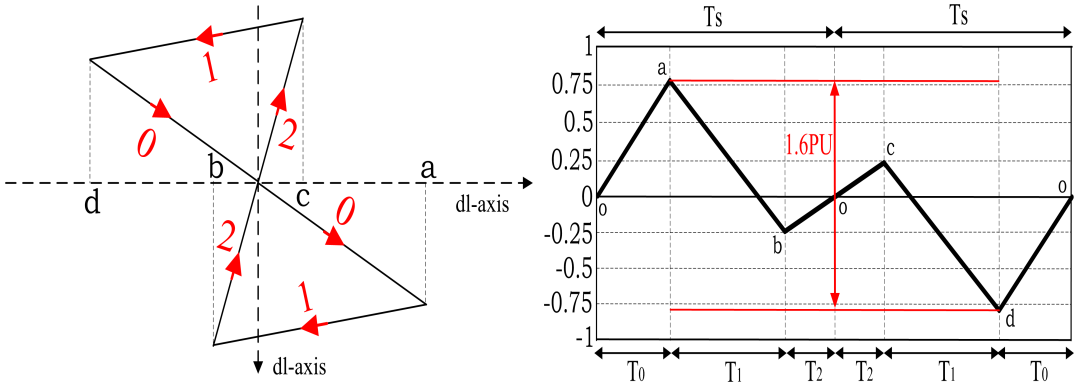
At $\delta = 30^o$, the load power factor axis ($dl-$ axis) is phase lag to the d-axis at 30^o and the projection of d-q error vector trajectory (shown in Fig. 2.5) on $dl - ql$ plane is shown in Fig. 2.6 (left). The corresponding projection of the error voltage trajectory on the $dl-$axis is shown in Fig. 2.6 (right). From Fig. 2.6, it is observed that in sector-1, the DPWM-2, DPWM MAX and DPWM-3 gives the maximum DC voltage ripple of 2 p.u. as shown in Fig. 2.6(a) (right). The DPWM-1, DPWM MIN and DPWM-4 gives the moderate DC voltage ripple (1.6 p.u.) as shown in Fig. 2.6(b) (right) while SVPWM generates the minimum DC voltage ripple (1.3 p.u.) as shown in Fig. 2.6(c) (right).

In sector-2, the error voltage trajectory on $dl - ql$ plane is shown in Fig. 2.7 (left) and the corresponding DC voltage ripple is shown in Fig. 2.7 (right). In sector-2, it is observed that the peak-to-peak DC bus voltage ripple is higher in DPWM-2, DPWM MIN and DPWM-3 of magnitude 2 p.u. (as shown in Fig. 2.7(b)), moderate in DPWM-1, DPWM MAX and DPWM-4 of magnitude 1.6 p.u. (as shown in Fig. 2.7(a)) and minimum in SVPWM of magnitude 1.3 p.u. (as shown in Fig. 2.7(c)). From the above analysis, it is observed that DPWM-MAX give the highest DC bus voltage ripple in sectors 1, 3, and 5, while it gives a moderate DC voltage ripple in sectors 2, 4, and 6. Similarly, DPWM MIN gives the highest DC bus voltage ripple in sectors 2, 4, and 6 while it gives a moderate DC voltage ripple in sectors 1, 3, and 5 at $\delta = 30^o$. From the above analysis, it is observed that the SVPWM gives the lowest DC bus voltage ripple at $\delta = 30^o$. The sector-wise p.u. DC bus voltage ripple variation is tabulated in Table-2.2 for all the PWM techniques mentioned in this work.

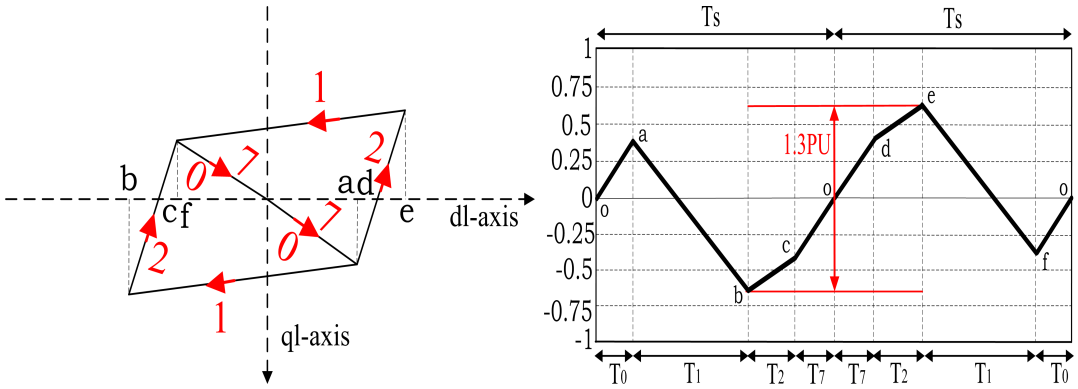
From Table-2.2, the minimum DC voltage ripple in SVPWM indicates that the SVPWM gives better performance of DC voltage ripple for the load having lesser δ compared to all DPWMs.



(a) DPWM-2,DPWM MAX and DPWM-3

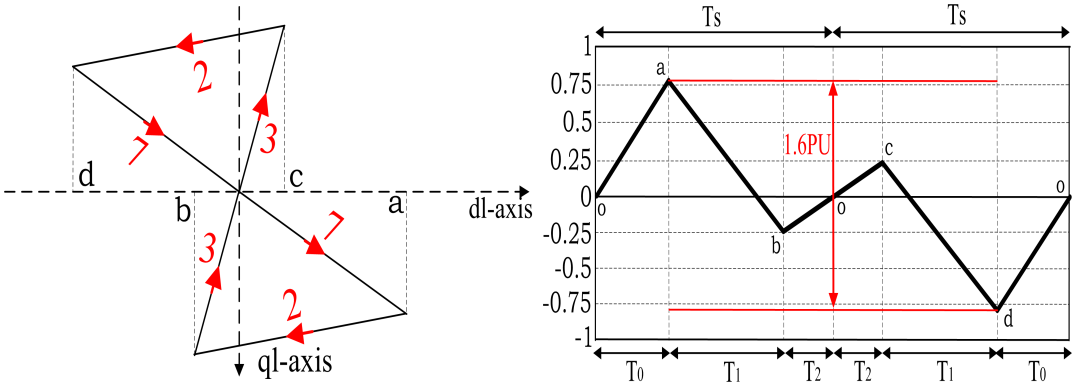


(b) DPWM-1,DPWM MIN and DPWM-4

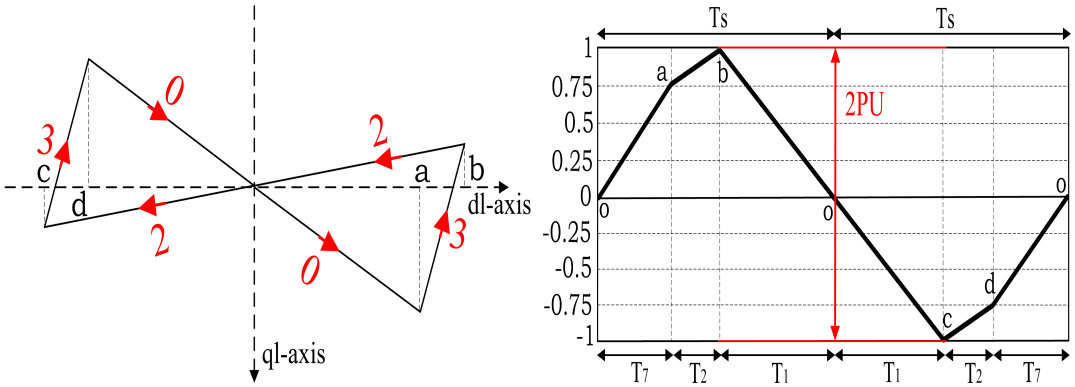


(c) SVPWM

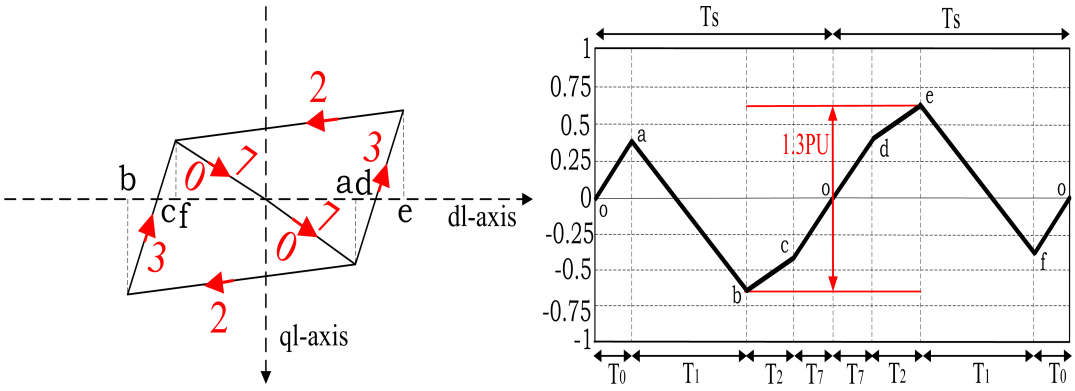
Figure 2.6: Error voltage vector trajectory in $dl - ql$ plane (left) with peak to peak DC voltage ripple (right) at $\theta = 15^o$ and $\delta = 30^0$ in sector-1



(a) DPWM-1,DPWM MAX and DPWM-4



(b) DPWM-2,DPWM MIN and DPWM-3



(c) SVPWM

Figure 2.7: Error voltage vector trajectory in $dl - ql$ plane (left) with peak to peak DC voltage ripple (right) at $\theta = 15^o$ and $\delta = 30^0$ in sector-2

Table 2.2: Sector-wise p.u. DC voltage ripple variation for DPWMs and SVPWM at $\theta = 15^o$ and $\delta = 30^o$

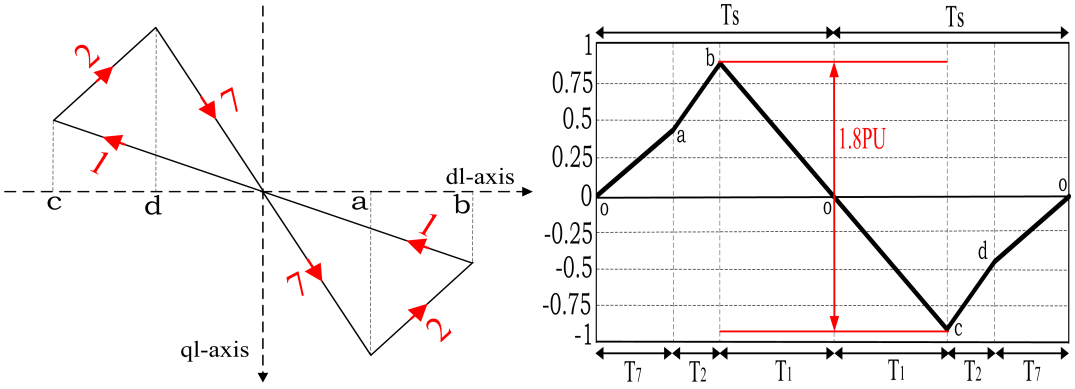
Sector		I	II	III	IV	V	VI	MAX(I, II, III, IV, V, VI)
DPWM-1	$0^o - 30^o$ $30^o - 60^o$	1.6 2	1.6 2	1.6 2	1.6 2	1.6 2	1.6 2	 2
DPWM-2	$0^o - 30^o$ $30^o - 60^o$	2 1.6	2 1.6	2 1.6	2 1.6	2 1.6	2 1.6	2
DPWM MAX	$0^o - 60^o$	2	1.6	2	1.6	2	1.6	2
DPWM MIN	$0^o - 60^o$	1.6	2	1.6	2	1.6	2	2
DPWM-3	$0^o - 60^o$	2	2	2	2	2	2	2
DPWM-4	$0^o - 60^o$	1.6	1.6	1.6	1.6	1.6	1.6	2
SVPWM	$0^o - 60^o$	1.3	1.3	1.3	1.3	1.3	1.3	1.3

2.3.2 At $\delta = 60^o$ (Inductor dominating load)

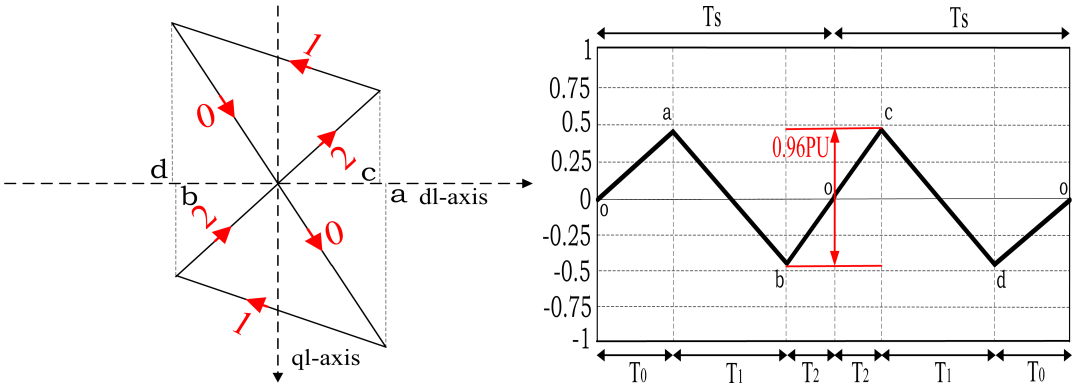
From the above analysis, it is observed that the DPWM-1, DPWM-2, DPWM MAX, DPWM MIN, and DPWM-3 produce the same DC bus voltage ripple in a fundamental cycle of load voltage. Due to this, DPWM-3, DPWM-4, and SVPWM are considered for the further analysis of DC voltage ripple at $\delta = 60^o$. At $\delta = 60^o$, the load axis is shifted from the reference space vector (V_{ref}) by 60^o. The error volt-sec trajectory on $dl - ql$ plane is shown in Fig. 2.8(a)(left) for DPWM-3, Fig. 2.8(b)(left) for DPWM-4 and Fig. 2.8(c)(left) for SVPWM. The projection of error volt-sect trajectory on $dl-$axis gives the DC bus voltage ripple as shown in Fig. 2.8 (right). From Fig. 2.8, it is observed that the DC bus voltage ripple is highest in DPWM-3 of magnitude 1.8 p.u. (shown in Fig. 2.8(a)(right)), moderate in SVPWM of magnitude 1.3 p.u. (shown in Fig. 2.8(c)(right)), and minimum in DPWM-4 of magnitude 0.96 p.u. (shown in Fig. 2.8(b)(right)). The sector-wise p.u. DC bus voltage ripple variation is tabulated in Table-2.3 for all the PWM techniques mentioned in this work. It is observed from Table-2.3 that the DPWM-4 generates the minimum DC bus voltage ripple at $\delta = 60^o$ compared to all discontinuous and continuous PWMs.

The variation of DC bus voltage ripple with respect to modulation index for all the mentioned PWM techniques by keeping the switching frequency constant for all the PWMs is shown in Fig. 2.9(a) for $\delta = 30^o$ and in Fig. 2.9(b) for $\delta = 60^o$.

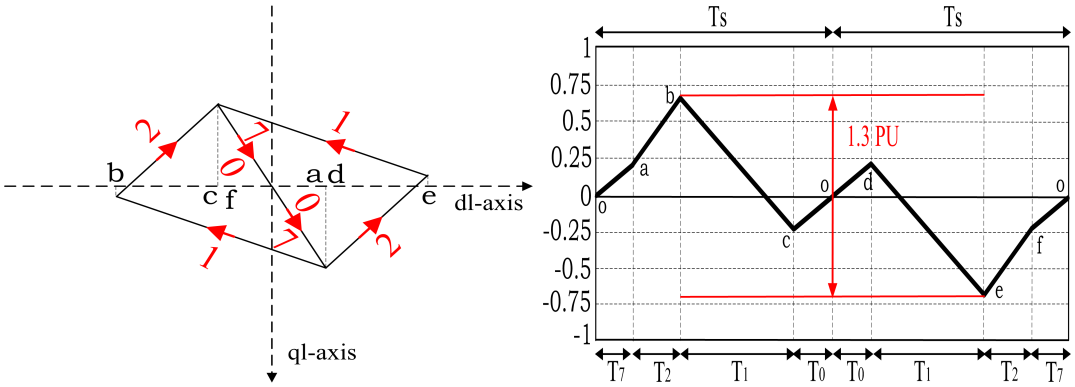
From Fig. 2.9 it is observed that the peak-to-peak DC voltage ripple (ΔV_{pp}) increases when the modulation index (m_a) increases. From Fig. 2.9(a) it can be observed that at $\delta = 30^o$, the SVPWM produces minimum DC bus voltage ripple at all modulation indexes (m_a). Similarly, it is also observed From Fig. 2.9(b) that at $\delta = 60^o$, the SVPWM generates the minimum DC voltage ripple from $m_a = 0.1$ to $m_a = 0.4$, while DPWM-4 generates the minimum DC bus voltage from $m_a = 0.4$ to $m_a = 1$. The above analysis shows that the SVPWM is suitable for the lower δ while the DPWM-4 is suitable for the higher delta with higher m_a. Considering discontinuous PWMs, DPWM-4 will generate



(a) DPWM-3



(b) DPWM-4

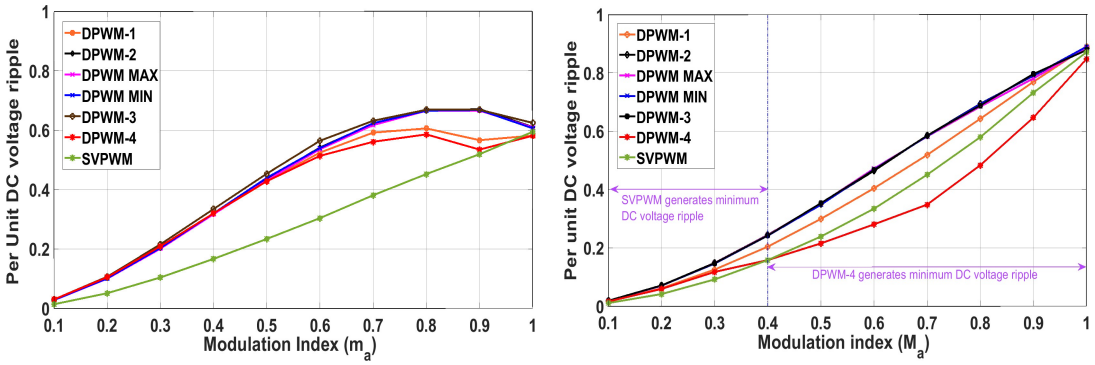


(c) SVPWM

Figure 2.8: Error voltage vector trajectory in $dl - ql$ plane (left) with peak to peak DC voltage ripple (right) at $\theta = 15^o$ and $\delta = 60^0$ in sector-1

Table 2.3: Sector-wise p.u. DC voltage ripple variation for DPWMs and SVPWM at $\theta = 15^o$ and $\delta = 60^o$

Sector		I	II	III	IV	V	VI	MAX(I, II, III, IV, V, VI)
DPWM-1	$0^o - 30^o$ $30^o - 60^o$	0.96 1.8	0.96 1.8	0.96 1.8	0.96 1.8	0.96 1.8	0.96 1.8	1.8
DPWM-2	$0^o - 30^o$ $30^o - 60^o$	1.8 0.96	1.8 0.96	1.8 0.96	1.8 0.96	1.8 0.96	1.8 0.96	1.8
DPWM MAX	$0^o - 60^o$	1.8	0.96	1.8	0.96	1.8	0.96	1.8
DPWM MIN	$0^o - 60^o$	0.96	1.8	0.96	1.8	0.96	1.8	1.8
DPWM-3	$0^o - 60^o$	1.8	1.8	1.8	1.8	1.8	1.8	1.8
DPWM-4	$0^o - 60^o$	0.96	0.96	0.96	0.96	0.96	0.96	0.96
SVPWM	$0^o - 60^o$	1.3	1.3	1.3	1.3	1.3	1.3	1.3



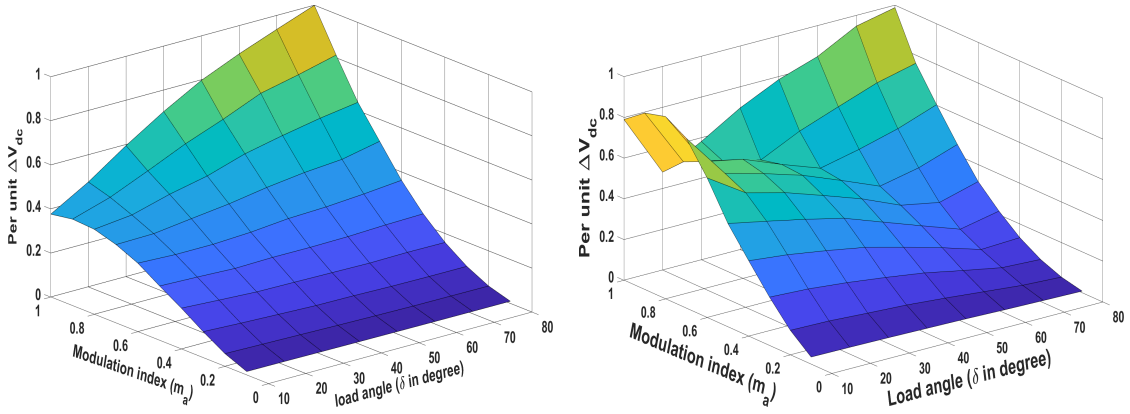
(a) at $\delta = 30^o$ (b) at $\delta = 60^o$

Figure 2.9: Peak to peak DC voltage ripple variation for different PWM techniques with respect to modulation index (m_a)

the lowest DC bus voltage ripple as compared to all DPWMs at all load angles (δ) and modulation index (m_a). From the above analysis, it is observed that only SVPWM and DPWM-4 give a lesser DC bus voltage ripple at different conditions.

The 3D plot of DC voltage ripple with respect to modulation index (m_a) and load angle (δ) are shown in Fig. 2.10(a) and Fig. 2.10(b). Using 3D plots, the region of operation for SVPWM and DPWM-4 is defined as shown in Fig. 2.11. Fig. 2.11 specified the regions for PWM techniques which give the minimum DC bus voltage ripple. In Fig. 2.11, the orange area shows that in this region SVPWM generates the minimum DC bus voltage ripple while the blue area shows that in this region DPWM-4 gives the minimum DC bus voltage ripple. Based on the analysis, the characteristics shown in Fig. 2.11 are divided into three regions:

- Region-1: This region is in between $\delta = 0^o$ to $\delta = 30^o$. In this region, only SVPWM generates the minimum DC bus voltage ripple.



(a) SVPWM (b) DPWM-4

Figure 2.10: Variation of DC voltage ripple with respect to modulation index (m_a) and load angle (δ)

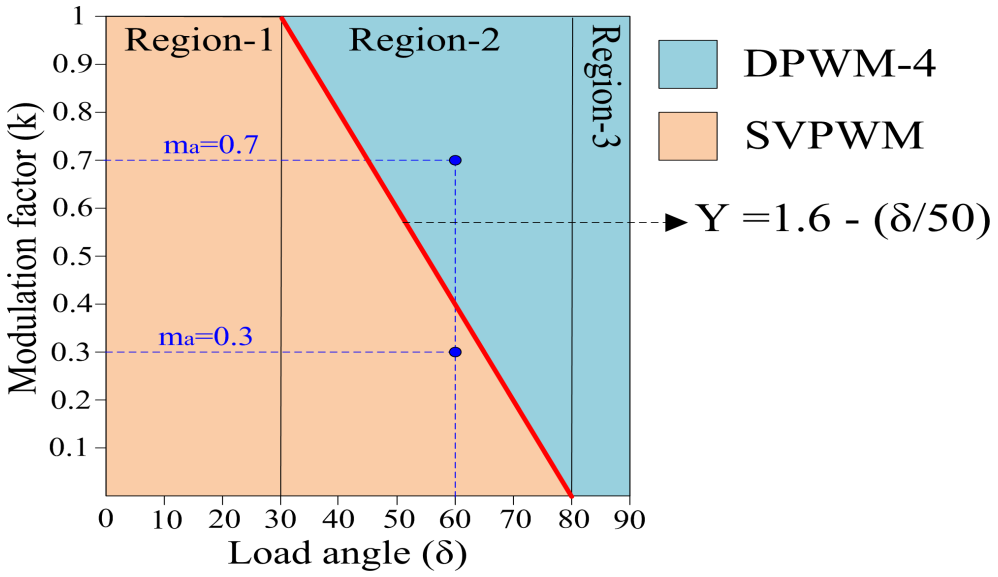


Figure 2.11: Region of PWM operation to get the minimum DC bus voltage ripple

- Region-2: This region is in between $\delta = 30^o$ to $\delta = 80^o$. In this region, SVPWM as well as DPWM-4 generates the minimum DC bus voltage ripple. The red line divides the SVPWM region and DPWM-4 region. The slope of the line is defined as $Y = 1.6 - (\delta/50)$. If the modulation index is lesser than Y then SVPWM is selected for switching the inverter. Otherwise, DPWM-4 is selected for switching the inverter.

- Region-3: This region is in between $\delta = 80^o$ to $\delta = 90^o$. In this region, only DPWM-4 generates the minimum DC bus voltage ripple.

From Fig. 2.11, it is observed that the SVPWM generates a minimum DC voltage ripple when the δ is lesser while at a higher δ, the DPWM-4 gives the minimum DC voltage ripple.

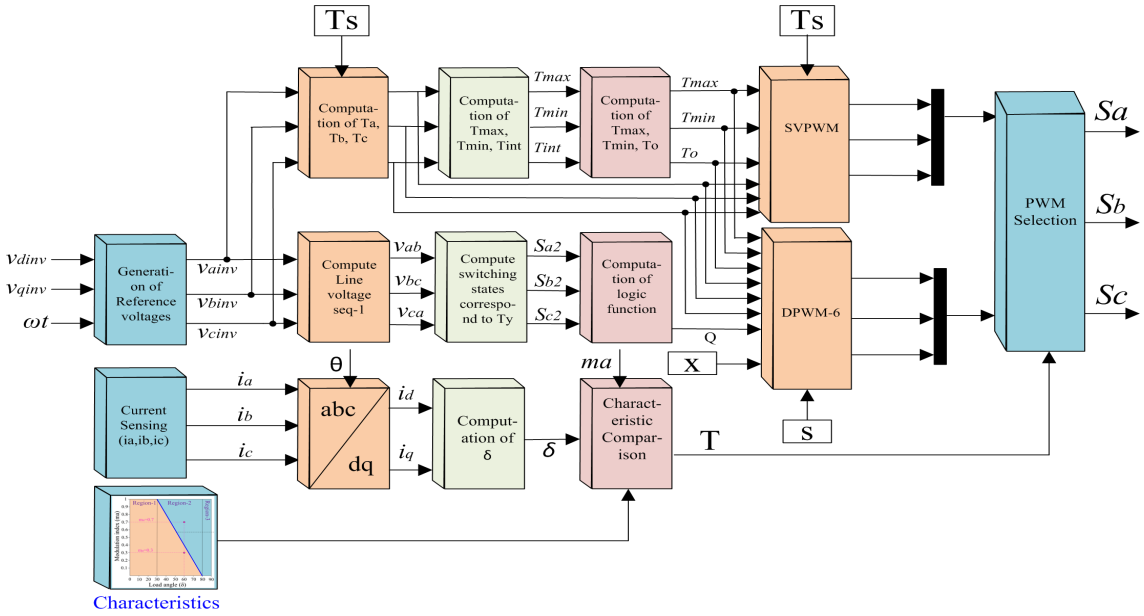


Figure 2.12: Algorithm of region-based PWM selection for minimized DC voltage ripple

2.3.3 Algorithm of region-based PWM selection for minimized DC voltage ripple

To select the PWM techniques based on the characteristics shown in Fig. 2.11, an algorithm is developed to minimize the DC voltage ripple. The step-wise block diagram of the algorithm is shown in Fig. 2.12. The detailed step of the algorithm is explained below.

Step-1: This step includes the generation of reference waves based on the m_a and θ.

$$v_{a_{ref}} = (1/2)m_a V_{dc}\cos(\theta)$$
$$v_{b_{ref}} = (1/2)m_a V_{dc}\cos(\theta - (2\pi/3))$$
$$v_{c_{ref}} = (1/2)m_a V_{dc}\cos(\theta - (4\pi/3))$$

Step-2: Computation of line sequence-2

$$V_{ab} = v_{a_{ref}} - v_{b_{ref}}$$
$$V_{bc} = v_{b_{ref}} - v_{c_{ref}}$$
$$V_{ca} = v_{c_{ref}} - v_{a_{ref}}$$

Step-3: Computation of switching states corresponding to T_2

if V_{ab}=+ve then $S_{a_2} = 1$ else $S_{a_2} = 0$
if V_{bc}=+ve then $S_{b_2} = 1$ else $S_{b_2} = 0$
if V_{ca}=+ve then $S_{c_2} = 1$ else $S_{c_2} = 0$

Step-4: Computation of logic function Q

$$Q = S_{a_2}.S_{b_2} + S_{b_2}.S_{c_2} + S_{c_2}.S_{a_2}$$

Step-5: Computation of timings corresponding to reference sine waves

$$T_{as} = v_{a_{ref}}(T_s/V_{dc})$$
$$T_{bs} = v_{b_{ref}}(T_s/V_{dc})$$
$$T_{bs} = v_{c_{ref}}(T_s/V_{dc})$$

Step-6: Computation of T_{max}, T_{min} and T_o

$$T_{max} = Max(T_{as}, T_{bs}, T_{cs})$$
$$T_{max} = Min(T_{as}, T_{bs}, T_{cs})$$
$$T_o = T_s - (T_{max} - T_{min})$$

Step-7: Generation of PWM techniques

- SVPWM

if $T_o >= 0$ **then**
  $T_{offset} = 0.5T_o - T_{min}$
  $S_a = T_{as} + T_{offset}$
  $S_b = T_{bs} + T_{offset}$
  $S_c = T_{cs} + T_{offset}$
else
  $T_{offset} = -T_{min}$
  $S_a = (T_{as} + T_{offset})(T_s/(T_{max} - T_{min}))$
  $S_b = (T_{bs} + T_{offset})(T_s/(T_{max} - T_{min}))$
  $S_c = (T_{cs} + T_{offset})(T_s/(T_{max} - T_{min}))$
end

- DPWM-4

if $Q == 1$ **then**
  $T_{offset} = -T_{min}$
  $S_a = T_{as} + T_{offset}$
  $S_b = T_{bs} + T_{offset}$
  $S_c = T_{cs} + T_{offset}$
else
  $T_{offset} = T_o - T_{min}$
  $S_a = T_{as} + T_{offset}$
  $S_b = T_{bs} + T_{offset}$
  $S_c = T_{cs} + T_{offset}$
end

Step-8: Sensing the output three-phase currents

Step-9: Transferring three-phase current into d-q quantities and computation of load angle (δ)

$$i_d = i_a \cos(\theta) + i_b \cos(\theta - 120^o) + i_c \cos(\theta - 240^o)$$
$$i_q = i_a \sin(\theta) + i_b \sin(\theta - 120^o) + i_c \sin(\theta - 240^o)$$
$$\delta = \tan^{-1}(i_q/i_d)$$

Step-10: Defining the region of operation

if $\delta <= 30^o$ **then**
 | Y==1;
else
 | **if** $\delta >= 80^o$ **then**
 | | Y=0;
 | **else**
 | | $m_{a_1} = (\delta/50) - 0.6$
 | | **if** $m_a >= m_{a_1}$ **then**
 | | | Y=1;
 | | **else**
 | | | Y=0
 | | **end**
 | **end**
end

Step-11: If Y==1 then pass SVPWM else pass DPWM-4

2.4 Results and Discussion

The proposed regional-based DC voltage ripple minimization algorithm is validated on the lab-developed prototype shown in Fig. 4.11. The experimental setup consists of semikron IGBT switches (SKM75GB12T4) based inverter, gate driver circuits, and AC loads. The proposed algorithm is implemented on the C2000 (TMS320F28379D) microcontroller interfaced with the gate drive circuit for triggering the inverter by taking the current feedback through the current sensor (LEM-LA55P).

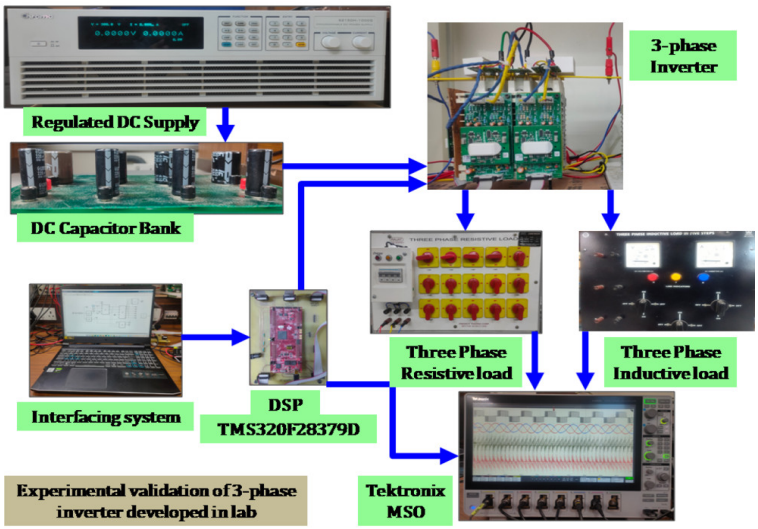
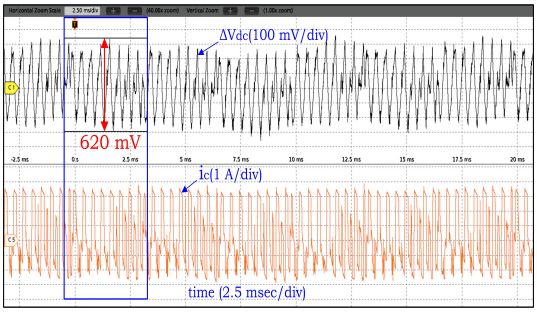


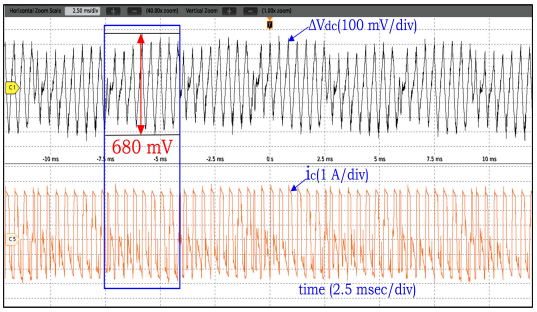
Figure 2.13: The lab experimental connection diagram of three-phase, two-level inverter with DSP control board and interfacing systems

The operating parameters of the prototype for validating the proposed algorithm are tabulated in Table-2.4.

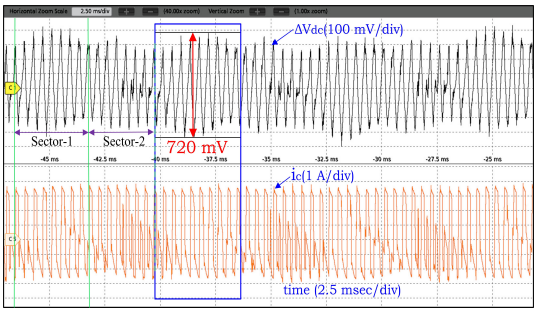
The variations of different reference wave patterns shown in Fig. 2.3 are generated using



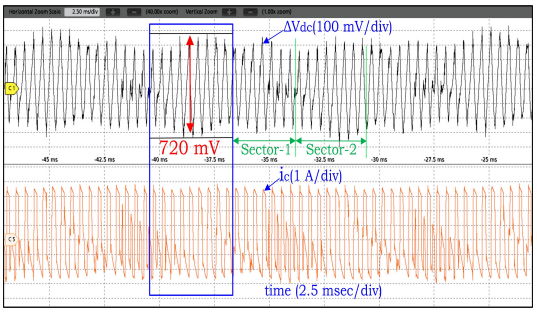
(a) DPWM-1



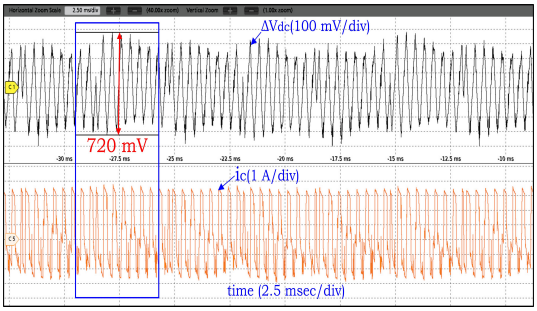
(b) DPWM-2



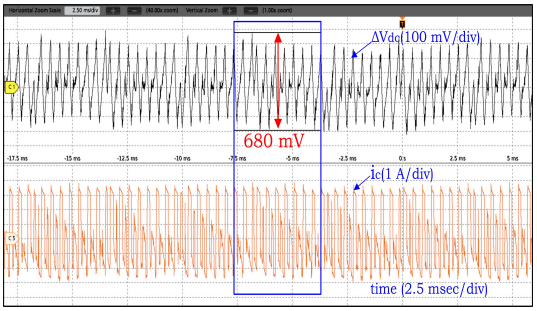
(c) DPWM MAX



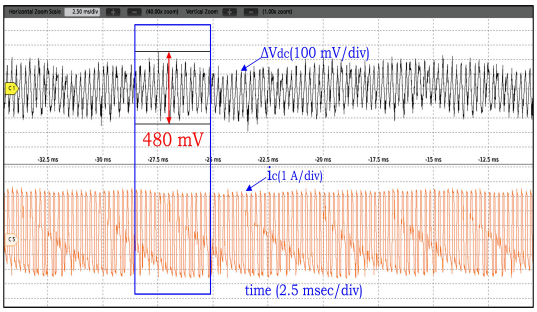
(d) DPWM MIN



(e) DPWM-3

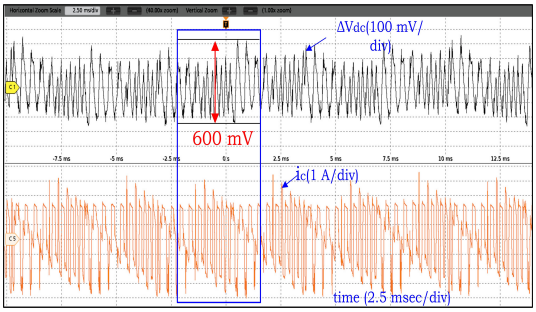


(f) DPWM-4

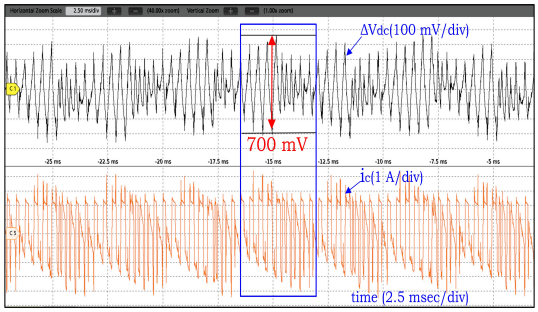


(g) SVPWM

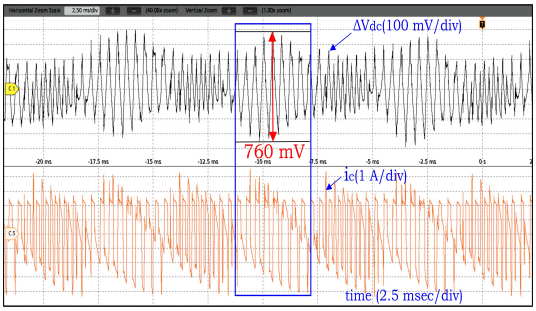
Figure 2.14: Variation of DC voltage ripple (top trace) and DC capacitor current (bottom trace) at $\delta = 30^o$ and $m_a = 0.7$



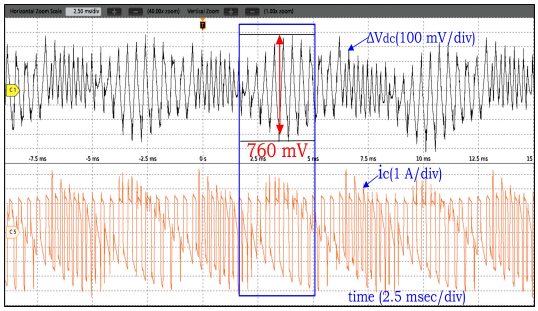
(a) DPWM-1



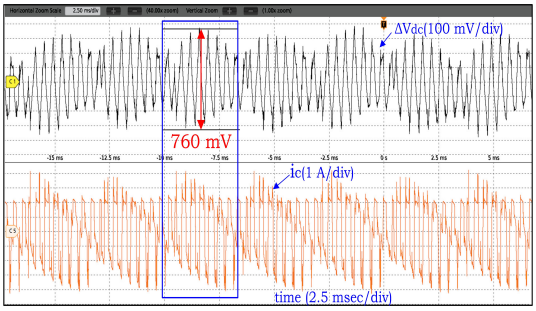
(b) DPWM-2



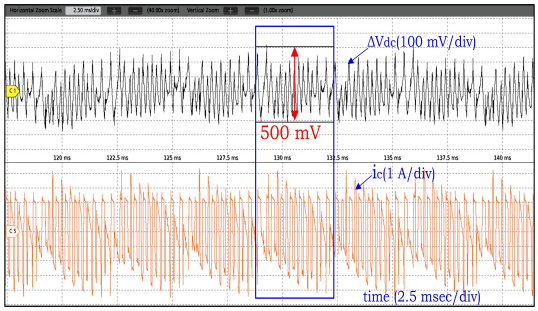
(c) DPWM MAX



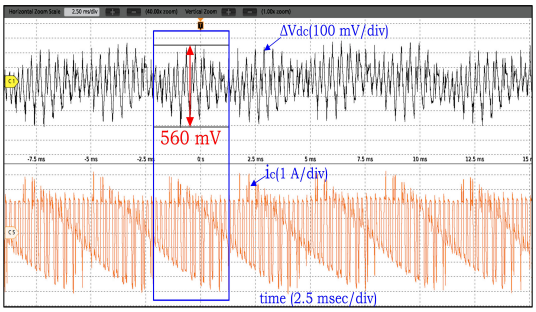
(d) DPWM MIN



(e) DPWM-3



(f) DPWM-4



(g) SVPWM

Figure 2.15: Variation of DC voltage ripple (top trace) and DC capacitor current (bottom trace) at $\delta = 60^o$ and $m_a = 0.7$

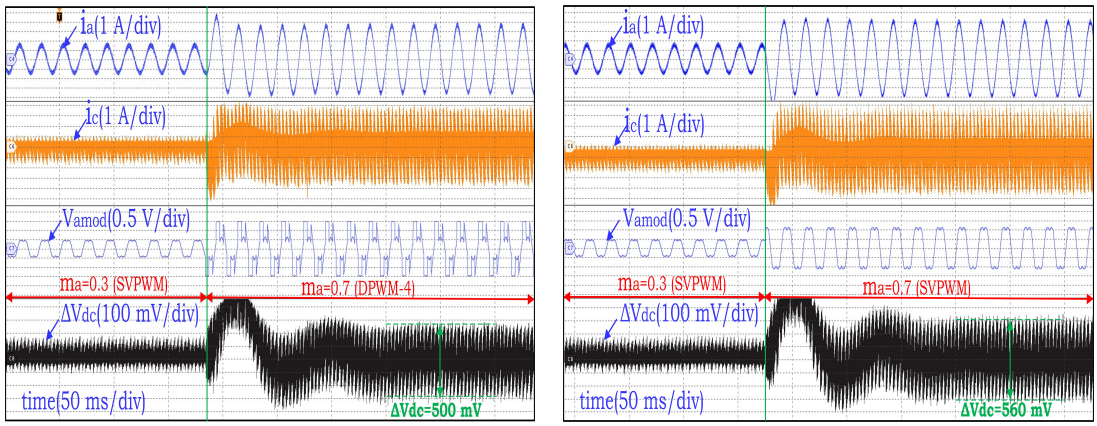
Table 2.4: Experimental operating parameter of grid-connected inverter

Parameters	Symbol	Values	Units
Power	P	1.26	kW
DC bus voltage	V_{dc}	600	V
Fundamental frequency	F_o	50	Hz
Switching Frequency	F_s	2400	Hz
DC link capacitor	C_{dc}	600	uf
Load Resistance	$r(\delta = 30^0)$	52	Ω
Load Inductance	$l(\delta = 30^0)$	96	mH
Load Resistance	$r(\delta = 60^0)$	30	Ω
Load Inductance	$l(\delta = 60^0)$	166	mH

DSP C2000 (TMS320F28379D) to elicit continuous and discontinuous PWMs. For all generated PWMs (continuous and discontinuous) mentioned in the previous section, the DC bus voltage ripple and capacitor current ripple behaviors at different power factor angles (δ =30°) and (δ =60°) are shown in Fig. 2.14 and Fig. 2.15 respectively. At $m_a = 0.7$, it is observed From Fig. 2.14 that all the discontinuous PWM give higher DC bus voltage ripple (DPWM-1 (ΔV_{dc} = 620 mV), DPWM-2 (ΔV_{dc} = 680 mV), DPWM MAX (ΔV_{dc} = 720 mV), DPWM MIN (ΔV_{dc} = 720 mV), DPWM-3 (ΔV_{dc} = 720 mV), DPWM-4 (ΔV_{dc} = 680 mV)) while the SVPWM gives minimum DC bus voltage ripple of 480 mV. Further, it can be seen from Fig. 2.14(c), that the DPWM MAX and DPWM MIN give different voltage ripples at different sectors due to clamping and non-clamping regions as highlighted in the third and fourth row of Table-2.2. However, at lower power factor angles, the SVPWM yields the minimum DC bus voltage ripple in all the sectors as evident from Fig. 2.14.

On the other hand, the hardware results shown in Fig. 2.15 at m_a =0.7 and δ =60°clearly indicate that the peak-to-peak DC bus voltage ripple is minimum in DPWM-4 (500 mV as shown in Fig. 2.15(f)), moderate in DPWM-1 and SVPWM (600 mV and 560 mV as shown in Fig. 2.15(a) and Fig. 2.15(g)) and maximum in DPWM-2, DPWM MAX, DPWM MIN and DPWM-3 (700 mV, 760 mV, 760 mV and 760 mV as shown in Fig. 2.15(b), Fig. 2.15(c), Fig. 2.15(d) and Fig. 2.15(e) respectively). From the experimental results depicted in Fig. 2.14 and Fig. 2.15, it is clearly evident that the δ variations reflected in the change of DC voltage ripple correspond to PWM techniques used as substantiated theoretically in section-2.3.1 and 2.3.2. It clearly shows that, the requirement of transition from SVPWM to DPWM-4 with the increase in δ for optimum voltage ripple realization adaptive to the load variation. The corresponding transition of the PWMs with a change in load is depicted in Fig. 2.16.

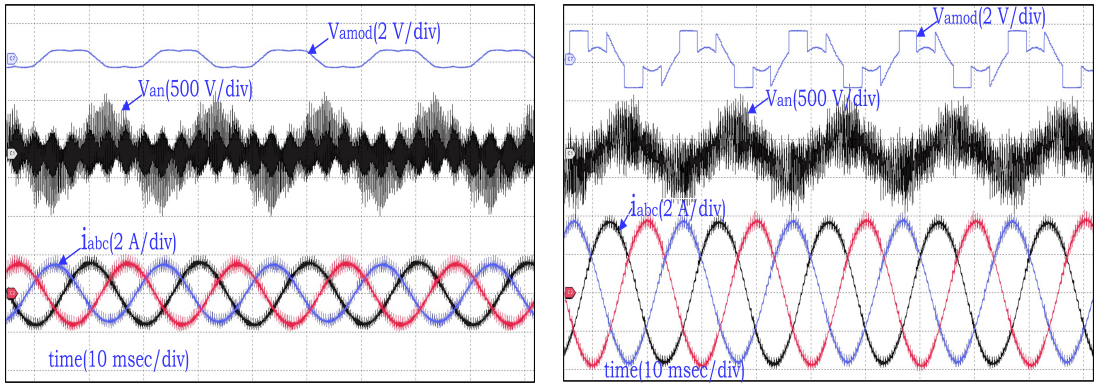
From Fig. 2.16, it is visible that at δ =60°, with the change m_a from 0.3 to 0.7, the selection of PWM adaptively changes from SVPWM to DPWM-4. With the change to DPWM-4, the DC bus voltage ripple is 500 mV as shown in the bottom trace of Fig.



(a) (b)

Figure 2.16: Variation of phase current (top trace), DC capacitor current (second trace), Modulating wave (third trace), and DC voltage ripple (bottom trace) for selection of PWM based on region-based characteristics for the transition of $m_a = 0.3$ to $m_a = 0.7$ at $\delta = 60^o$.

2.16(a). Whereas with SVPWM thought the change in m_a, the voltage ripple at m_a=0.7 is observed as 560 mV as shown in Fig. 2.16(b). With the adaptive change of PWMs corresponding to the m_a, the realized phase voltage, and phase current are depicted in Fig. 2.17. From Fig. 2.17, it is evident that the realized current across the load with both SVPWM and DPWM-4 is sinusoidal in nature. Finally, it can be concluded that with the change in m_a and δ the DC bus voltage ripple can be minimized with the corresponding selection of PWMs as proposed in this work.



(a) $m_a = 0.3$ (SVPWM) (b) $m_a = 0.7$ (DPWM-4)

Figure 2.17: Variation of modulating wave (top trace), phase voltage (middle trace), and three-phase current (bottom trace) for $m_a = 0.3$ (SVPWM) and $m_a = 0.7$ (DPWM-4).

2.5 Conclusion

In this work, the region of operation of different DPWMs and CPWMs is identified for three-phase, two-level VSI, considering the minimum DC voltage ripple criterion. To identify the region of operation, the DC capacitor current is mathematically modeled using

the computation of error voltage on d-q axes and then the projection of error voltage on $dl - ql$ axes. The DC capacitor current on the dl axis gives the actual DC capacitor current. Using the DC capacitor current on dl-axis, the DC voltage ripple is modeled. Using a mathematical model of DC voltage ripple, the discontinuous PWMs (DPWMs) and continuous PWMs (CPWMs) are analyzed in the direction of minimum DC voltage ripple for $\delta = 30^o$ and $\delta = 60^o$. After analysis, it is found that the DPWM-4 and SVPWM only generate the minimum DC voltage ripple. Based on the analysis, the region of operation of SVPWM and DPWM-4 is identified using modulation index (m_a) and load impedance angle (δ). Using the region of operation, an algorithm is developed to adaptively select the PWM technique for minimizing the DC voltage ripple.The experimental result shows that the SVPWM generates the lesser DC bus voltage ripple of 480 mV at $\delta = 30^o$ while DPWM-4 generates the minimum DC voltage ripple of 500 mV at $\delta = 60^o$.

Chapter 3

Minimum DC Voltage Ripple Switching Sequence Elicitation for Dual Inverter

In recent years, the dual inverter configuration with a common DC link has gained significant attention for applications in both motor drives and grid-connected solar inverters. This configuration is notable for its ability to generate the required AC voltage while maintaining lower DC bus potentials compared to conventional setups [11]. In three-phase two-level based solar inverters, higher input DC voltage is achieved by connecting solar panels in series, which can lead to Potential Induced Degradation (PID) in large-scale installations. This is due to elevated system voltages and specific environmental conditions. PID negatively affects the performance and lifespan of solar panels [86]. The dual inverter, with its common DC link, requires a lower DC bus voltage to achieve the same output voltage, thereby reducing the PID effect and extending the solar panel lifespan. Despite the higher switch count in dual inverters for solar applications, which increases system costs, the cost of solar panels outweighs the cost of inverters significantly. Moreover, in motor drive applications, the surplus of switching devices in dual inverters allows for the elimination of common-mode voltage using CMV-eliminated PWM techniques. This enhances operational flexibility, especially in systems employing a common DC bus [11]-[12]. Considering the applicability of the dual inverter with a wide range of applications, this chapter extends the DC voltage ripple analysis to the dual inverter with varying power factor angles.

3.1 A single stage dual inverter configuration with common DC bus

The circuit configuration of the dual inverter with common DC link is shown in Fig. 3.1. The two 3 phase 2 level inverter are connected back to back to make the dual inverter. An open end load is connected between the inverter-1 and inverter-2 with resistance (r) and reactive impedance (x_l). s_a is the inverter-1 switching function corresponding to phase-a, s_b is the inverter-1 switching function corresponding to phase-b and s_c is the inverter-1 switching function corresponding to phase-c. Similarly, s'_a, s'_b, s'_c are referring to inverter-2 a'-phase, b'-phase and c'-phase switching states. In both the inverters, each

pole switching state varies between 1 (ON) and 0 (OFF), and the pole's top switch is instantaneous complementary to the bottom switch.

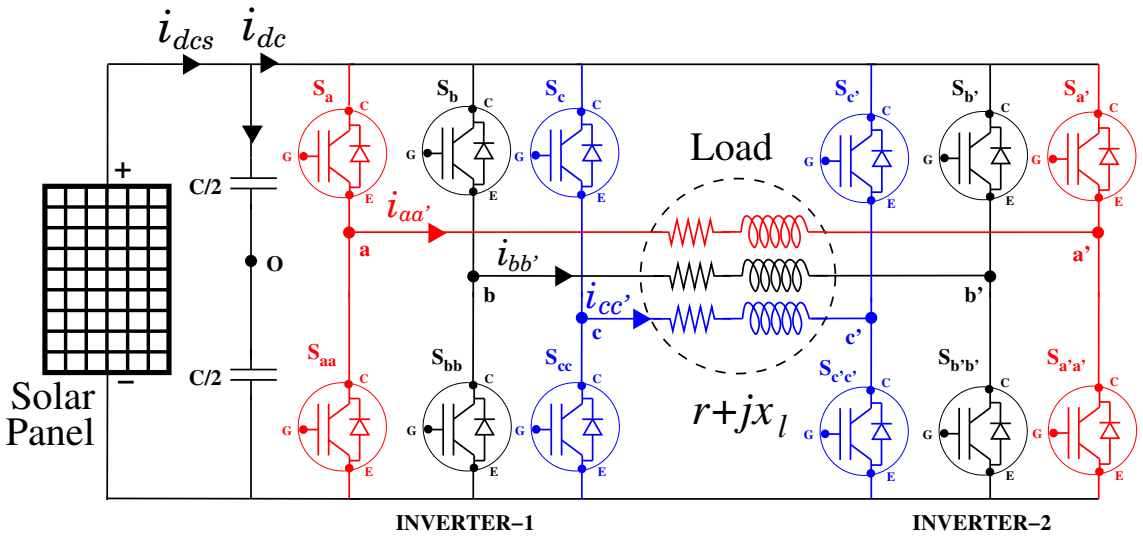


Figure 3.1: The solar-powered dual inverter configuration with common DC bus

The dual inverter switched in the average sense using the instantaneous switching state. While switching in the average sense, the individual inverter generates the common mode voltage. The difference between the common mode voltage of the individual inverter defines the overall common mode voltage of the dual inverter. The common mode voltage analysis is presented in the subsequent subsection.

3.1.1 Common Mode Voltage

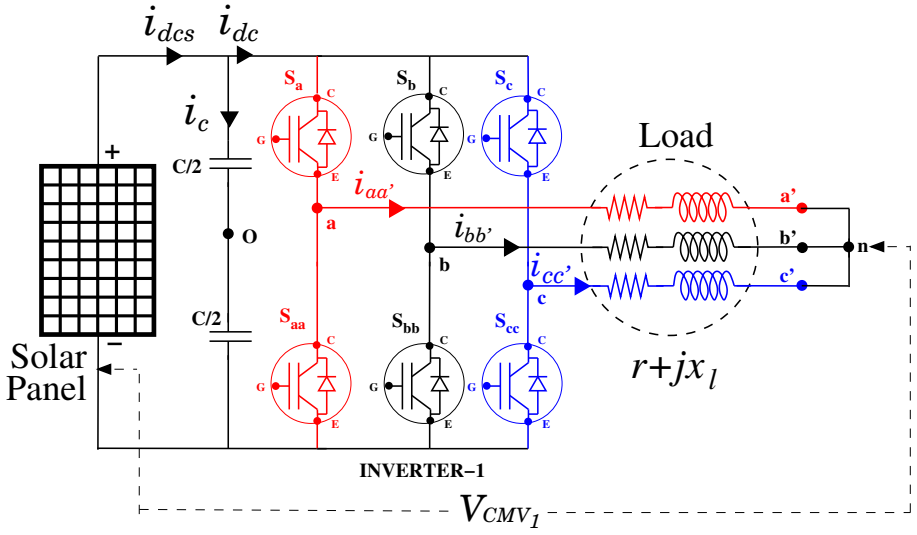


Figure 3.2: Circuit configuration to compute the common mode voltage of the inverter-1 in a dual inverter configuration

Depending upon the switching state selection to realize the load space vector, the magnitudes of the common-mode voltage variation can be computed in a dual inverter by taking the difference of the common mode voltage of the inverter-1 and inverter-2.

The common mode voltage is the voltage which is present between the load neutral and the DC capacitor bank mid-point or negative terminal of the DC bus. In this chapter, negative terminal of the DC bus is used to measure the common mode voltage. The dual inverter with the common DC link uses the open end load. Thus to compute the common mode voltage of the dual inverter with single DC link, the common mode voltage of the individual inverter should be computed firstly. Consider the circuit where inverter-2 forms the neutral as shown in Fig. 3.2. From Fig. 3.2, the common mode voltage for the inverter-1 can be computed as

$$V_{CMV_1} = \frac{V_{dc}(s_a + s_b + s_c)}{3} \tag{3.1}$$

Where V_{CMV_1} is the common mode voltage of the inverter-1 measured between the neutral point "n" and DC bus negative terminal. If a leg top switch is ON then $S_a = 1$ and if it OFF then $S_a = 0$ in (3.1). Similarly follows for leg b and c. Using (3.1), the common mode voltage of inverter-1 is computed and tabulated in Table-3.1.

Table 3.1: Common mode voltage of inverter-1 corresponding to eight switching states

Switching states	8(000)	1(100)	2(110)	3(010)	4(011)	5(001)	6(101)	7(111)
V_{CMV_1}	0	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	V_{dc}

Similarly, to compute the common mode voltage of the inverter-2, the circuit configuration is as shown in Fig. 3.3.

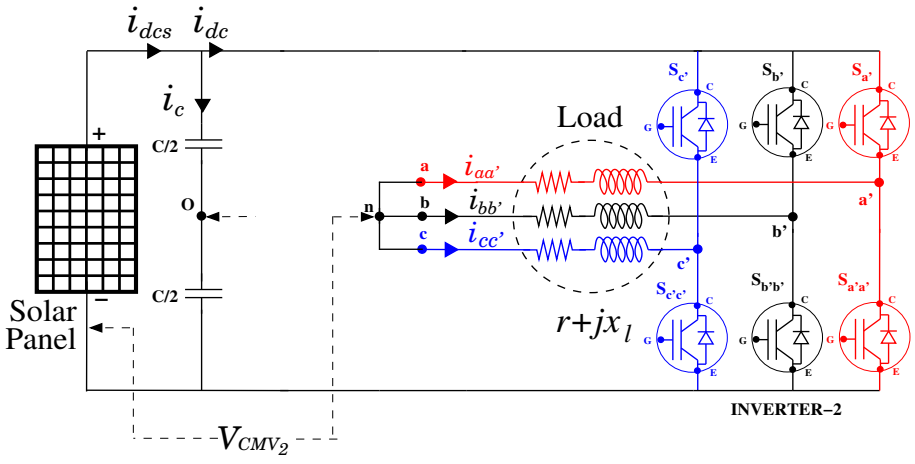


Figure 3.3: Configuration to compute the common mode voltage of the inverter-2 in a dual inverter

From Fig. 3.3, the common mode voltage for the inverter-2 can be computed as

$$V_{CMV_2} = \frac{V_{dc}(s_{a'} + s_{b'} + s_{c'})}{3} \tag{3.2}$$

Using (3.2), the common mode voltage of inverter-2 can be tabulated as

The common mode voltage of the dual inverter is the difference between the common

Table 3.2: Common mode voltage of inverter-2 corresponding to eight switching states

Switching states	8'(000)	1'(100)	2'(110)	3'(010)	4'(011)	5'(001)	6'(101)	7'(111)
V_{CMV_2}	0	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	V_{dc}

mode voltage of the individual inverter which can be expressed using (3.1) and (3.2) as;

$$V_{CMV} = V_{CMV_1} - V_{CMV_2} = V_{dc}\frac{((s_a - s'_a) + (s_b - s'_b) + (s_c - s'_c))}{3} \tag{3.3}$$

Where V_{CMV} is the common mode voltage of the dual inverter. Each inverter in a dual inverter posses the 8 (2^3) switching state. Hence the total 64 ($8 \times 8 = 64$) switching combination is possible in the case of dual inverter which is tabulated in Table-3.3 along with there common mode voltage.

Table 3.3: Common mode voltage of dual inverter corresponding to 64 switching states

Switching states	8(000)	1(100)	2(110)	3(010)	4(011)	5(001)	6(101)	7(111)
8'(000)	0	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	V_{dc}
1'(100)	$\frac{-V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$
2'(110)	$\frac{-2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$
3'(010)	$\frac{-V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$
4'(011)	$\frac{-2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$
5'(001)	$\frac{-V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$
6'(101)	$\frac{-2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$
7'(111)	$-V_{dc}$	$\frac{-2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	0

The dual inverter with common DC link can only operate with the switching states that gives the zero common mode voltage. In this chapter, the exclusive switching locations/states with zero common-mode voltages are used to make the reference voltage space vector (V_{ref}). The space spread of the zero common-mode voltage yield switching locations is shown in Fig. 3.4.

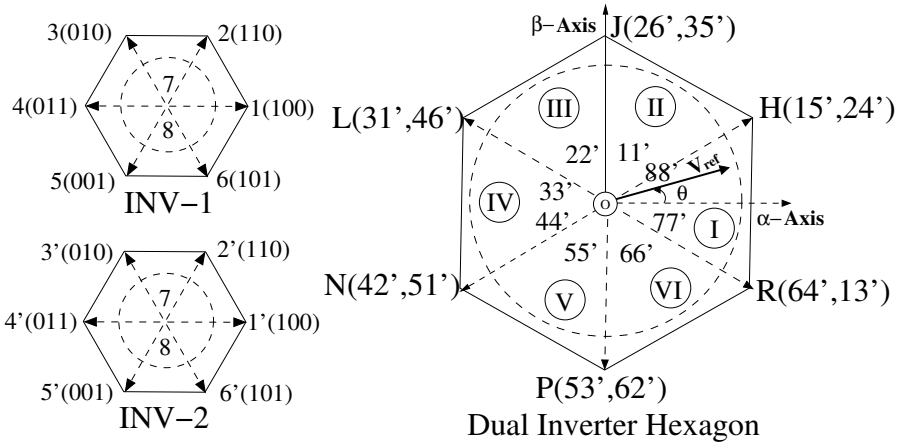


Figure 3.4: On the left, the switching vector positions of Inverter-1 and Inverter-2 are depicted, while on the right, the dual inverter's zero common-mode voltage (CMV) illustrates the switching space vector locations.

To operate the dual inverter effectively, calculating the switching dwell time for its switching states is essential. The procedure for computing the switching dwell time is detailed in the following subsection.

3.1.2 Switching Dwell Time Computation

The primary objective of the dual inverter configuration is to realize the load reference voltage space vector defined as:

$$\overrightarrow{V_{ref}} = m_a.V_{dc}e^{j\theta} \tag{3.4}$$

Where $\overrightarrow{V_{ref}}$ is the fundamental reference space vector of the dual inverter, m_a is the modulation index, V_{dc} is the DC bus voltage and θ is the phase shift of the $\overrightarrow{V_{ref}}$ from α axis as shown in right side figure of Fig. 3.4. But, due to insufficient switching resources, the VSIs synthesize the demanded space vector in an average sense by equating the volt-sec of the load space vector and inverter switching vectors in a sampling time interval (T_s) as:

$$\overrightarrow{V_{ref}}T_s = V_xT_x + V_y.T_y + V_0T_0 \tag{3.5}$$

Here V_x, V_y and V_0 are the switching vectors of the dual inverter configuration can be derived depending upon the dual inverter switching states as:

$$\overrightarrow{V_{sw}} = V_{dc}[(s_a - s'_a)e^{j0} + (s_b - s'_b)e^{(-j120^0)} + (s_c - s'_c)e^{j120^0}] \tag{3.6}$$

In (3.4), m_a controls the magnitude of output fundamental space vector. θ is the rotational angle of the space vector. From the identified space locations HJLNPR (active) O (null) shown in Fig. 3.4, it is evident that the load space vector can be realized in an average sense with two active vector (V_x and V_y) and null vector (V_0) as depicted in (3.5). The space vector position in a hexagon shown in Fig. 3.4 decides the selection of active and null vectors. For instance of load space vector in sector-1, the V_x and V_y depicted in (3.5) represent V_R and V_H respectively. Whereas in sector-2, V_H become V_x, and V_J equal to V_y (referring to Fig. 3.4). Along with the active and null vectors, the corresponding dwell times of the switching vector play a crucial role in the realization of the load space vector in a sampling time interval (T_s). In this work, the dwell times (T_x, T_y and T_0) of the active switching vectors V_x, V_y and null vector V_0 respectively computed by considering $T_x + T_y + T_0 = T_s$ as:

$$T_x = m_a \sin(n.60^0 - \theta)T_s \tag{3.7}$$

$$T_y = m_a \sin(\theta - (n-1)60^0)T_s \tag{3.8}$$

$$T_0 = T_s - (T_x + T_y) \tag{3.9}$$

Here n varies from 1 to 6 depending upon the load space vector position. Since the load space vector realization is accomplished in an average sense with available switching states of the inverter, the error voltage at the AC side contributes to the instantaneous load current. The computational method of deriving the DC voltage ripple through

instantaneous AC load error voltage space vector prediction is explained elaborately in the subsequent section.

3.2 Modelling of DC voltage ripple through instantaneous AC load error voltage

The selection of the switching states with zero common-mode voltage to realize the load space vector ($\overrightarrow{V_{ref}}$) in the average sense is demonstrated in the preceding section. The common-mode voltage elimination gives the flexibility to operate the dual inverters with the common DC bus, as shown in Fig. 3.1. Thus, the single DC capacitor bank is sufficient to handle the dual inverter's switching stress and the load's reactive power requirement. In this work, the DC capacitor instantaneous current model is derived considering the load space vector ($\overrightarrow{V_{ref}}$) in the synchronous reference frame. In a synchronous reference frame, the load space vector composed of three-phase voltages can be represented as:

$$v_d = m_a V_{dc}(\cos^2\theta + \cos^2(\theta - \frac{2\pi}{3}) + \cos^2(\theta + \frac{2\pi}{3})) = \frac{3}{2} m_a V_{dc} \tag{3.10}$$

$$v_q = m_a V_{dc}(\sin(\theta)\cos(\theta) + \sin(\theta - \frac{2\pi}{3})\cos(\theta - \frac{2\pi}{3}) + \sin(\theta + \frac{2\pi}{3}))\cos(\theta + \frac{2\pi}{3})) = 0 \tag{3.11}$$

It indicates that V_{ref} is always aligned with the d-axis irrespective of the position of the load vector. Thus, the V_{ref} projection on q-axis is zero. The $\overrightarrow{V_{ref}}$ is synthesized in an average sense using the instantaneous switching states as demonstrated in the preceding section. The switching vector's instantaneous subtended components on the d-and q-axis are computed as:

$$v_{d_{sw}} = V_{dc}((s_a - s'_a).\cos(\theta) + (s_b - s'_b)\cos(\theta - 120^0) + (s_c - s'_c)\cos(\theta + 120^0)) \tag{3.12}$$

$$v_{q_{sw}} = V_{dc}((s_a - s'_a).\sin(\theta) + (s_b - s'_b)\sin(\theta - 120^0) + (s_c - s'_c)\sin(\theta + 120^0)) \tag{3.13}$$

For an instance, the space vector ($\overrightarrow{V_{ref}}$) is in first sector shown in Fig. 3.5(a) is realized in average sense using the active ('R' ,'H') and null ('O') switching locations. In this realization, the active switching locations projections on dq-axes computed using (3.12) and (3.13) can be identified as V_{dR} and V_{qR} (with 'R'), V_{dH} and V_{qH} (with 'H') respectively as depicted in Fig. 3.5(a). As it is shown in Fig. 3.5(a), $\overrightarrow{V_{ref}}$ aligned and rotate synchronously with d-axis, the AC fundamental frequency appear to be DC quantity in d-q reference frame. Thus instantaneous switching components derived using (3.12) and (3.13) helps to derive the instantaneous error voltage in the d-q axes as:

$$\overrightarrow{V_{err_d}} = \overrightarrow{v_d} - \overrightarrow{v_{d_{sw}}}, \quad \overrightarrow{V_{err_q}} = \overrightarrow{v_q} - \overrightarrow{v_{q_{sw}}} \tag{3.14}$$

Although the load space vector V_{ref} is aligned with the d-axis, the fundamental current drawn by the load is influenced by the load power factor. Thus it is necessary to consider the load power factor to map the AC error voltages onto the DC side. Therefore, in this

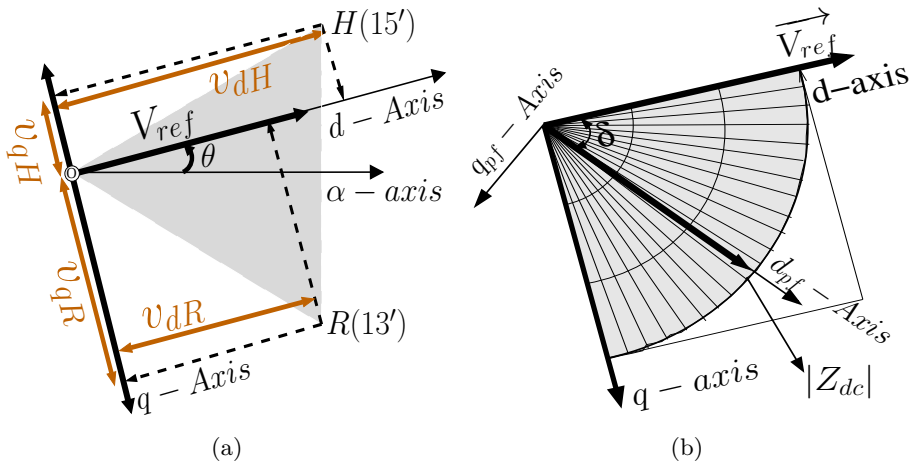


Figure 3.5: (a) The realization of Switching location projection on d-q axis while synthesizing V_{ref} in sector-1 (b) The load power factor references ($d_{pf} - q_{pf}$) realization using load impedance information

work, the reference power factor axis is derived from the AC load real and reactive power information, as shown in Fig. 3.5(b). In Fig. 3.5(b), the resistance correspond to real power (r) aligned with the d-axis and reactance correspond to reactive component (x_l) aligned with q-axis. Using the (2.15), (4.19), (2.17) and (2.20), the DC capacitor current of the dual inverter can be expressed as:

$$i_{dc} = \frac{m_a V_{dc} \sin(\delta)}{x_l}[(S_a - S_{a'})\cos(\theta - \delta) + (S_b - S_{b'})\cos(\theta - \delta - 120) + (S_c - S_{c'})\cos(\theta - \delta + 120)] \tag{3.15}$$

The DC bus current is composed of the average mean current superimposed with the ripple current. In the ideal scenario of sufficient DC bus capacitance, the ripple current contributed by the capacitor and average current drawn from the DC source, the average current (i_{dcs}) can be computed in a sampling time interval using:

$$i_{dcs} = \frac{1}{T_s}\int_0^{T_s} i_{dc}.dt = \frac{i_{dc_x}T_x + i_{dc_y}T_y}{T_s} \tag{3.16}$$

Further, substituting (3.7), (3.8) and (3.15) in (3.16) yield to

$$\begin{aligned} i_{dcs} &= (\frac{m_a^2 V_{dc} sin(\delta)}{x_l}T_s)[(\cos(\theta - \delta) - \cos(\theta - \delta - 120^o))\sin(n.60^o - \theta) + (\cos(\theta - \delta) - \cos(\theta \\ &\quad - \delta - 120^o)).\sin(\theta - (n-1)60^o)] \\ &= \frac{3m_a^2 V_{dc}.\cos^2(\delta)}{2r} \end{aligned} \tag{3.17}$$

The ripple current supported by the capacitor can be computed by subtracting the average

current i_{dcs} (3.17) from total DC link current i_{dc} (3.15) as:

$$\begin{aligned} i_{c_{d_{pf}}} &= i_{dcs}(Avg\ source\ current) - i_{dc}(DC\ link\ current) \\ &= \frac{3m_a^2 V_{dc}\cos^2(\delta)}{2r} - \frac{m_a V_{dc}\sin(\delta)}{x_l} F_{d_{pf}}(.) \\ &= \frac{m_a}{\sqrt{r^2+x_l^2}} \underbrace{(\underbrace{\frac{3}{2}m_a V_{dc}\cos(\delta)}_{v_d\ on\ d_{pf}-axis} - \underbrace{V_{dc}F_{d_{pf}}(.)}_{v_{dsw}\ on\ d_{pf}-axis})}_{V_{err}projection\ on\ d_{pf}-axis(V_{errd_{pf}})} \end{aligned} \tag{3.18}$$

$$F_{d_{pf}}(.) = [(f(sa))\cos(\theta-\delta) + (f(sb))\cos(\theta-\delta-120) + (f(sc))\cos(\theta-\delta+120)]$$

Similarly the $i_{c_{q_{pf}}}$ computed from the error voltage projection on q_{pf} as:

$$i_{c_{q_{pf}}} = \frac{m_a}{\sqrt{r^2+x_l^2}} \underbrace{(\underbrace{\frac{3}{2}m_a V_{dc}\sin(\delta)}_{v_d\ on\ q_{pf}-axis} - \underbrace{V_{dc}F_{q_{pf}}(.)}_{v_{q_{sw}}\ on\ q_{pf}-axis})}_{V_{err}projection\ on\ q_{pf}-axis\ \ (V_{errq_{pf}})} \tag{3.19}$$

$$F_{q_{pf}}(.) = [(f(sa))\sin(\theta-\delta) + (f(sb))\sin(\theta-\delta-120) + (f(sc))\sin(\theta-\delta+120)]$$

Here $f(sa)$, $f(sb)$ and $f(sc)$ represents the VSI's (dual inverter) instantaneous switching state. Using (3.18) and (3.19), the capacitor current vector can be computed as:

$$\overrightarrow{i_c} = i_{c_{d_{pf}}} + j i_{c_{q_{pf}}} = \frac{m_a}{\sqrt{r^2+x_l^2}}(V_{errd_{pf}} + jV_{errq_{pf}}) \tag{3.20}$$

With the computed $\overrightarrow{i_c}$, the instantaneous ripple voltage across the DC bus can be computed as:

$$\overrightarrow{\Delta V_{dc}} = \frac{1}{C_{dc}}\int_0^{T_{sw}} \overrightarrow{i_c}.dt \tag{3.21}$$

$$\Delta V_{dc_{d_{pf}}} = \frac{m_a}{C_{dc}|Z|}\int_0^{T_{sw}} V_{errd_{pf}}.dt \tag{3.22}$$

$$\Delta V_{dc_{q_{pf}}} = \frac{m_a}{C_{dc}|Z|}\int_0^{T_{sw}} V_{errq_{pf}}.dt \tag{3.23}$$

From (3.22) and (3.23), it is evident that, the error voltage vector on the power factor axes, encapsulate the DC bus voltage ripple. Further, it can be reiterate that, the DC bus voltage ripple exactly matches with the $\Delta V_{dc_{d_{pf}}}$ computed using (3.22). For easy understanding, the DC voltage ripple elicitation through the proposed mathematical computational procedure for a dual inverter in a sampling time interval is shown in Fig 3.6. For voltage ripple realization, the load space vector ($\overrightarrow{V_{ref}}$) is assumed to be positioned in a sector-1. The space vector in sector-1 is realized in an average sense using the switching

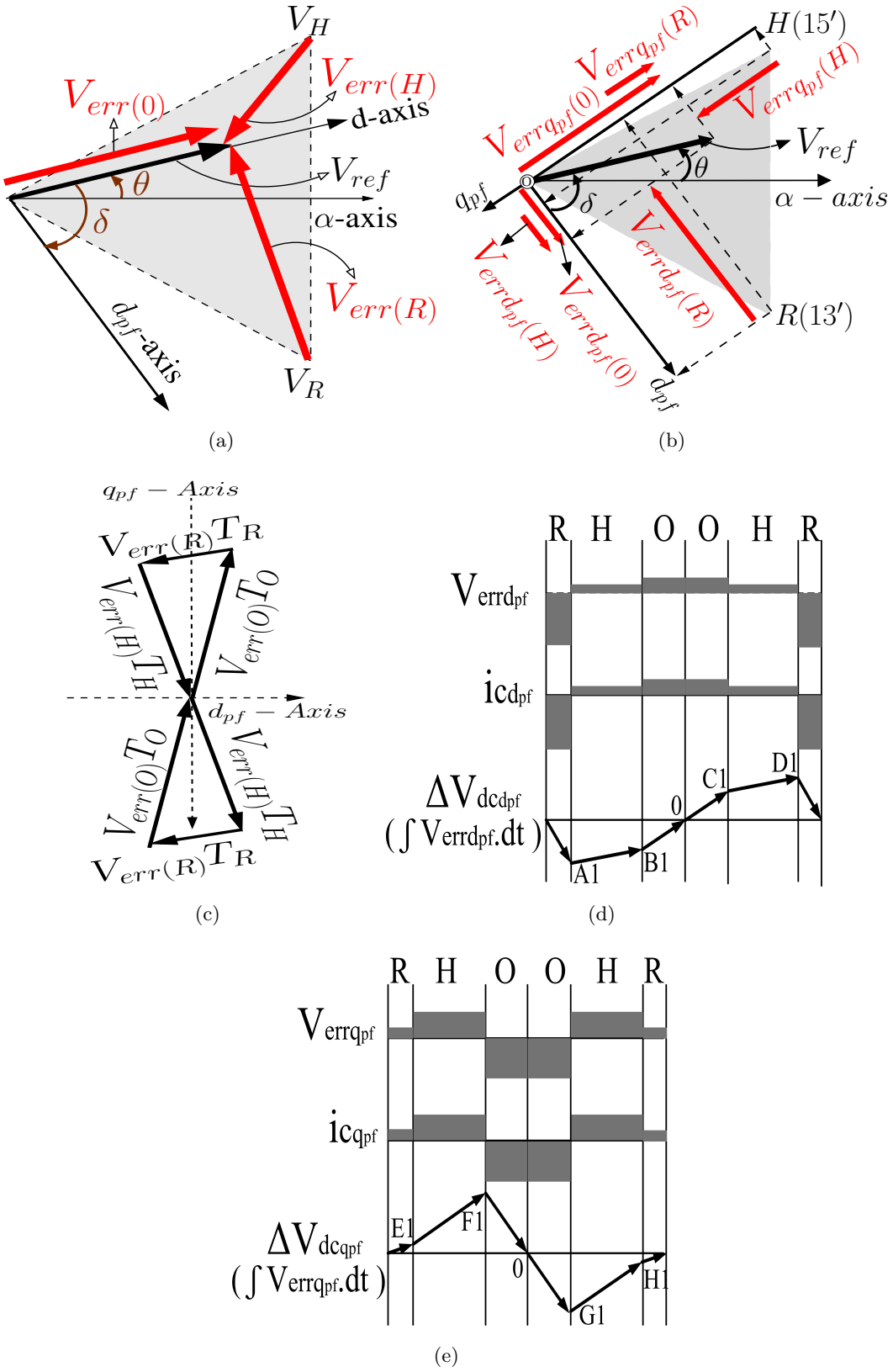


Figure 3.6: (a) Realisation of error vectors from switching locations (b) Error vectors projections on d_{pf} and q_{pf} axes (c) Error volt-sec space vector Trajectory (d) The error voltage magnitude, capacitor current and instantaneous error voltage integration on d_{pf}-axis ($\Delta V_{dc_{d_{pf}}}$) (e)The error voltage magnitude, capacitor current and corresponding instantaneous error voltage integration on q_{pf}-axis ($\Delta V_{dc_{q_{pf}}}$) while realizing the space vector in sector-1

locations R, H and O. The instantaneous switching vectors exert the instantaneous error vector as depicted in Fig. 3.6(a) can be derived as:

$$\overrightarrow{V_{err(H)}} = \overrightarrow{V_{ref}} - \overrightarrow{V_H}; \overrightarrow{V_{err(R)}} = \overrightarrow{V_{ref}} - \overrightarrow{V_R}; \overrightarrow{V_{err(O)}} = \overrightarrow{V_{ref}} \tag{3.24}$$

The ascertained error vectors corresponds to the switching states of the dual inverter is translated to the synchronous power factor coordinates (d_{pf} and q_{pf}-axes) using (3.18) & (3.19). The corresponding computed error voltage segments are shown in Fig. 3.6(b). The corresponding error voltage vector trajectory in synchronous power factor reference frame for the complete load space vector realization in a sampling time interval is shown in Fig. 3.6(c). From (3.18) and (3.19) it is evident that the error voltage space trajectory is in resemblance with the capacitor current space trajectory but with the magnitude difference of ($\frac{m_a}{\sqrt{r^2+x_l^2}}$) as depicted in (4.27). The error voltage and and error volt-sec projections on the d_{pf} and q_{pf} are shown in top and bottom traces of Fig. 3.6(d) and Fig. 3.6(e) respectively. In both the cases (shown in Fig. 3.6(d) and Fig. 3.6(e)), from top and middle traces it is clearly visible that, the error voltages on the d_{pf} and q_{pf} axes have a clear resemblance with the DC capacitor currents on d_{pf} and q_{pf} axes respectively, however, the DC capacitor current matches with the real axis (d_{pf}-axis) component. Further, the error volt-sec trajectory on d_{pf} and q_{pf} axes shown in bottom traces of Fig. 3.6(d) and Fig. 3.6(e) presents the DC bus voltage ripple in d_{pf} and q_{pf} respectively. However, the instantaneous error volt sec component on real-axis (d_{pf}-axis) (shown in bottom trace of Fig. 3.6(d)) mimics the DC voltage ripple derived from the DC capacitor bank.

From the erstwhile discussion, it is clear that the instantaneous error voltage derived in the synchronous power factor reference frame characterizes the DC bus voltage ripple. From Fig. 3.6(d) and Fig. 3.6(e), it is clear that the instantaneous error voltage magnitudes define the DC bus voltage ripple slope. However, as elaborated in the subsequent section, the peak ripple voltage magnitudes can be altered with error volt polarity-based switching sequencing.

3.3 The error voltage polarity based Switching sequence for minimum DC voltage ripple

In the preceding section, the DC bus voltage ripple is derived by exploiting the load error voltage vector information. While deriving the load space vector with two active and null vectors in an average sense, the instantaneous error voltages translated to the DC side using the synchronous power factor reference frame depict the DC bus current profiles. Since the peak DC bus voltage ripple profile is dependent on error voltage, in this work, the error voltage polarity influence on the peak DC bus ripple is explained by considering

two load space vector positions at $\theta = 337.5^o$ and 345^o. In both sampling time intervals, the error voltage magnitudes on d_{pf}-axis are computed for individual switching locations R, H and O (referring to Fig. 3.4) using (3.18) by assuming m_a=0.6 and $\delta = 60^o$. As per

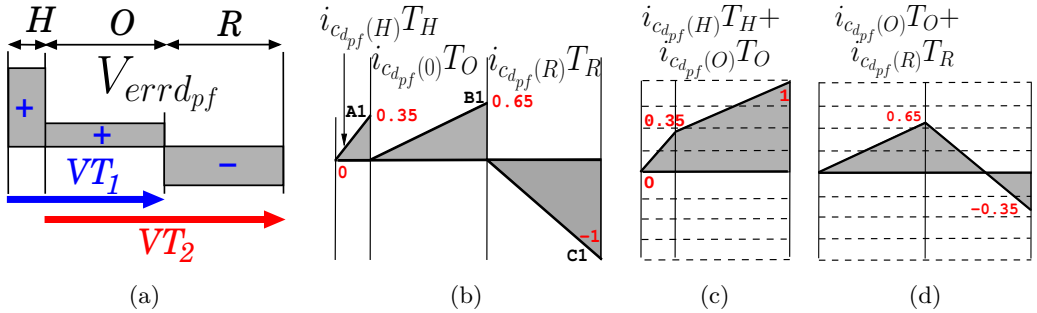


Figure 3.7: (a) The error voltage magnitude on d_{pf} -axis (b) The segment-wise error voltage integration profile on d_{pf} -axis. The error volt sec behavior with (c) identical polarity error voltage yield switching instants (d)opposite polarity yield error voltage switching placed together

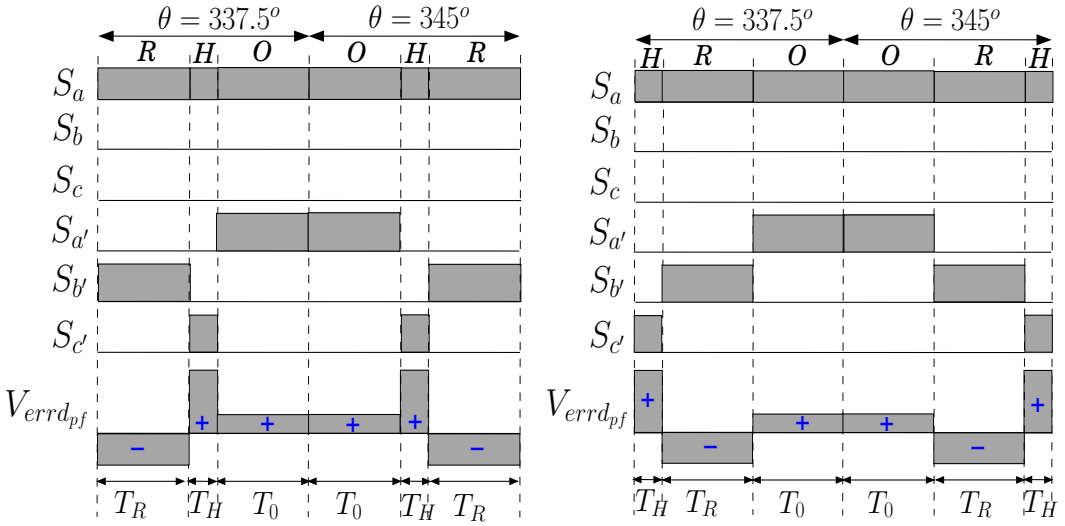
the computation, the switching locations 'H' and 'O' exhibits the positive error voltage magnitude, whereas R exhibits the error voltage with negative polarity, as shown in Fig. 3.7(a). Corresponding to the error voltage magnitudes, the DC bus voltage ripple variation for each switching states computed using (3.22) is depicted in Fig. 3.7(b). Nevertheless, in a sampling time interval, in consecutive switching instances, the error volt-sec segments are additive progressively, as shown in Fig. 3.7(c) and Fig. 3.7(d). It means the second switching instant error volt-sec segment start from the tail point of the first error volt-sec segment. Thus, the placement of the same polarity error voltage yield switching instants together results in the same direction ripple addition as shown in Fig. 3.7(c). Whereas with alternative polarity error voltage switching instances results in the ripple variation in an alternative direction as shown in Fig. 3.7(d). The derived inference of volt-sec (DC voltage ripple) variation with successive error voltage polarity switching instants is used to derive the two switching sequencing techniques named:

1. Consecutive Error Voltage Sign Sequencing (CEVSS)
2. Alternative Error Voltage Sign Sequencing (AEVSS)

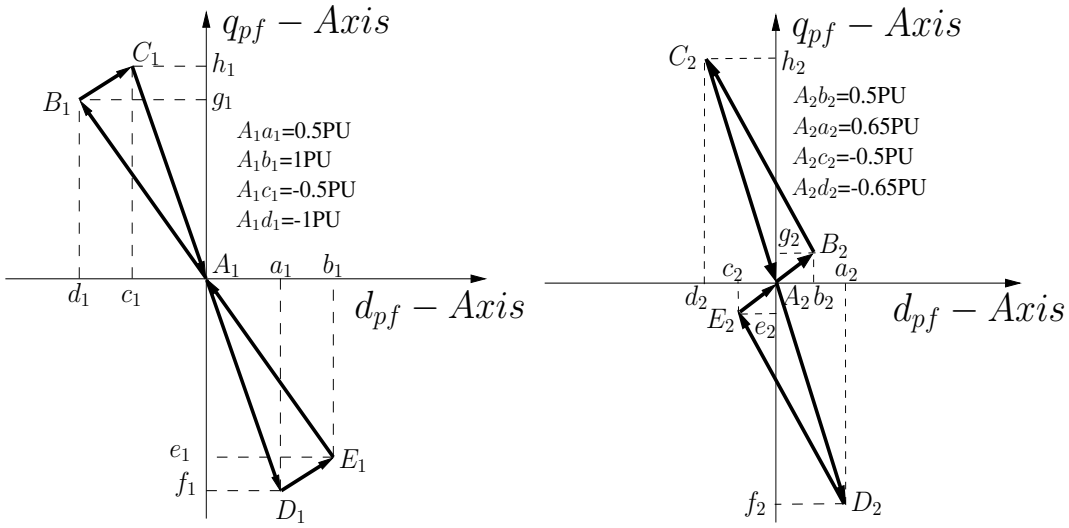
3.3.1 Consecutive Error Voltage Sign Sequencing (CEVSS)

In CEVSS, the load space vector is realized in a sampling time interval with the consecutive use of switching states with the same error voltage polarity on d_{pf} axis. For ease in explanation of CEVSS, the former load space vector instances at $\theta = 337.5^o$ and 345^o in a sector-1 are considered. In a sampling time interval corresponds to each space vector position, the CEVSS employs the switching locations with the same error voltage polarity on d_{pf} axis, i.e., 'H' and 'O', consecutively, as shown in the left trace of Fig. 3.8(a).

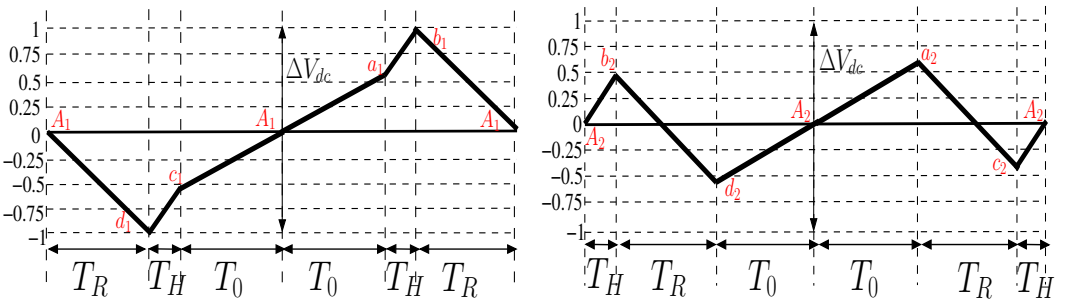
Based on the switching state selection, the error volt-sec (DC voltage ripple) space trajectory computed using (4.27) is shown in left trace of Fig. 3.8(b). As it can be



(a) The switching sequence of dual inverter to realize the V_{ref} and corresponding instantaneous error voltage computed using (3.18)



(b) The error volt-sec space vector trajectory on d_{pf}-q_{pf} axis



(c) The trajectory of error volt-sec vector projection on d_{pf}-axis ($\Delta V_{dc_{d_{pf}}}$ computed using (3.22)) equivalent to DC bus voltage ripple

Figure 3.8: The elicitation of DC bus voltage ripple at $\theta = 337.5^o$ and $\theta = 345^o$ with CEVSS (left traces) and AEVSS (right traces)

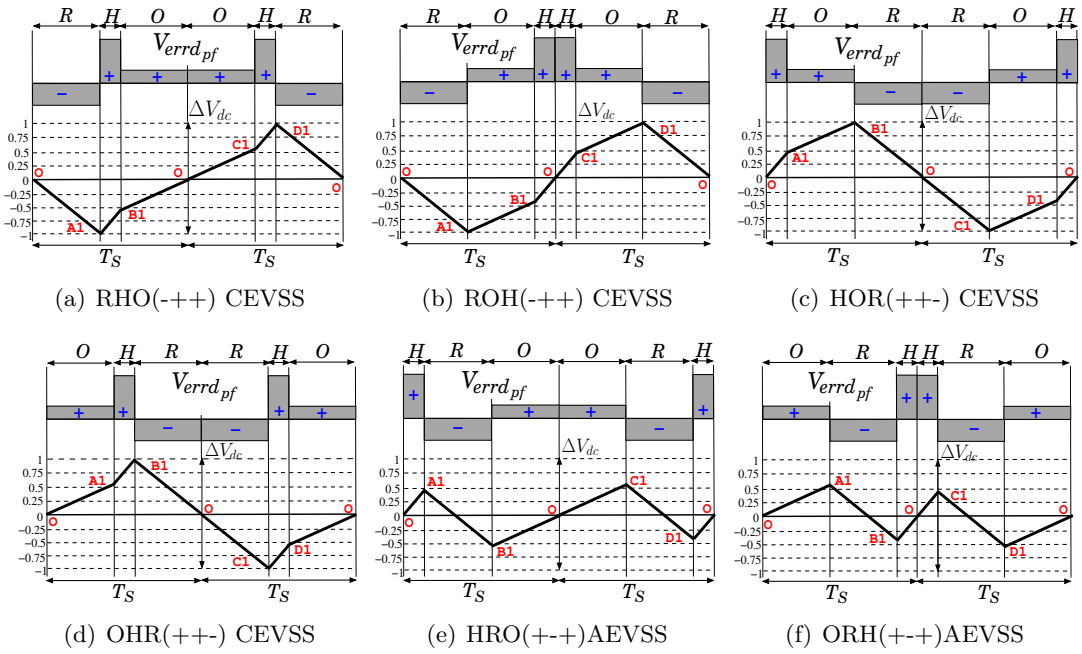
identified from Fig. 3.8(b), the error volt-sec vectors $\overrightarrow{A_1B_1}$ is realized with the switching state R, $\overrightarrow{B_1C_1}$ and $\overrightarrow{C_1A_1}$ are correspond to switching states 'H' and 'O' respectively in a first sampling time interval correspond to $\theta = 337.5^o$. Similarly, the trajectory $\overrightarrow{A_1D_1}$, $\overrightarrow{D_1E_1}$ and $\overrightarrow{E_1A_1}$ are realized error volt-sec vectors with switching states O, H and R respectively at $\theta = 345^o$. As discussed in the preceding section, error volt-sec vector projections on the d_{pf}-axis resemble the DC bus voltage ripple. The variation of the DC voltage ripple by projecting the error volt-sec space vector onto the d_{pf}-axis is shown in the left trace of Fig. 3.8(c). Here, to predict the peak DC voltage ripple in a sampling time interval, the magnitude transitions of each projected DC voltage ripple segment ($\Delta V_{dc_{d_{pf}}}$ computed using (3.22)) at every switching instance are tabulated in Table-3.4. From Table-3.4 it is evident that, in two sampling time intervals, the exhibited peak-peak voltage ripple is 2 p.u. (considering the peak error volt-sec with switching location R as base value). In CEVSS, although the switching sequence R H O (for $\theta = 337.5^o$) and O H R (for $\theta = 345^o$) considered alternatively as shown in left trace of Fig. 3.8(a), the total of six such sequencing can be realized as shown in Fig. 3.9. It can be identified from Fig. 3.9 that among six switching sequences, the four switching sequences are realized by placing the same error voltage polarity yield switching instances together and falls under the category of CEVSS, resulting in ripple voltages as shown in Fig. 3.9(a)-3.9(d). From Fig. 3.9(a)-3.9(d), it is evident that the peak-peak ripple magnitude is 2 p.u. confirming the uniformity in peak-peak ripple realization with CEVSS shown in the left trace of Fig. 3.8. The remaining two switching sequences are shown in Fig. 3.9(e) & Fig. 3.9(f) fall under category of Alternative Error Voltage Sign Sequencing (AEVSS). The voltage ripple realization with the AEVSS method is explained in the following sub-section.

Table 3.4: The elicitation of peak-peak DC bus voltage ripple ($\Delta V_{dc_{d_{pf}}}$) at $\theta = 337.5^o$ and 345^o with CEVSS

Sample No.	Switching location	ΔV_{dc} Segment		
		Slope from (Fig. 3.8(c))	Value	$\Delta V_{dc_{dpf}}$ (P-P)
$\theta = 337.5^o$	R	(-)A_1d_1	0 → (-1) p.u.	2 p.u.
	H	(+)d_1c_1	(-1)→(-0.65) p.u.	
	O	(+)c_1A_1	(-0.65)→(0) p.u.	
$\theta = 345^o$	O	(+)A_1a_1	(0)→(0.65) p.u.	
	H	(+)a_1b_1	(0.65)→(1) p.u.	
	R	(-)b_1A_1	(1)→(0) p.u.	

3.3.2 Alternative Error Voltage Sign Sequencing (AEVSS)

In AEVSS, unlike the CEVSS, the switching states in a sampling time interval are selected so that no subsequent switching state yields the same error voltage polarity. It means the switching location 'R' that yields the negative error voltage introduced between positive error voltage yielded switching locations 'H' and 'O' as shown in the right trace of Fig. 3.8(a). The same procedure is followed in two sampling time intervals to realize the space



(a) RHO(-++) CEVSS (b) ROH(-++) CEVSS (c) HOR(++-) CEVSS

(d) OHR(++-) CEVSS (e) HRO(+-+)AEVSS (f) ORH(+-+)AEVSS

Figure 3.9: The possible switching sequence configurations for achieving load space vector with common-mode voltage elimination within two sampling time intervals (T_s) correspond to $\theta = 337.5^o$ and 345^o

vector at $\theta = 337.5^o$ and 345^o. With the alternative error voltage switching, the error volt-sec (DC bus voltage ripple) space trajectory on synchronous power factor coordinates computed using (4.27) is shown in the right trace of Fig. 3.8(b). In voltage space trajectory, the vectors $\overrightarrow{A_2B_2}$, $\overrightarrow{B_2C_2}$ and $\overrightarrow{C_2A_2}$ are realized with the switching instances H R O respectively at $\theta = 337^o$. Similarly $\overrightarrow{A_2D_2}$, $\overrightarrow{D_2E_2}$ and $\overrightarrow{E_2A_2}$ are realized by placing switching states O R and H in sampling time interval to realize the load space vector at $\theta = 345^o$. Further, the error volt-sec space trajectory projected onto the d_{pf} axis realizes the DC bus voltage ripple pattern as shown in the right trace of Fig. 3.8(c). The corresponding projected segments magnitude variations on d_{pf} are tabulated in tabulated in Table-3.5. From Table-3.5 it is evident that with the AEVSS method, the peak to peak voltage ripple magnitude is 1.3 p.u.. Apart from the demonstrated switching sequence, the other AEVSS placement shown in Fig. 3.9(e) & Fig. 3.9(f) also yields the same 1.3 p.u. peak to peak voltage magnitude. With this discussion, it can be concluded that the switching sequence to realize the space vector in sampling time interval influences the peak-peak magnitude of DC bus voltage. Moreover, it is evident from the discussion that the DC bus voltage ripple is grossly dependent on the instantaneous space location used to realize the space vector but does not vary with the switching combination. For example, the switching location H can be realized with the dual inverter switching combination 15' or 24' (Fig. 3.4), but both switching combinations yield the same error voltage vector. Thus, broadly switching locations are considered to realize the DC bus voltage ripple in this work. Since the peak to peak DC voltage ripple magnitude is influenced by the switching sequence within the sampling time interval, all possible switching sequence realizations broadly fall

in either CEVSS or AEVSS. Further, it is demonstrated in this work the AEVSS method is superior compared to the CEVSS method in terms of accomplished reduced peak-peak voltage ripple. The superiority of AEVSS over CEVSS in terms of reduced voltage ripple and corresponding DC capacitor bank size reduction is demonstrated experimentally in subsequent sections.

Table 3.5: The elicitation of peak-peak DC bus voltage ripple ($\Delta V_{dc_{d_{pf}}}$) at $\theta = 337.5^o$ and 345^o with AEVSS

Sample No.	Switching location	ΔV_{dc} Segment		
		Slope from (Fig. 3.8(c))	Value	$\Delta V_{dc_{dpf}}$ (P-P)
$\theta = 337.5^o$	H	(+)A_2b_2	(0)→(0.35) p.u.	1.3 p.u.
	R	(-)b_2d_2	(0.35)→(-0.65) p.u.	
	O	(+)d_2A_2	(-0.65)→(0) p.u.	
$\theta = 345^o$	O	(+)A_2a_2	(0)→(0.65) p.u.	
	R	(-)a_2c_2	(0.65)→(-0.35) p.u.	
	H	(+)c_2A_2	(-0.35)→(0) p.u.	

3.4 DC bus RMS voltage computation

The DC bus peak to peak voltage ripple influences the DC voltage ripple RMS value. The DC bus voltage ripple RMS value in both CEVSS and AEVSS in a sampling time interval can be computed using

$$\Delta V_{dc_{RMS}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} (\Delta V_{dc})^2.dt} \tag{3.25}$$

In a former mentioned space vector position at $\theta = 337^o$, the switching states used R H O in sampling time interval. For the mentioned sequence, the total RMS DC voltage ripple can be derived from individual DC voltage ripple segments at each switching instance as :

$$\Delta V^2_{dc_{RMS}} = \Delta V^2_{dc_{RMS(R)}} + \Delta V^2_{dc_{RMS(H)}} + \Delta V^2_{dc_{RMS(0)}} \tag{3.26}$$

At each segment the RMS value can be computed for the segments presented in left trace of Fig. 3.8(c)

$$\Delta V^2_{dc_{RMS(T_R)}} = \frac{1}{T_s}\int_0^{T_R} (\frac{-d1}{T_R}t)^2.dt \tag{3.27}$$

$$\Delta V^2_{dc_{RMS(T_H)}} = \frac{1}{T_s}\int_0^{T_H} (\frac{(d1-c1)}{T_H}t - d1)^2.dt \tag{3.28}$$

$$\Delta V^2_{dc_{RMS(T_0)}} = \frac{1}{T_s}\int_0^{T_0} (c1(\frac{t}{T_0} - 1))^2.dt \tag{3.29}$$

3.5 Results & Discussion

The proposed DC bus voltage ripple computational model is verified on the dual inverter hardware prototype shown in Fig. 3.10. The operating parameters of the dual inverter with considered load composition to derive different load power factors are tabulated in Table.3.6.

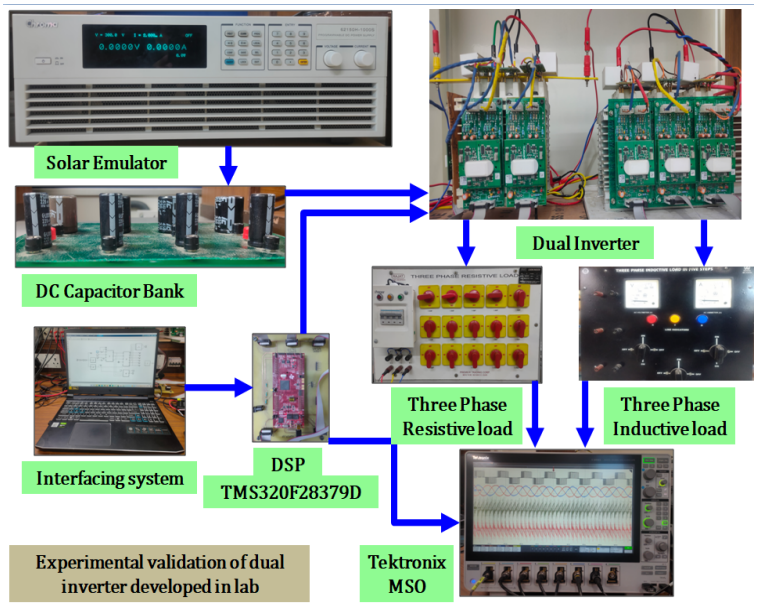


Figure 3.10: The dual inverter configuration lab experimental setup with a DSP control board, interfacing sensor, and measuring circuitry

Table 3.6: The experimental operating parameters of dual inverter

Parameters	Symbol	Values	Units
DC Bus Voltage	(V_{dc})	300	V
Fundamental Frequency	(ω_0)	104.67	Rad/sec
Switching Frequency	(ω_s)	5026.54	Rad/sec
DC Link Capacitor	(C_{dc})	100	uf
Load Resistance	r $(\delta = 60^o)$	133	Ω
Load Inductance	l $(\delta = 60^o)$	2.2	H
Load Resistance	r $(\delta = 40^o)$	203	Ω
Load Inductance	l $(\delta = 40^o)$	1.63	H

The demonstrated CEVSS and AEVSS PWMs implemented on the DSP board (TMS320F28379D) to switch the dual inverter for realizing the load space vector in average sense. While synthesizing the load space vector in average sense at m_a=0.6 and $\delta = 60^o$, the a-phase voltage and three-phase currents are shown in Fig. 3.11. The a-phase voltage depicted in Fig. 3.11 is the time average DC chopped voltage to mimic the AC voltage across the load with the magnitude variation between +300 V to -300 V. With the employed common DC bus for both the inverters, the sinusoidal three-phase currents are shown in the bottom trace of Fig. 3.11.

The common mode voltage of inverter-1, inverter-2 and dual inverter are shown in Fig.

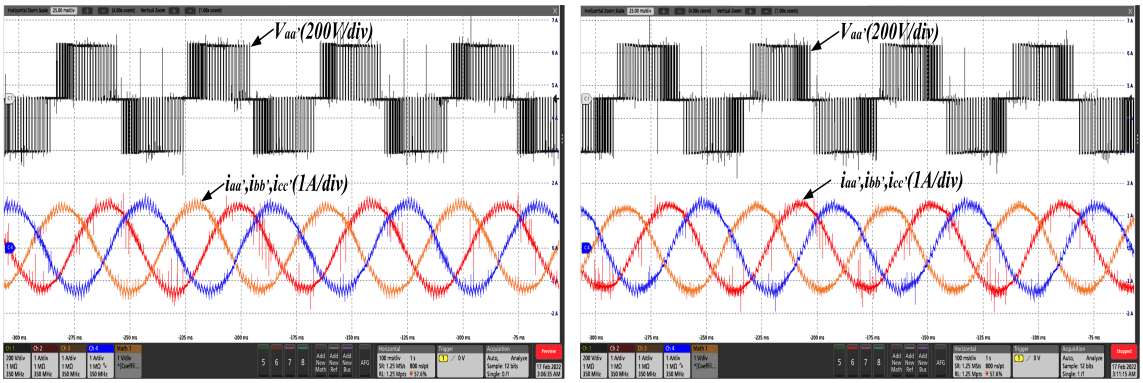
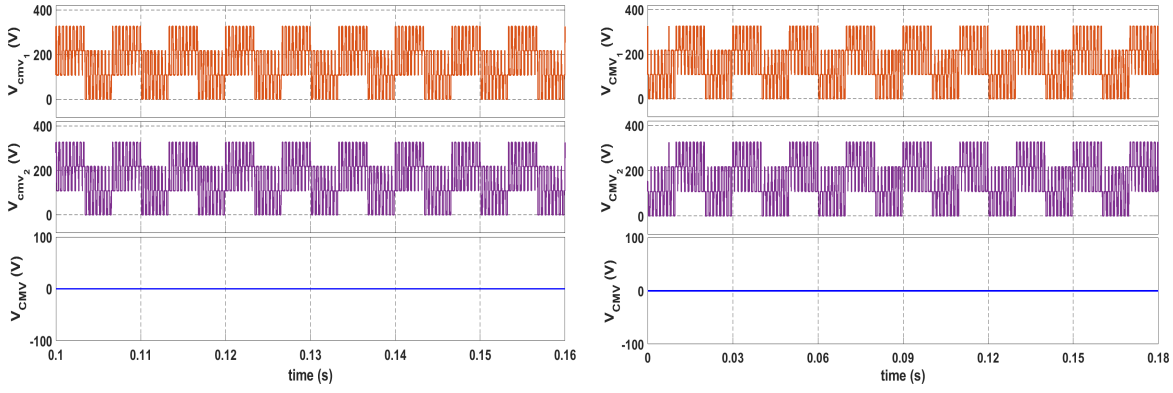


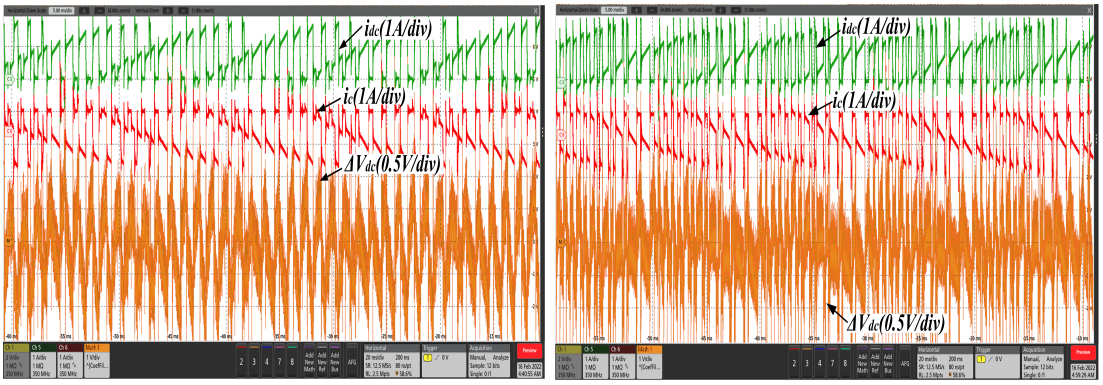
Figure 3.11: The load a-phase voltage derived using dual inverter configuration (top trace, X-axis:25 ms/div, Y-axis:200 V/div), and AC load three phase currents (bottom trace, X-axis:25 ms/div Y-axis:1 A/div) using CEVSS (left) and AEVSS (right)



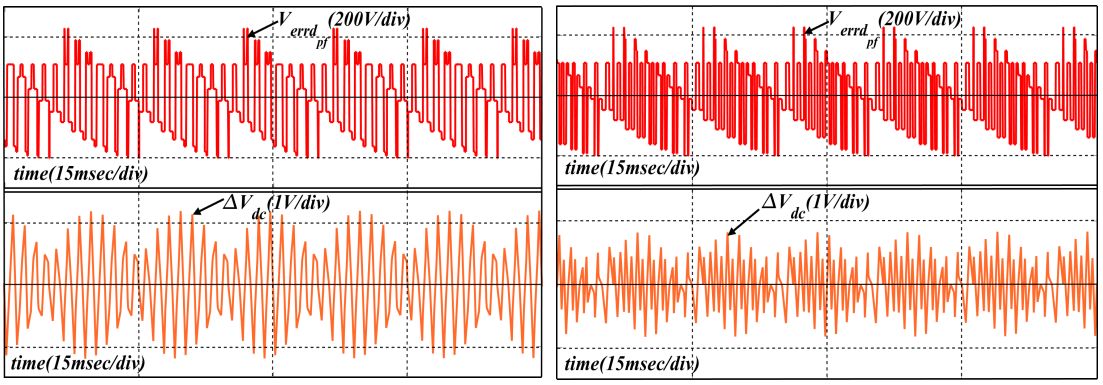
(a) CEVSS (b) AEVSS

Figure 3.12: The variation of common mode voltage of inverter-1 (V_{CMV_1}) (top trace), common mode voltage of inverter-2 (V_{CMV_2}) (middle trace) and common mode voltage of dual inverter (bottom trace) for CEVSS and AEVSS switching

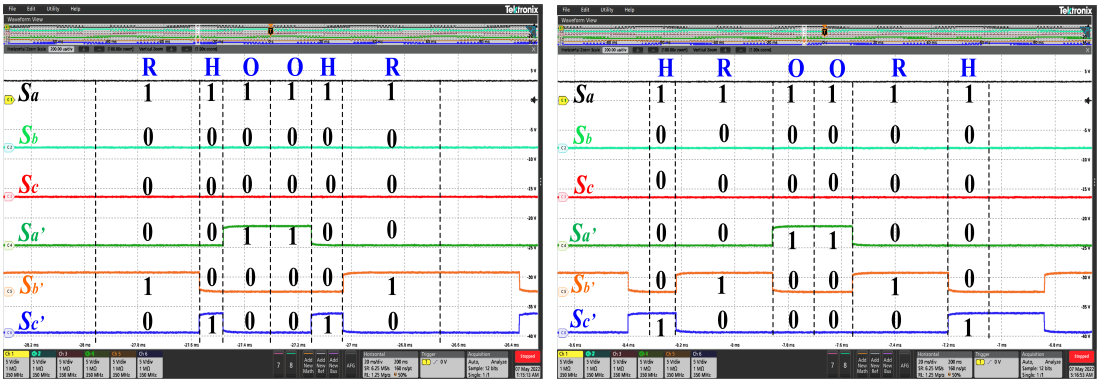
3.12 for CEVSS and AEVSS switching. From Fig. 3.12, although the inverter-1 and inverter-2 common mode voltages are present, the dual inverter common mode voltage is zero. From Fig. 3.12 it is also observed that both the switching schemes maintains the zero common mode voltage as claimed.



(a) Hardware results of DC link current (top trace, Y-axis:1 A/div), DC Capacitor current (middle trace, Y-axis:1 A/div) and DC voltage ripple (bottom trace, Y-axis:0.5 V/div) (X-axis:5 ms/div)

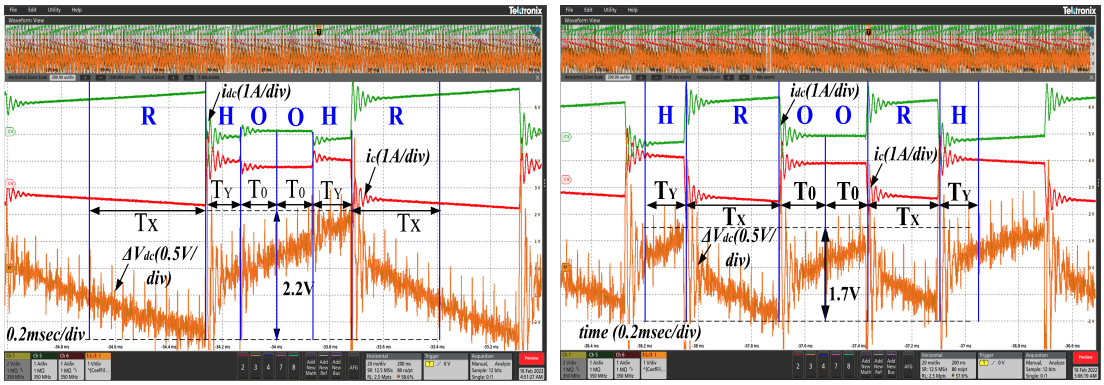


(b) Theoretically obtained error voltage projection on d_{pf}-axis computed using (3.18) (top trace,Y-axis:200 V/div) and error volt-sec on d_{pf}-axis computed using (3.22) (bottom trace,Y-Axis:1 V/div) over a fundamental cycle (X-axis:15 ms/div)

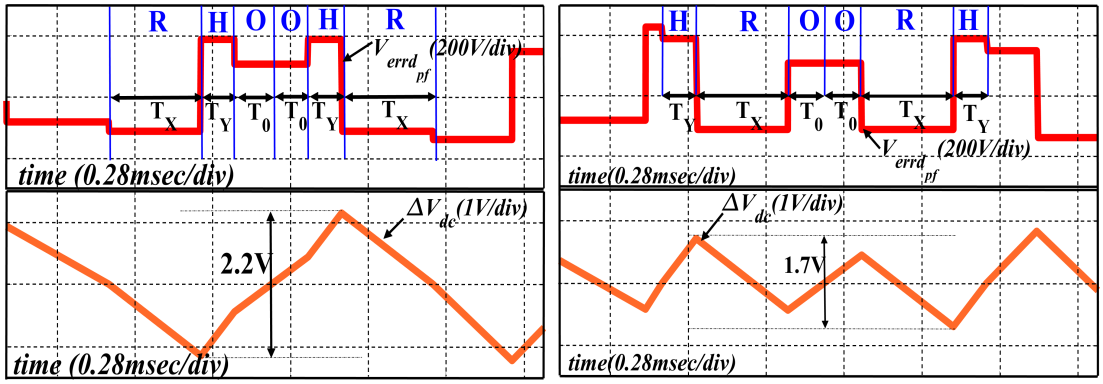


(c) The inverter-1 and inverter-2 pulse pattern to derive the space vector at $\theta = 337.5^o$ and $\theta = 345^o$(Y-axis:5 V/div),(X-axis:0.2 msec/div)

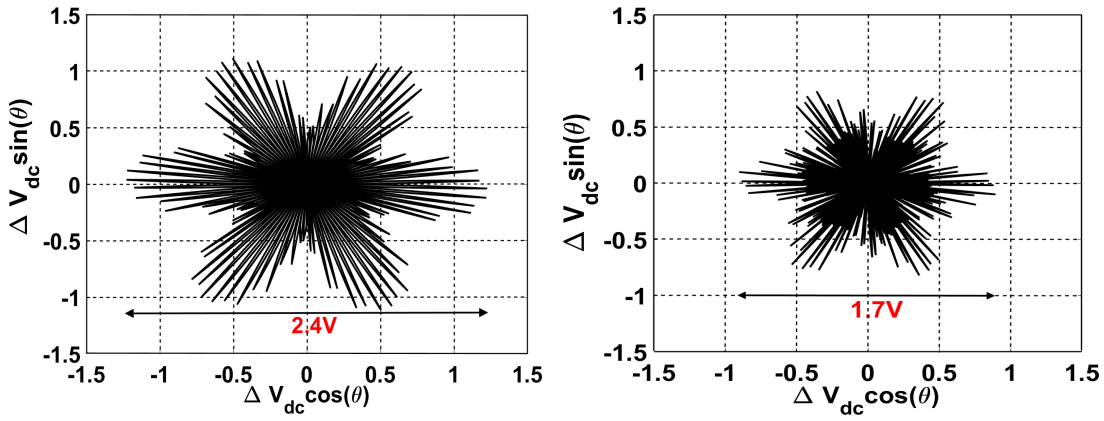
Further to demonstrate the computational DC bus voltage ripple model proposed in this work, the dual inverter DC side parameters such as DC link current, DC capacitor bank current, and the DC voltage ripple is taken for both CEVSS and AEVSS PWMs and shown respectively in the top, middle and bottom trace of Fig. 3.13(a). It is evident



(d) The zoomed portion of Fig. 3.13(a) at $\theta = 337.5^o$ and $\theta = 345^o$ representing experimentally obtained DC link current(top trace,Y-axis:1 A/div), DC Capacitor current (middle trace,Y-axis:1 A/div) and DC voltage ripple (bottom trace,Y-axis:0.5 V/div),(X-axis:0.2 ms/div)

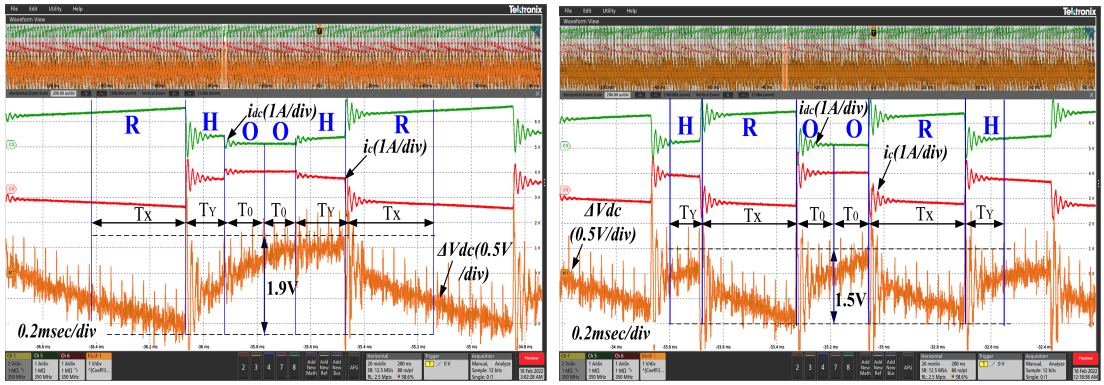


(e) The zoomed portion of Fig. 3.13(b) at $\theta = 337.5^o$ and $\theta = 345^o$ representing computational results of error voltage projection on d_{pf}-axis (top trace,Y-axis:200 V/div) and corresponding error volt-sec pattern on d_{pf}-axis (bottom trace,Y-axis:1 V/div),(X-axis:0.28 ms/div)

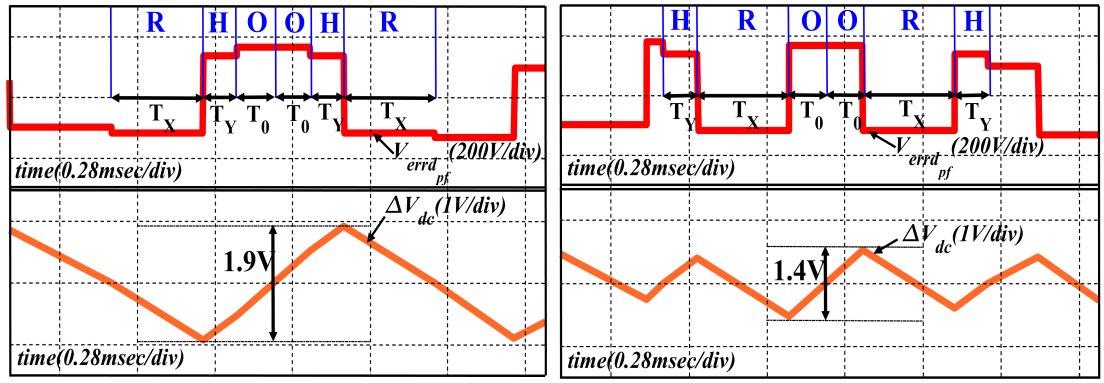


(f) The DC bus voltage ripple space plot ($\Delta V_{dc_{d_{pf}}} \cos(\theta) - \Delta V_{dc_{d_{pf}}} \sin(\theta)$) for fundamental cycle of V_{ref} (Y-axis:0.5 V/div),(X-axis:0.5 V/div)

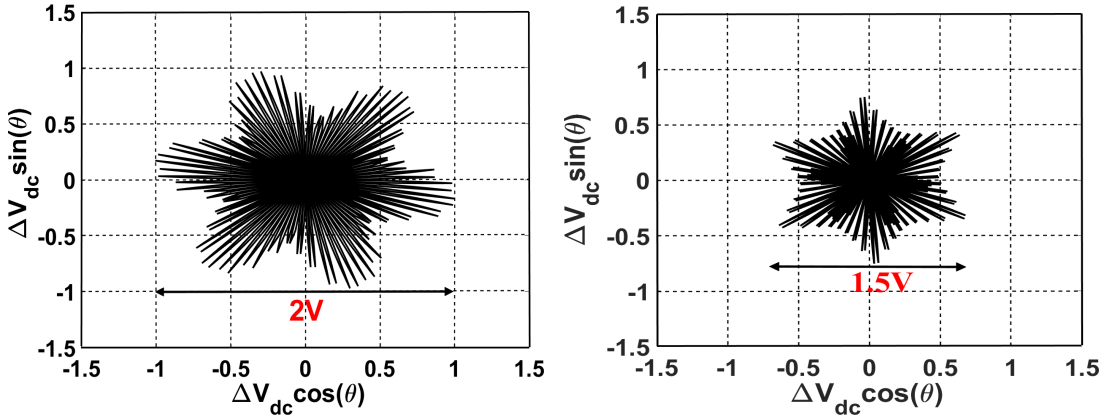
Figure 3.13: The AC and DC electrical parameter variation of the dual inverter while realizing load space vector at m_a= 0.6 and $\delta = 60^o$ using CEVSS (Left) and AEVSS (Right) PWMs



(a) The experimentally obtained DC link current(top trace,Y-axis:1A/div), DC Capacitor current (middle trace,Y-axis:1 A/div) and DC voltage ripple (bottom trace:0.5 V/div) at at $\theta = 337.5^o$ and $\theta = 345^o$ (X-axis:0.2 ms/div)



(b) The theoretically computed error voltage projection on d_{pf}-axis using (3.18) (top trace,Y-axis:200 V/div) and error volt-sec on d_{pf}-axis computed using (3.22) at $\theta = 337.5^o$ and $\theta = 345^o$ (bottom trace,Y-axis:1 V/div),(X-axis:0.28 ms/div)

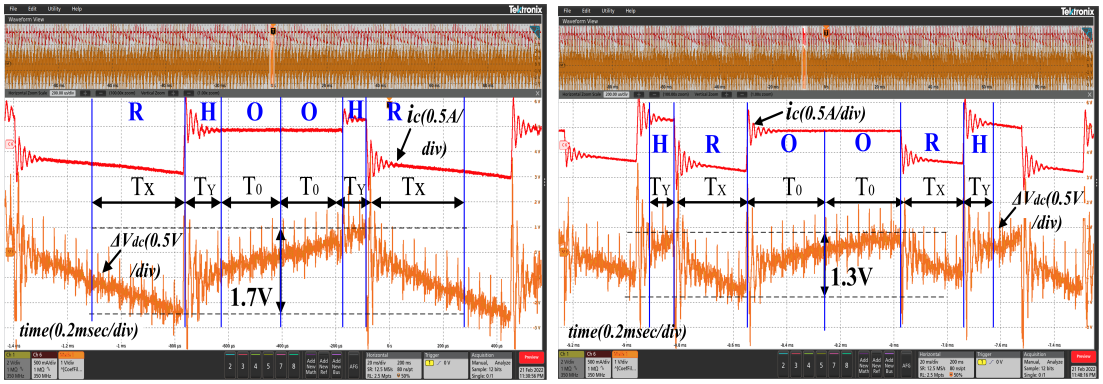


(c) The DC bus voltage ripple space plot ($\Delta V_{dc_{d_{pf}}} \cos(\theta) - \Delta V_{dc_{d_{pf}}} \sin(\theta)$) for fundamental cycle of V_{ref} (Y-axis:0.5 V/div),(X-axis:0.5 V/div)

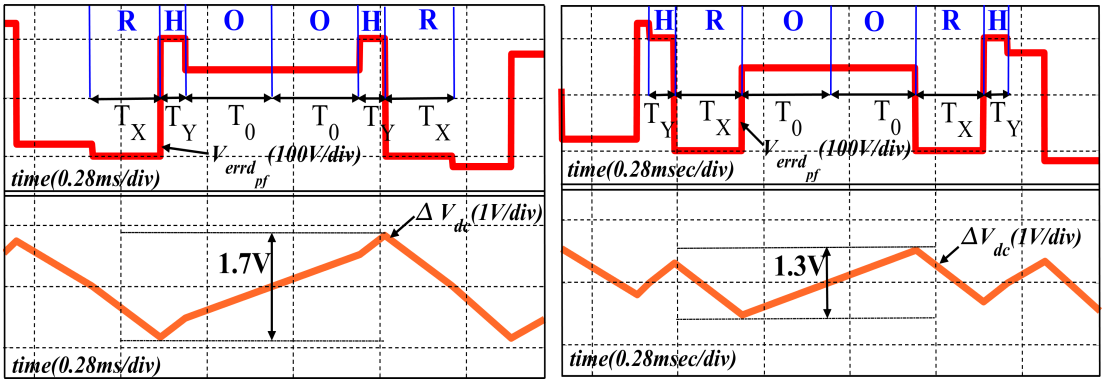
Figure 3.14: The DC voltage ripple realization at m_a=0.6 and $\delta = 40^o$ with CEVSS (Left) and AEVSS (Right)

from the DC bus current and DC capacitor current shown in top and middle trace of Fig. 3.13(a) that the capacitor supports the DC bus current ripple. The average current is drawn from the solar PV panel. As demonstrated in the preceding section, the computational error voltage and the error volt sec on d_{pf} axis shown in top and bottom traces of Fig. 3.13(b) is in resemblance with the DC capacitor current and DC bus voltage ripple respectively (shown in middle and bottom trace of Fig. 3.13(a)) for CEVSS and AEVSS. From Fig. 3.13(a) and Fig. 3.13(b), it is evident that the hardware results are in close correspondence with the theoretically computed results confirms the efficacy of the proposed DC voltage ripple mathematical model. Further to demonstrate the superiority of the AEVSS over the CEVSS in terms of reduced DC bus voltage ripple, the zoomed portion of the experimentally obtained DC link current, DC capacitor current and corresponding DC bus voltage ripple along with the inverter-1 and inverter-2 switching pattern at $\theta = 337.5^o$ and 345^o are shown in Fig. 3.13(c) & Fig. 3.13(d). Along with the experimental results, the zoomed portion of the computational error voltage and error volt-sec on d_{pf} axis at the same switching instants of $\theta = 337.5^o$ and 345^o are shown for CEVSS and AEVSS respectively in left and right traces of Fig. 3.13(e). From Fig. 3.13(d) and Fig. 3.13(e), it is visible that the derived computation model instantaneously maps the DC bus capacitor current and the DC bus voltage ripple at every instant. Moreover, it confirms that AEVSS PWM exhibits lesser peak-peak DC bus voltage ripple compared to CEVSS, as demonstrated in Section-3.3. Additionally to shown the DC bus voltage ripple reduction in a complete fundamental cycle with AEVSS compared to CEVSS, the voltage ripple space plot ($\Delta V_{dc}\cos(\theta) - \Delta V_{dc}\sin(\theta)$) shown in Fig. 3.13(f). From Fig. 3.13(f) it is observed that the AEVSS switching contributes to less DC voltage ripple compared to CEVSS.

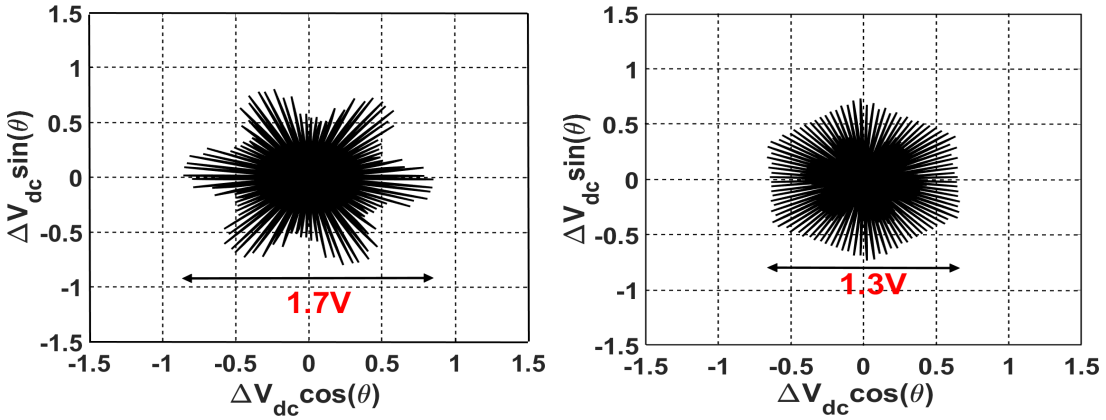
Further, the efficacy of the derived DC bus ripple voltage computational model and superiority of AEVSS over CEVSS in terms of reduced peak voltage ripple are demonstrated by considering the two additional test cases at different space vector modulation index and power factor angles. The first test case derived by choosing m_a=0.6 and $\delta = 40^o$. Whereas in the second test case, the m_a=0.4 and $\delta = 60^o$ (case-2) are chosen to validate the capacitor current and the DC bus voltage ripple. The experimentally obtained DC link current (top), DC capacitor current (middle) and DC voltage ripple at $\theta = 337.5^o$ and 345^o are furnished in Fig. 3.14(a) for case-1 and Fig. 3.15(a) for case-2. To demonstrate the experimental DC capacitor current and DC voltage ripple accordance with the theoretically derived error voltage and error volt-sec on d_{pf} axis, the computed $V_{errd_{pf}}$ using (3.18) and $\Delta V_{dc_{d_{pf}}}$ using (3.22) at $\theta = 337.5^o$ and 345^o are shown in top and bottom trace of Fig. 3.14(b) for case-1 and Fig. 3.15(b) for case-2. The experimental and theoretical results depicted for both cases show that the derived computational model is effective in deriving the DC capacitor current and DC bus voltage ripple at different modulations and power factor angles. From the results furnished left side and right side of Fig. 3.13 to Fig. 3.15 correspond to CEVSS and AEVSS, it is visible that AEVSS exhibit the lesser peak-peak voltage ripple compared to CEVSS in all the case. The same has been



(a) The experimentally obtained DC capacitor current (top trace,Y-axis:0.5 A/div) and DC voltage ripple (bottom trace:0.5 V/div) at $\theta = 337.5^o$ and $\theta = 345^o$ (X-axis:0.2 ms/div)



(b) The theoretically computed error voltage projection on d_{pf}-axis using (3.18) (top trace,Y-axis:100 V/div) and error volt-sec on d_{pf}-axis computed using (3.22) at $\theta = 337.5^o$ and $\theta = 345^o$ (bottom trace,Y-axis:1 V/div),(X-axis:0.28 ms/div)



(c) The DC bus voltage ripple space plot ($\Delta V_{dc_{d_{pf}}} \cos(\theta) - \Delta V_{dc_{d_{pf}}} \sin(\theta)$) for fundamental cycle of V_{ref} (Y-axis:0.5 V/div),(X-axis:0.5 V/div)

Figure 3.15: The DC voltage ripple realization at m_a=0.4 and $\delta = 60^o$ with CEVSS (Left) and AEVSS (Right)

confirmed by plotting the DC bus voltage ripple in a space ($\Delta V_{dc}\cos(\theta) - \Delta V_{dc}\sin(\theta)$) over a cycle shown in Fig. 3.14(c) and Fig. 3.15(c) for case-1 and case-2 respectively.

Table 3.7: DC voltage ripple RMS value computed with CEVSS (cell top value) and AEVSS (cell bottom value) at different load angles (δ) and modulation indices (m_a)

δ \ m_a	**0.1**	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**	**1**
0^o	0.0811 0.0810	0.2900 0.2900	0.5754 0.5747	0.8863 0.8637	1.1694 1.1694	1.3827 1.3820	1.4684 1.4684	1.3920 1.3887	1.1129 1.1129	0.6897 0.6877
10^o	0.0802 0.0801	0.2881 0.2858	0.5747 0.5647	0.8903 0.8671	1.1867 1.1395	1.4149 1.3355	1.5285 1.4013	1.4820 1.3003	1.2392 1.0142	0.8073 0.6950
20^o	0.0768 0.0757	0.2768 0.2702	0.5548 0.5315	0.8637 0.8106	1.1594 1.0611	1.4019 1.2312	1.5395 1.2757	1.5348 1.1687	1.3538 0.9202	0.9867 0.8099
30^o	0.0713 0.0699	0.2584 0.2477	0.5182 0.4860	0.8172 0.7375	1.1063 0.9568	1.3521 1.1029	1.5166 1.1355	1.5591 1.0398	1.4524 0.8803	1.1890 0.9900
40^o	0.0634 0.0621	0.2318 0.2192	0.4704 0.4289	0.7451 0.6481	1.0225 0.8368	1.2697 0.9584	1.4548 0.9850	1.5481 0.9262	1.5282 0.8956	1.3870 1.1890
50^o	0.0531 0.0515	0.1959 0.1813	0.4016 0.3531	0.6451 0.5312	0.8996 0.6810	1.1415 0.7840	1.3455 0.8259	1.4943 0.8455	1.5674 0.9734	1.5591 1.3983
60^o	0.0424 0.0404	0.1579 0.1417	0.3288 0.2750	0.5378 0.4139	0.7681 0.5355	1.0000 0.6295	1.2269 0.7076	1.4252 0.8265	1.5877 1.0913	1.7053 1.5813
70^o	0.0299 0.0275	0.1147 0.0970	0.2458 0.1893	0.4182 0.2890	0.6172 0.3887	0.8411 0.4960	1.0797 0.6378	1.3289 0.8598	1.5714 1.2086	1.8106 1.7209
80^o	0.0166 0.0142	0.0687 0.0528	0.1594 0.1109	0.2890 0.1900	0.4598 0.2990	0.6677 0.4498	0.9179 0.6601	1.2019 0.9468	1.5182 1.3255	1.8641 1.8139
90^o	0.0059 0.0059	0.0358 0.0332	0.0930 0.0897	0.1893 0.1893	0.3322 0.3255	0.5242 0.5282	0.7697 0.7641	1.0730 1.0697	1.4385 1.4352	1.8727 1.8671

Further, to verify the superiority of the AEVSS compared to CEVSS in terms of less voltage ripple yielding, the DC bus voltage ripple RMS value for both the switching sequences is computed and furnished in Table-3.7. It is evident from Table-3.7 that the RMS value computed with CEVSS (cell top value) is greater than computed RMS values with AEVSS (cell bottom value) at all space vector modulations (0.1 to 1) and from the power factor angle greater than 0^o and less than 90^o. It demonstrates the efficacy of the AEVSS in accomplishing reduced DC bus voltage ripple at all space vector modulations and the load power factor angles. In Table-3.7, all RMS value are shown in per unit by normalizing with CEVSS's DC ripple RMS value at m_a=0.6 and $\delta = 60^o$ as this condition exhibits the maximum DC voltage ripple reduction with AEVSS compared to CEVSS.

Similarly, the peak to peak DC bus ripple variation comparison for both the switching sequences is presented in Fig. 3.16. As it is shown in Fig. 3.16, the AEVSS exhibit lesser DC bus voltage ripple at power factor angles $\delta = 40^o$, 60^o and 80^o. Nevertheless, the peak to peak voltage ripple reduction with the AEVSS is maximum at a higher modulation index in line with the DC ripple RMS value computations. It is due to minimum usage of the null switching state in a sampling time interval.

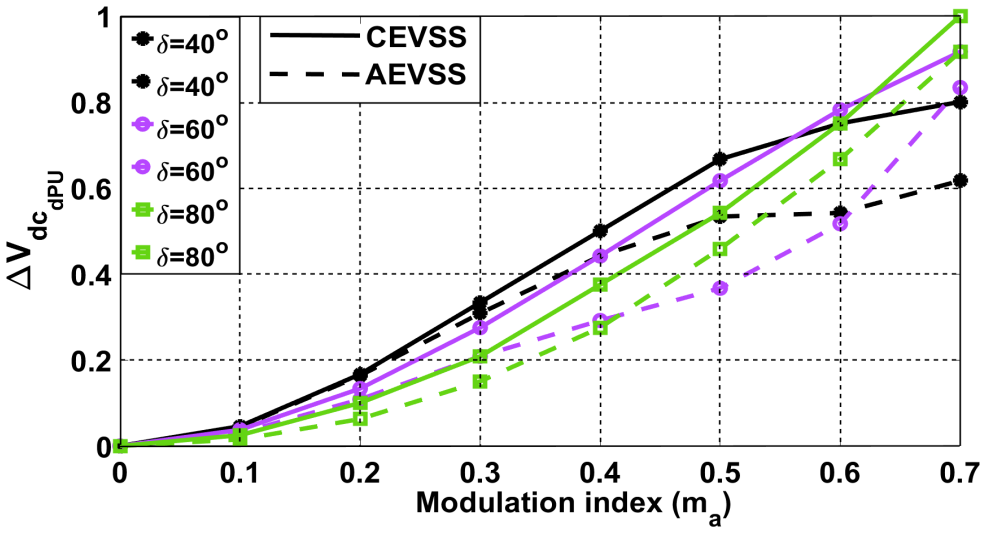


Figure 3.16: The variation DC bus voltage ripple peak - peak magnitude at different modulation indices (m_a) and load power factor angles (δ) with CEVSS and AEVSS PWMs

3.5.1 The dual inverter DC source voltage and current ripple characteristics

Since the inverter interfaced with the grid or dedicated loads operates in the closed-loop control to send the available active power into the grid, the converters' dynamic response depends on the system impedance components like DC capacitor bank and AC inductor and load resistance. Apart from the dynamic response, considering the reliability of the converter, the reduced DC capacitance without compromising the DC voltage ripple is highly desirable. This work demonstrates that the AEVSS yields a lesser DC voltage ripple than the CEVSS method with the given DC capacitance in a dual inverter with a common-mode voltage elimination configuration.

It has been demonstrated by connecting 100μ farad capacitor across the DC bus of the dual inverter, the DC source current, the capacitor current and the DC bus voltage ripple are shown in the top, middle, and bottom trace of Fig. 3.17 respectively for CEVSS (left) and AEVSS (right). From the zoomed portion of the DC source current shown in the top trace of Fig. 3.17, it is evident that the peak-peak current ripple is drawn from the DC source is 0.8A in the case of AEVSS and, on the other hand, with CEVSS, it is 1.5 A. It indicates that the current ripple experienced by the DC source is more in the case of CEVSS than AEVSS. Similarly, with CEVSS, the DC bus voltage ripple across the DC source is 6.4 Volts, but with AEVSS, it is only 4 V (peak to peak). Therefore, to accomplish the peak-peak voltage of 4 V with CEVSS, it must have a DC capacitance of 160 μfarad. From the DC source current ripple and voltage ripple comparison, it can be concluded that the AEVSS method demands a 35% lesser DC capacitance value compared to CEVSS to accomplish the designated voltage ripple.

The dynamic variation of three phase output current, DC source current and DC capacitor current is shown in Fig.3.18. From Fig.3.18 it is observed that the when the irradiance decreases the from 800 W/m^2 to 400 W/m^2, the three phase currents, DC source current

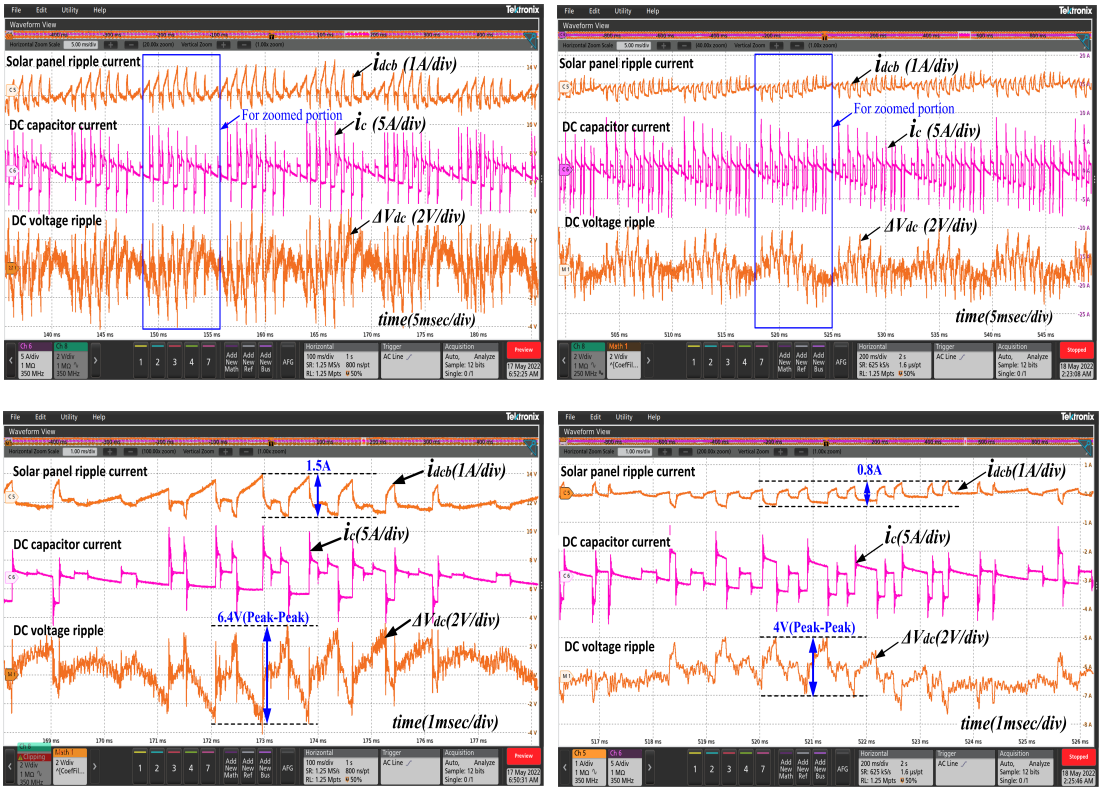


Figure 3.17: The experimentally obtained solar PV array current (top,Y-axis:1 A/div), the DC capacitor current (middle, Y-axis:5 A/div) and the DC bus voltage ripple (bottom trace,Y-axis:2 V/div) with CEVSS PWM (left) and AEVSS PWM (right) for one fundamental cycle (top scope,X-axis:5 ms/div) and zoomed in a sub-hexagonal sector cycle (bottom X-axis:1 ms/div)

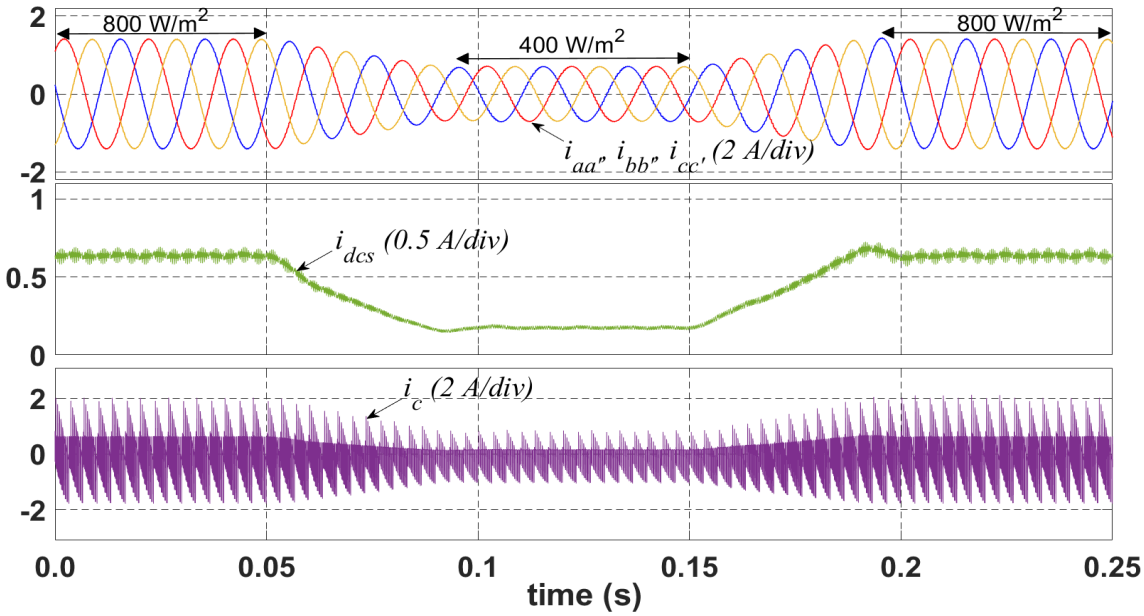


Figure 3.18: Variation of three phase current (top trace), DC source current (middle trace) and DC capacitor current (bottom trace) for the dynamic change of irradiance at C_{dc}= 1200 uf

and DC capacitor current decreases. Similarly, when the irradiance increases the from 400 W/m^2 to 800 W/m^2, the three phase currents, DC source current and DC capacitor current will also get increases. It indicates the direct proportionality of power with the three phase currents. DC source currents and DC capacitor currents.

3.6 Conclusion

The presented work in this chapter demonstrated the DC bus voltage ripple computational method by exploiting the AC error voltage vector information. The proposed model is independent of instantaneous current information, making the derived model an offline model. Thus it supports assessing the PWM techniques for minimum voltage ripple. The derived computational method in this work demonstrates the dual inverter switching sequence influence on the DC bus voltage ripple by selecting the switching instants with the same error voltage polarity consecutively and alternatively named CEVSS and AEVSS, respectively. Further, it has been identified that, between the derived switching sequences, the AEVSS yields minimum voltage ripple compared to CEVSS. The exhibited minimum DC voltage ripple with AEVSS has been further confirmed by computing the voltage ripple RMS value at different modulations and loading conditions. Finally, from derived switching sequencing through proposed DC voltage ripple computational model in this work, it is observed that the DC capacitor size with the AEVSS method is 35% lesser than the CEVSS method to accomplish the designated DC percentage voltage ripple at m_a=0.6 and $\delta = 60^o$.

In practical scenario, in PV grid-connected inverter operations, δ typically ranges from 5^o to 10^o. When designing for AEVSS switching, the DC capacitor sizing should be based on the worst-case conditions as outlined in Table-3.7 at $\delta = 10^o$. Here, the highest DC bus voltage ripple is observed at $m_a = 0.7$ for AEVSS, resulting in 1.4013 PU. Engineers must design the DC capacitor to accommodate this voltage ripple as the system exclusively operates with AEVSS. Comparatively, CEVSS generates a higher DC voltage ripple of 1.5285 PU. Consequently, there is an 8.32% reduction in DC capacitance requirement with AEVSS compared to CEVSS in PV grid-connected inverters. In motor drive applications, during full load conditions, the motor drive operates with δ ranging from 30^o to 40^o. When considering the worst-case scenario and designing with AEVSS switching, the highest DC bus voltage ripple is 1.1355 PU at $m_a = 0.7$ and $\delta = 30^o$. In contrast, CEVSS generates a higher DC voltage ripple of 1.5591 PU. This results in a substantial 27.16% reduction in DC capacitance requirement with AEVSS compared to CEVSS in motor drive application. Therefore, even under worst-case conditions, AEVSS switching consistently requires less DC link capacitance.

Chapter 4

A Novel Switching Vector Sequencing Method to Minimize DC Voltage Ripple

Nowadays, dual inverters with separate DC links are gaining popularity in motor drive applications due to their enhanced scalability and control flexibility compared to dual inverters with a common DC link. A significant advantage of using a dual inverter with a separate DC link is its ability to offer higher switching redundancies across the load. In dual inverters with a common DC link, each inverter operates at a switching frequency, and consequently, the load current also experiences the harmonics at switching frequency. This switching pattern can lead to higher total harmonic distortion (THD) in the load current. In contrast, in a dual inverter with separate DC links, although each inverter operates at switching frequency, the load experiences a higher effective switching frequency. This higher effective frequency results in lower THD in the load current compared to a dual inverter with a common DC link. Currently, there is a research gap in the analysis of DC voltage ripple and DC source current ripple in the literature for dual inverter with separate DC link. Addressing this gap and aiming to reduce load current THD, this chapter focuses on analyzing and minimizing DC link ripple using a dual inverter with a separate DC link.

4.1 Dual inverter configuration with separate DC source

The dual two-level inverter-fed open-end winded induction motor operated with a separate DC source is shown in Fig. 4.1. Here, S_a, S_b, and S_c are the top switch switching functions of inverter-1 corresponding to poles a, b, and c. Similarly, $S_{a'}$, $S_{b'}$ and $S_{c'}$ are the top switch switching function of inverter-2 corresponding to pole a', b' and c'. $i_{aa'}$, $i_{bb'}$ and $i_{cc'}$ are the three-phase load current of dual inverter. i_{dc_1}, i_{dc_2}, i_{c_1}, i_{c_2}, i_{dcs_1} and i_{dcs_2} are the DC link current, DC capacitor current and DC source current of inverter-1 and inverter-2 respectively. R_s denotes the series resistance. The two inverters are connected back to back as shown in Fig. 4.1 to synthesize the average voltage across the induction motor. The average voltage synthesized across the motor with the two inverters can be defined as:

$$V_{ref}\angle\theta = \underbrace{\frac{V_{ref}}{2}\angle\theta}_{V_{ref_1}} - \underbrace{\frac{V_{ref}}{2}\angle(\theta+\pi)}_{V_{ref_2}} \tag{4.1}$$

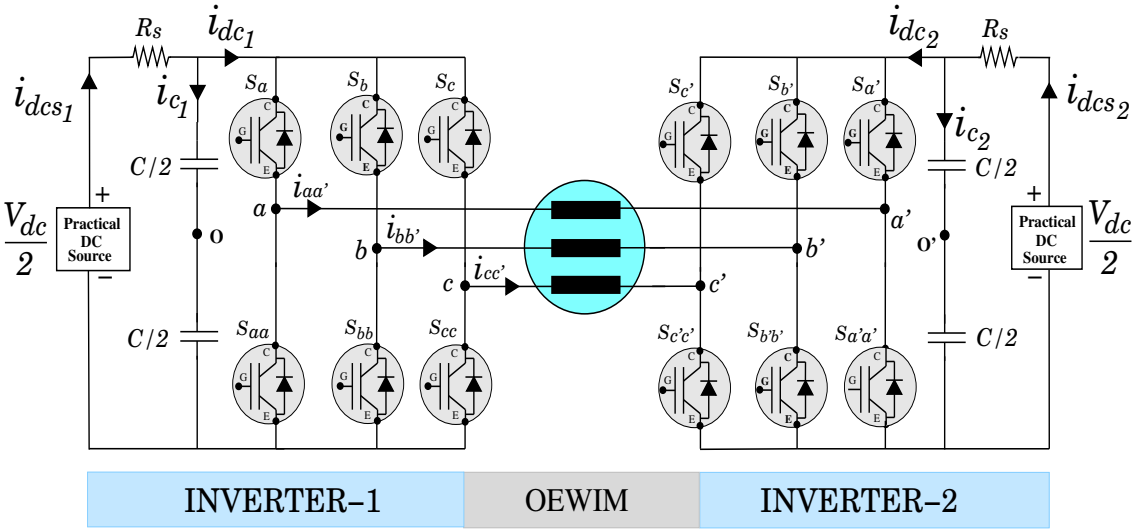


Figure 4.1: The open-end winding induction motor (OEWIM) powered by a dual inverter with isolated DC sources.

Where V_{ref} is the reference voltage space vector generated across the load. V_{ref_1} and V_{ref_2} are the individual inverter reference voltage space vector. θ represents dual inverter space vector angle. The 180^o phase shifted operation by inverter-1 and inverter-2 as per (4.1), derives the maximum voltage across the induction motor drive. The realization of the average load space vector with inverter-1 and inverter-2 using volt-sec balance is shown in Fig. 4.2 can be mathematically written as:

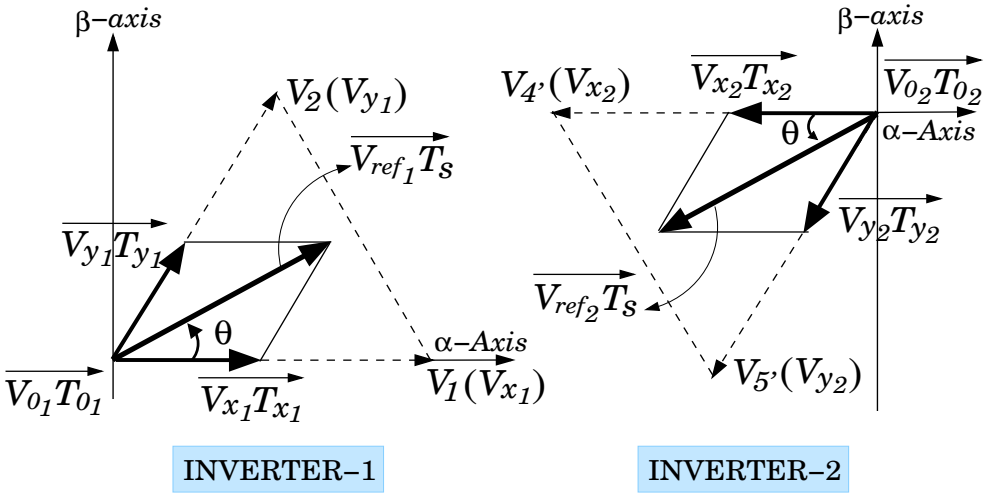
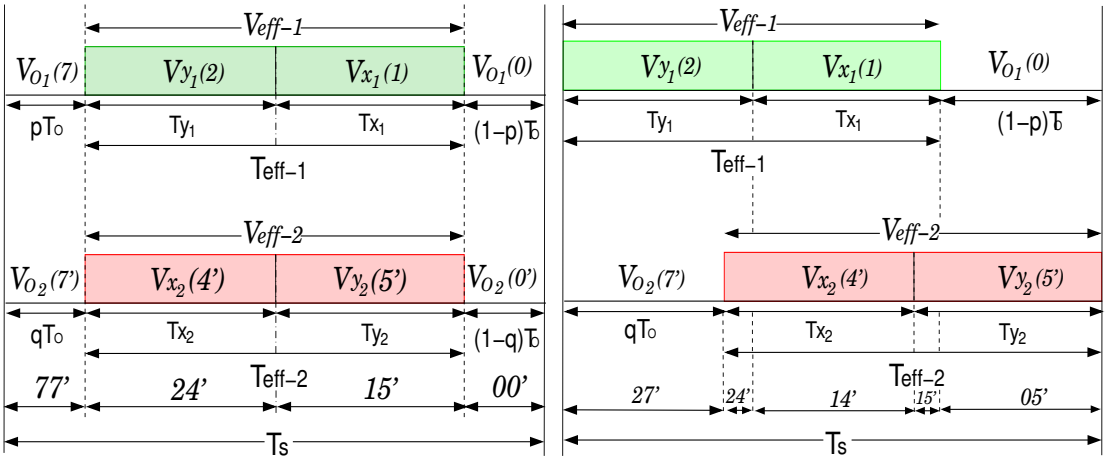


Figure 4.2: The OEWIM reference vector realization with inverter-1 and inverter-2 using volt-sec balance

$$\overrightarrow{V_{ref_1}T_s} = \overrightarrow{(p)V_{0_1}T_{0_1}} + \underbrace{\overrightarrow{V_{x_1}T_{x_1}} + \overrightarrow{V_{y_1}T_{y_1}}}_{\overrightarrow{V_{eff-1}T_{eff-1}}} + \overrightarrow{(1-p)V_{0_1}T_{0_1}} \tag{4.2}$$

$$\overrightarrow{V_{ref_2}T_s} = \overrightarrow{(q)V_{0_2}T_{0_2}} + \underbrace{\overrightarrow{V_{x_2}T_{x_2}} + \overrightarrow{V_{y_2}T_{y_2}}}_{\overrightarrow{V_{eff-1}T_{eff-1}}} + \overrightarrow{(1-q)V_{0_2}T_{0_2}} \tag{4.3}$$

Where T_s is the sampling time interval. As mentioned in (4.2) and (4.3), the two inverters synthesize the reference vector (V_{ref_1} and V_{ref_2}) in the average sense using the nearest active and null vectors. Thus the sampling time interval (T_s) is composed of null and active voltage vectors with the designated dwell times derived instantaneously based on the magnitude and position of the reference vector. In this work, the space vector is assumed to be rotating in an anti-clockwise direction and covers the six sectors of a hexagon in one cycle. For presenting the generalized volt-sec balance equation as mentioned in (4.2) and (4.3), the switching vector and corresponding dwell time behind the space vector (V_1 in Fig. 4.2) is mentioned as V_{x_1}, and T_{x_1}, similarly, the active switching vector ahead of the space vector (V_2 in Fig. 4.2) represented with V_{y_1} and T_{y_1} for inverter-1. The null vector along with its time is represented for inverter-1 as V_{0_1} and T_{0_1}. Similarly for inverter-2, the active and null vectors can be represented as V_{x_2}, V_{y_2} and V_{0_2} while timings can be represented as T_{x_2}, T_{y_2} and T_{0_2}. $T_{eff_1}(T_{x_1} + T_{y_1})$ and $T_{eff_2}(T_{x_2} + T_{y_2})$ are the effective times of inverter-1 and inverter-2.



(a) Continuous PWM (SVPWM) (b) Discontinuous PWM

Figure 4.3: The placement of active and null vectors in a sampling time interval to derive the continuous and discontinuous PWMs

In (4.2) and (4.3), the p and q represent the null volt-sec segregation indexes that vary from 0 to 1. The null time segregation in a sampling time interval by simply varying the p (inverter-1) and q (inverter-2), as shown in Fig. 4.3 to realize the continuous and discontinuous PWMs. The placement of the active and null vectors in a sampling time interval defines the load current and DC voltage ripple signatures. In line with the current ripple signatures, the switching vector influence on the DC bus voltage ripple and DC source current ripple is modeled in the following section.

4.2 Mathematical modeling of instantaneous DC voltage ripple variation with instantaneous inverter switching

The fundamental average voltage synthesized by the dual inverter in d-q reference frame can be computed using (3.10) and (3.11). Where v_d and v_q are the direct and quadrature

axis components of the reference voltage space vector. Since the dual inverter synthesized instantaneous voltages in an average sense with isolated DC sources, the individual inverters influence the respective DC link currents and, thereby the DC link voltage ripple. Therefore, this work analyzes the individual inverter switching and DC link voltage ripple. For an individual inverter, the instantaneous switching voltage in a synchronous reference frame using (3.12) and (3.13) for dual inverter with seperate DC link can be represented as:

$$v_{d_{swr}} = \frac{2}{3}\frac{V_{dc}}{2}(S_{a_r}\cos(\theta-\psi) + S_{b_r}\cos(\theta-2\pi/3-\psi) + S_{c_r}\cos(\theta+2\pi/3-\psi)) \quad (4.4)$$

$$v_{q_{swr}} = \frac{2}{3}\frac{V_{dc}}{2}(S_{a_r}\sin(\theta-\psi) + S_{b_r}\sin(\theta-2\pi/3-\psi) + S_{c_r}\sin(\theta+2\pi/3-\psi)) \quad (4.5)$$

Where $(S_{a_r}, S_{b_r}\&S_{c_r})$ are the instantaneous switching states of the inverter to realize the V_{ref} in an average sense. $v_{d_{swr}}$ and $v_{q_{swr}}$ are direct and quadrature axis components of instantaneous switching voltage. ψ denotes the fundamental phase shift between the inverter-1 and inverter-2. Here for inverter-1 r=1 and $\psi = 0$, similarly for inverter-2 r=2 and $\psi = \pi$. In motor drives, although the reference vector (V_{ref}) synthesizes in the average sense, the current vector (i) is displaced from the V_{ref} by the power factor angle (δ) as shown in Fig. 4.4 can be expressed as

$$i\angle -\delta = \frac{v_d}{Z\angle\delta} \implies \frac{v_d}{r+jx_l} \quad (4.6)$$

As depicted in (4.6), the load impedance and the reference voltage define the load current.

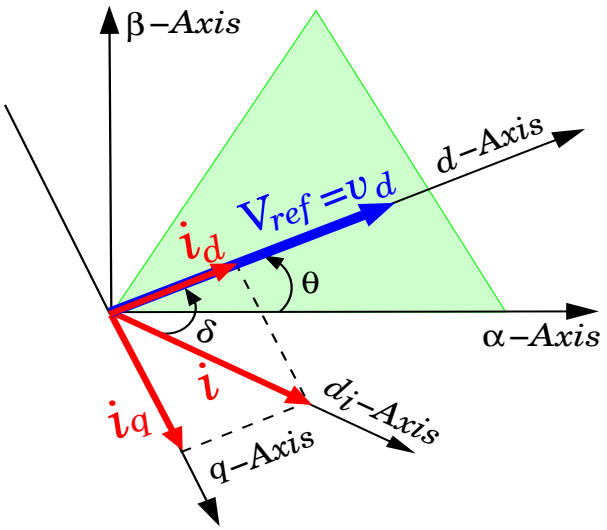


Figure 4.4: The current vector coordinate realization with consideration of power factor angle δ

The load current is decomposed into real (i_d) and reactive (i_q) components respectively aligned with the reference voltage vector (V_{ref}) and quadrature axis (q-axis) as shown in Fig. 4.4. With the defined real and reactive components of the current, the instantaneous

load impedance (Z) of the motor can be mathematically represented as:

$$Z = r + jx_l = \frac{v_d}{i_d + ji_q} \tag{4.7}$$

Rationalizing the (4.7) to separate the real and imaginary part as:

$$Z = r + jx_l = \frac{v_d}{i_d + ji_q} * \left(\frac{i_d - ji_q}{i_d - ji_q}\right) \tag{4.8}$$

Separating the real and imaginary part, the (4.8) can be simplified as

$$Z = r + jx_l = \left(\frac{v_d i_d}{i_d^2 + i_q^2}\right) + j\left(\frac{-v_d i_q}{i_d^2 + i_q^2}\right) \tag{4.9}$$

Where r and x_L are the per-phase equivalent AC resistance and reactance of the load. Upon the computation of AC side impedance, the equivalent DC impedance can be derived as a function of inverter modulation (m_a) as:

$$Z_{dc} = R_{dc} + jX_{Ldc} = (R/m_a) + j(X_L/m_a) \tag{4.10}$$

The influence of inverter modulation on DC side impedance is explained by considering the scenarios of instantaneous m_a =0 and m_a=1. When m_a=0, AC side impedance reflection on the DC side is infinite. At m_a=1, the AC and DC side impedances are the same as per (4.10). With the computed equivalent DC impedance, the individual inverter DC bus current can be modeled as follows:

$$i_{dc_r} = \frac{V_{dce_r}}{Z_{dce_r}} = \frac{v_{d_{sw_r}} \cos(\delta - \psi) + v_{q_{sw_r}} \sin(\delta - \psi)}{(R_{dc} \cos(\delta - \psi) + X_{Ldc} \sin(\delta - \psi))/2} \tag{4.11}$$

Here V_{dce_r} is the AC voltage reflections on the current axis ($d_i - axis$), computed using (4.4) and (4.5). Similarly, Z_{dce_r} is the impedance (Z_{dc}) reflections on the current axis. For inverter-1, the (4.4), (4.5) and(4.11) can be expressed as

$$v_{d_{sw_1}} = \frac{2}{3}\frac{V_{dc}}{2}(S_{a_1} \cos(\theta) + S_{b_1} \cos(\theta - 2\pi/3) + S_{c_1} \cos(\theta + 2\pi/3)) \tag{4.12}$$

$$v_{q_{sw_1}} = \frac{2}{3}\frac{V_{dc}}{2}(S_{a_1} \sin(\theta) + S_{b_1} \sin(\theta - 2\pi/3) + S_{c_1} \sin(\theta + 2\pi/3)) \tag{4.13}$$

$$i_{dc_1} = \frac{V_{dce_1}}{Z_{dce_1}} = \frac{v_{d_{sw_1}} \cos(\delta) + v_{q_{sw_1}} \sin(\delta)}{(R_{dc} \cos(\delta) + X_{Ldc} \sin(\delta))/2} \tag{4.14}$$

The $v_{d_{sw_1}} \cos(\delta)$ and $v_{q_{sw_1}} \sin(\delta)$ term can be expanded as

$$\begin{aligned} v_{d_{sw_1}} \cos(\delta) = \frac{2}{3}\frac{V_{dc}}{2}[&S_{a_1} \cos(\theta).\cos(\delta) + S_{b_1} \cos(\theta - (2\pi/3)).\cos(\delta) \\ &+ S_{c_1} \cos(\theta + (2\pi/3)).\cos(\delta)] \end{aligned} \tag{4.15}$$

$$\begin{aligned} v_{q_{sw_1}} \sin(\delta) = \frac{2}{3}\frac{V_{dc}}{2}[&S_{a_1} \sin(\theta).\sin(\delta) + S_{b_1} \sin(\theta - (2\pi/3)).\sin(\delta) \\ &+ S_{c_1} \sin(\theta + (2\pi/3)).\sin(\delta)] \end{aligned} \tag{4.16}$$

Adding (4.15) and (4.16) as:

$$\begin{aligned} v_{d_{sw_1}}\cos(\delta)+v_{q_{sw_1}}\sin(\delta) = \frac{2}{3}\frac{V_{dc}}{2}[&S_{a_1}(\cos(\theta).\cos(\delta)+\sin(\theta).\sin(\delta)) \\ &+ S_{b_1}(\cos(\theta-(2\pi/3)).\cos(\delta)+\sin(\theta-(2\pi/3)).\sin(\delta)) \\ &+ S_{c_1}(\cos(\theta+(2\pi/3)).\cos(\delta)+\sin(\theta+(2\pi/3)).\sin(\delta))] \end{aligned} \quad (4.17)$$

The (4.17) can be written in composed form as

$$\begin{aligned} v_{d_{sw_1}}\cos(\delta)+v_{q_{sw_1}}\sin(\delta) = \frac{2}{3}\frac{V_{dc}}{2}(&S_{a_1}\cos(\theta-\delta)+S_{b_1}\cos(\theta-(2\pi/3)-\delta) \\ &+ S_{c_1}\cos(\theta+(2\pi/3)-\delta)) \end{aligned} \quad (4.18)$$

Expanding the term $(R_{dc}\cos(\delta)+X_{Ldc}\sin(\delta))/2$

$$\begin{aligned} (R_{dc}\cos(\delta)+X_{Ldc}\sin(\delta))/2 &= \frac{1}{2m_a}(R\cos(\delta)+X_L\sin(\delta)) \\ &= \frac{1}{2m_a}\left(R.\frac{R}{Z}+X_L.\frac{X_L}{Z}\right) = \frac{1}{2m_a}\left(\frac{R^2+X_L^2}{Z}\right) \\ &= \frac{1}{2m_a}(\frac{Z^2}{Z}) = \frac{Z}{2m_a} = \frac{X_L}{2m_a\sin(\delta)} \end{aligned} \quad (4.19)$$

Dividing (4.17) by (4.19) gives the DC link current as

$$i_{dc_1} = \frac{2}{3}\frac{m_a V_{dc}\sin(\delta)}{X_L}[S_{a_1}\cos(\theta-\delta)+S_{b_1}\cos(\theta-\delta-2\pi/3)+S_{c_1}\cos(\theta-\delta+2\pi/3)] \quad (4.20)$$

For both the inverters of the dual inverter, the DC link current expression can be written in a composed form as

$$\begin{aligned} i_{dc_r} = \frac{2}{3}\frac{m_a V_{dc}\sin(\delta)}{X_L}&[S_{a_r}\cos(\theta-\delta-\psi)+S_{b_r}\cos(\theta-\delta-2\pi/3-\psi) \\ &+ S_{c_r}\cos(\theta-\delta+2\pi/3-\psi)] \end{aligned} \quad (4.21)$$

Where ψ is the phase shift between the two inverters. For inverter-1, r=1 and ψ=0 while for inverter-2 r=2 and $\psi = \pi$. Using (4.21), the DC bus current can be computed as a function of inverter switching, modulation index, DC bus voltage, and motor loading condition. As it is depicted in (4.20), the DC bus current is a function of the overall modulation index, motor loading (Z), and individual inverter switching states. Thus the DC capacitor current is the function of individual switching states, and it can be modeled as :

$$
\begin{aligned}
i_{c_r} &= i_{dcs}(Avg\ source\ current) - i_{dc}(DC\ link\ current) \\
&= \frac{1}{2}\frac{m_a^2 V_{dc}\cos(\delta-\psi)}{Z} - \frac{2}{3}\frac{m_a V_{dc}}{Z}F_d(.) \\
&= \frac{2}{3}\frac{m_a}{\sqrt{R^2+X_L^2}}(\frac{3}{4}m_a V_{dc}\cos(\delta-\psi) - V_{dc}F_d(.))
\end{aligned} \tag{4.22}
$$

$$
F_d(.) = [(S_{a_r})\cos(\theta-\delta-\psi) + (S_{b_r})\cos(\theta-\delta-(2\pi/3)-\psi) + (S_{c_r})\cos(\theta-\delta+(2\pi/3)-\psi)]
$$

Where i_{dcs} is the average DC source current and i_{c_r} is the DC capacitor current. From (4.22), it is evident that the instantaneous switching states define the DC capacitor current at a given motor loading condition. Therefore, active and null switching states in a sampling time interval define the polarity of the capacitor current, explained in the subsequent section. In any switching sequence, the instantaneous voltage ripple can be derived from the instantaneous capacitor current as:

$$
\Delta V_{dc_r} = \frac{1}{C}\int (i_{c_r})dt \tag{4.23}
$$

Here ΔV_{dc_r} represents the instantaneous DC voltage ripple and C represents the DC link capacitance at the individual DC bus of the dual inverter. With the computed DC voltage ripple, the input source current ripple variations are explained by considering the null switching states of the inverter. At the null switching state, the AC load is isolated from the DC bus, forcing the available source current to flow to the DC capacitor, which reflects as a raised instantaneous capacitor voltage. Correspondingly, the current from the source reduces with the negative slope compared to the DC bus voltage. Similarly, in the active state, the drop in the slope of the DC voltage ripple reflects the instantaneous rise in the source current. Therefore, the source current ripple can be modeled as follows:

$$
\Delta i_{dcs_r} = \frac{1}{R_s C}\int (-i_{c_r})dt \tag{4.24}
$$

Here, Δi_{dcs_r} represents the instantaneous DC source current ripple at the individual DC bus of the dual inverter. As per the (4.22) and (4.23), the voltage ripple is influenced by the load current, whereas the load current ripple is dependent on the instantaneous phase voltage error magnitudes. In a dual inverter with an isolated DC bus, placing an effective time in the opposite corner of the sampling time interval yields the minimum load current ripple. At minimum load, the current ripple yields effective time placement; the placement of the active time sequence influences the DC voltage ripple. Therefore realization of the appropriate sequence for minimum DC bus voltage ripple is explained in the following section.

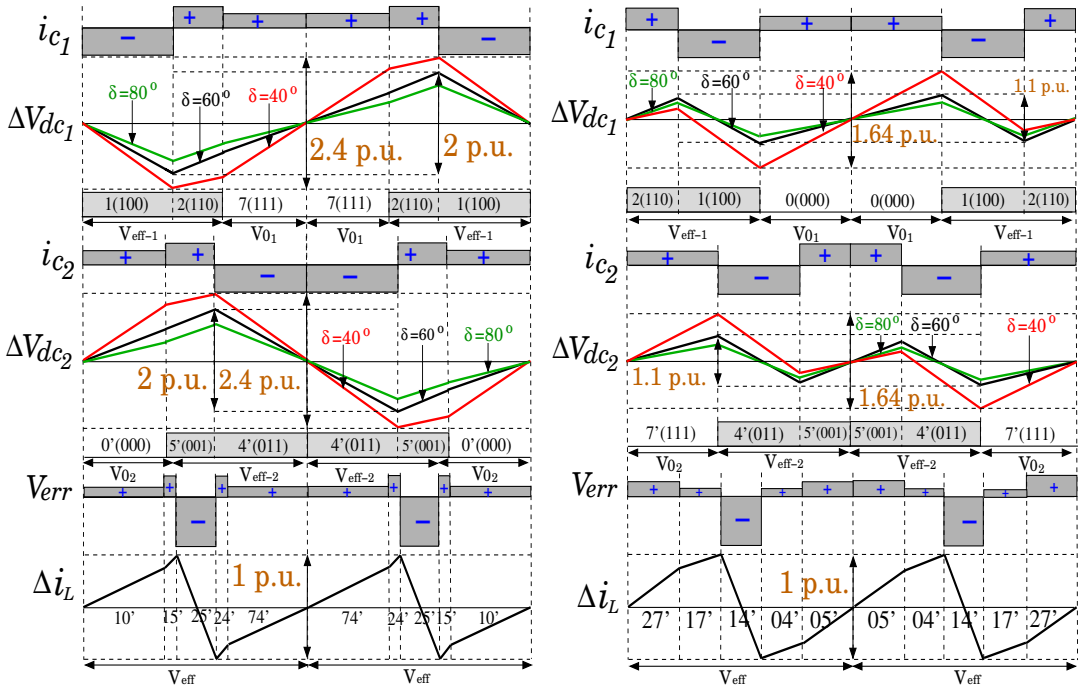
4.3 The influence of effective and null time placement on the DC bus voltage ripple

The instantaneous switching states define the instantaneous capacitor current magnitude as per (4.22), and the sequence of switching states defines the overall peak-to-peak magnitude of the DC bus voltage ripple. The selection of the switching sequence must be based on the capacitor current polarity. The influence of the switching sequence on the DC bus voltage ripple peak to peak magnitude is analyzed by considering the following two possible switching sequences:,

- (i_c) Same sign consecutive placement (SSCP) method
- (i_c) Opposite sign consecutive placement (OSCP) method

To realize the SSCP (conventional) and OSCP sequencing, it is required to compute capacitor current polarity in each sampling time interval (at each position of the space vector) and place them based on the capacitor current polarity, which is illustrated in subsequent subsections.

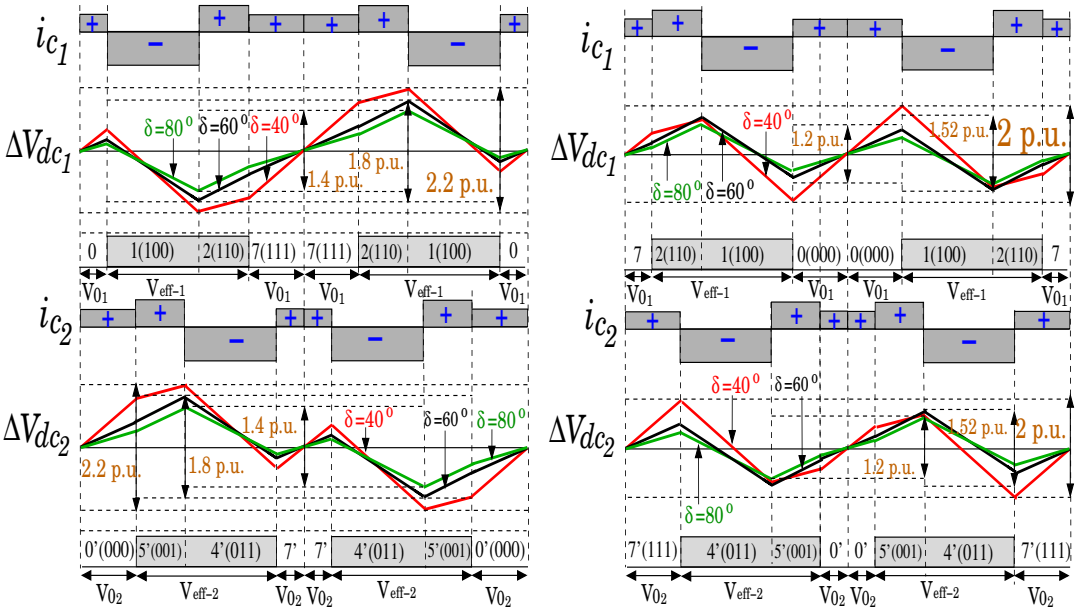
4.3.1 Same sign consecutive placement (SSCP) method



(a) SSCP switching (p=0 and q=1) (b) OSCP switching (p=0 and q=1)

Figure 4.5: The capacitor current magnitude variations and corresponding voltage ripple variations of inverter-1 (first and second trace) and inverter-2 (third and fourth trace) with the switching states of inverter and the load current ripple variation in dual inverter with the discontinuous PWM (bottom trace) (p=0 and q=1)

At p=0 and q=1, the effective time of inverter-1 and inverter-2 are placed in either corner of the sampling time interval as shown in Fig. 4.5. Upon computation of the capacitor



(a) SSCP switching (p=0.3 and q=0.7) (b) OSCP switching (p=0.3 and q=0.7)

Figure 4.6: The capacitor current magnitude variations and corresponding voltage ripple variations of inverter-1 (first and second trace) and inverter-2 (third and fourth trace) at p=0.3 and q=0.7

current polarity in the SSCP method, the switching states with the same sign capacitor current are placed consecutively, as depicted in Fig. 4.5(a) for inverter-1 and inverter-2. For inverter-1, the switching state V_1 gives the negative polarity (-) capacitor current computed using (4.22), while the state V_2 and V_7 gives the positive polarity (+) capacitor current. In the SSCP switching methodology, the same sign-yielding switching states are placed together, and the switching sequence is followed as $V_1 - V_2 - V_7$ (-++). Similarly, inverter-2 uses the switching sequence $V_{0'} - V_{5'} - V_{4'}$ (++-) and keeps the same polarity capacitor current yielding switching state simultaneously. With this method, the DC bus voltage ripple is 2 p.u. at $\theta = 15^o$ and δ= 60^o as shown in Fig. 4.5(a).

4.3.2 Opposite sign consecutive placement (OSCP) method

In the OSCP method, after computation of the polarity of the capacitor current, the switching states with the opposite polarity capacitor current are placed consecutively, as depicted in Fig. 4.5(b) for both inverter-1 and inverter-2. The switching sequence $V_2 - V_1 - V_0$ (+-+) and $V_{7'} - V_{4'} - V_{5'}$ (+-+) are used for switching of dual inverter in OSCP method. The OSCP method with the opposite polarity capacitor current yield switching stated placed together, only exhibits 1.1 p.u. of the DC bus voltage ripple in both inverters at $\theta = 15^o$ and $\delta = 60^o$ as depicted in Fig. 4.5(b). It can be further observed from Fig. 4.5(a) and Fig. 4.5(b) that the OSCP method yields a lesser DC voltage ripple than the SSCP method.

Similarly, the variation of DC voltage ripple at unequal null time segregation (p=0.3 and q=0.7) is shown in Fig. 4.6. From Fig. 4.6 it is observed that the OSCP switching gives the lesser DC bus voltage ripple as compared to SSCP switching at all load angles (δ).

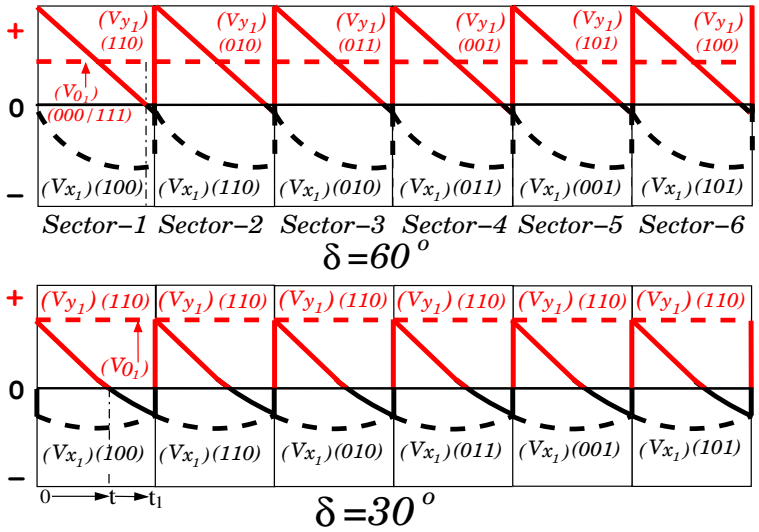
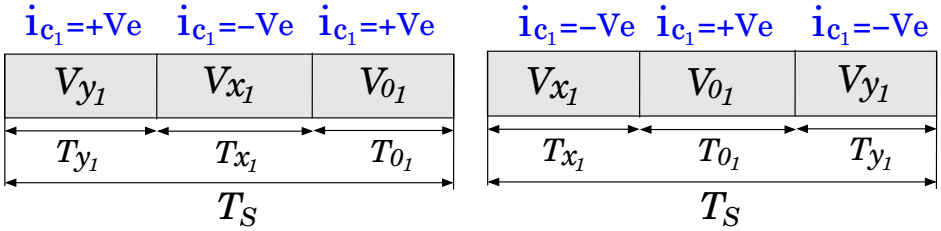


Figure 4.7: The DC capacitor current i_{c_1} variation with the switching state correspond to V_{x_1}, V_{y_1} and V_{0_1} in each sector at $\delta = 60^o$ (top trace) and $\delta = 30^o$ (bottom trace)

As the reference vector is composed of three switching vectors in an average sense, in this work, it is observed that the switching state behind the space vector (V_{x_1} referring Fig. 4.2) exhibits the negative i_{c_1} and null vector (V_{0_1}) exhibits the positive i_{c_1} magnitudes always. However, the switching vector ahead of the space vector (V_{y_1}) in each inverter changes its polarity depending on the power factor angle, as shown in Fig. 4.7. The variations of the capacitor current with three switching states V_{x_1}, V_{y_1}, and V_{0_1} in a fundamental cycle at $\delta = 60^o$ and 30^o are shown in Fig. 4.7. From Fig. 4.7, it is evident that the computation of polarity of i_{c_1} corresponds to the switching vector V_{y_1} is sufficient to derive the optimum switching sequence depending upon the power factor angles as follows:

1. (Seq-1) If the capacitor current i_{c_1} corresponds to V_{y_1} is positive $\Longrightarrow$ the switching sequence in a sampling time interval is V_{y_1} (+ve), V_{x_1} (-ve) and V_{0_1} (+ve) as shown in Fig. 4.8(a).

2. (Seq-0) if the V_{y_1} exhibits the negative i_{c_1}, the sequence must be V_{x_1} (-ve), V_{0_1} (+ve) and V_{y_1} (-ve) as depicted in Fig. 4.8(b).



(a) Seq-1 (b) Seq-0

Figure 4.8: Deriving the switching sequence with the proposed OSCP method for seq=1 (i_{c_1} of V_{y_1} is positive) and seq=0 (i_{c_1} of V_{y_1} is negative))

Based on the requirement of only computing the capacitor current polarity ahead of the space vector, a signal flow diagram for the algorithm to derive the switching sequence

dynamically at each sampling time interval for both the inverter is shown in Fig. 4.9. The proposed switching sequence is realized from the phase voltages by simply shifting

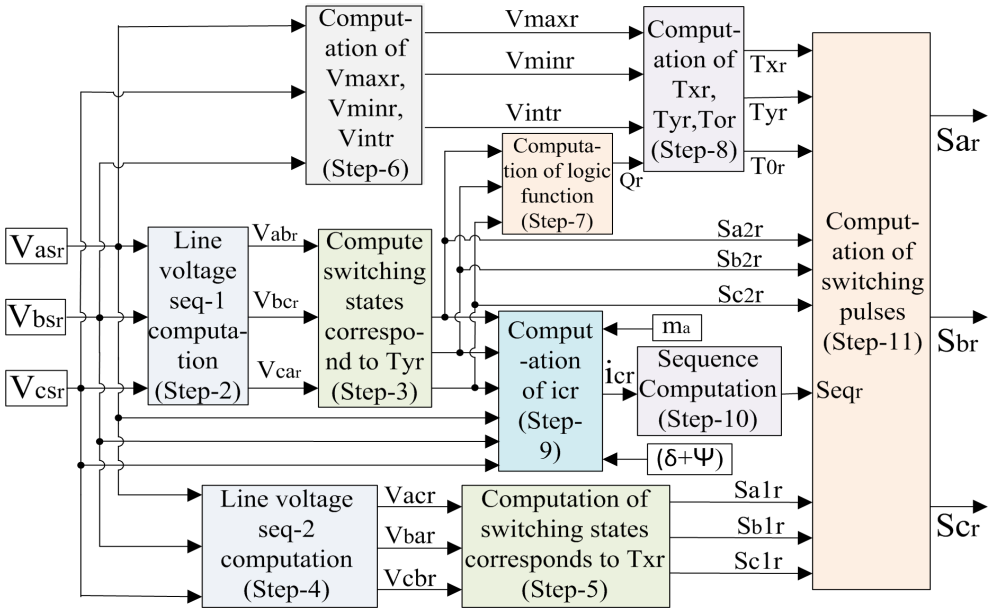


Figure 4.9: Block diagram representation of DC bus voltage ripple minimization algorithm for dual inverter

and segregating the effective and null times in a sampling time interval (T_s). To realize the optimum DC bus voltage ripple, the capacitor current polarity of the switching state ahead of the reference vector is computed to derive the dynamic sequencing of the switching states. In order to compute the capacitor current polarity of the switching vector ahead of the reference vector, The switching state information is necessary. The switching state information is computed by simply phase shifting the reference voltage by 30^o lagging. The detailed step-by-step switching sequence realization procedure is shown in Fig. 4.9, and each step is illustrated in the algorithm.

Step-1: Generate the reference phase voltages correspond to space vector of inverter-1 and inverter-2 (V_{as_r},V_{bs_r},V_{cs_r} for example V_{as_r}= $(V_{ref}/2)$ $\cos(\theta + \psi)$; for inverter-1 r=1 and $\psi = 0$, similarly for inverter-2 r=2 and $\psi = \pi$; The b-phase and c-phase are +/-120^o from the a-phase as ahown in top trace of Fig. 4.10.

Steps 2 to 9 are common for both inverters after generating reference three-phase voltages from the load space vector.

Step-2: Shift the phase voltages by 30^o to compute the binary switching states for each leg (S_{a2_r}, S_{b2_r}, S_{c2_r}) corresponding to voltage vector V_{y_r} as shown in second trace of Fig. 4.10.

$$V_{ab_r} = V_{as_r} - V_{bs_r}, V_{bc_r} = V_{bs_r} - V_{cs_r}, V_{ca_r} = V_{cs_r} - V_{as_r}$$

T_{count} is counter counts from 0 to T_s. Step 10 ensures the appropriate switching state placement.

Step-3: Compute the switching states corresponding to T_{y_r}

if $V_{ab_r} = +ve$, $S_{a2_r} = 1$ else $S_{a2_r} = 0$
if $V_{bc_r} = +ve$, $S_{b2_r} = 1$ else $S_{b2_2} = 0$
if $V_{ca_r} = +ve$, $S_{c2_r} = 1$ else $S_{c2_r} = 0$

Step-4: Shift the phase voltages by -30^o to realize the binary switching states (S_{a1_r}, S_{b1_r}, S_{c1_r}) correspond to V_{x_r} as shown in third trace of Fig. 4.10.

$$V_{ac_r} = V_{as_r} - V_{cs_r}, V_{ba_r} = V_{bs_r} - V_{as_r}, V_{cb_r} = V_{cs_r} - V_{bs_r}$$

Step-5: Compute the switching states corresponding to T_{x_r}

if $V_{ac_r} = +ve$, $S_{a1_r} = 1$ else $S_{a1_r} = 0$
if $V_{ba_r} = +ve$, $S_{b1_r} = 1$ else $S_{b1_r} = 0$
if $V_{cb_r} = +ve$, $S_{c1_r} = 1$ else $S_{c1_r} = 0$

Step-6: Compute the maximum (V_{max_r}) minimum (V_{min_r}) and intermediate (V_{int_r}) phase voltage magnitudes for switching sequence realization referring to bottom trace of Fig. 4.10.

$$\begin{aligned} V_{max_r} &= Max(V_{as_r}, V_{bs_r}, V_{cs_r}) \\ V_{min_r} &= Min(V_{as_r}, V_{bs_r}, V_{cs_r}) \\ V_{int_r} &= -V_{max_r} - V_{min_r} \end{aligned}$$

Step-7: Compute the logic function (Q_r) from switching states correspond to V_{y_r} for switching sequence evaluation

$$Q_r = S_{a2_r}S_{b2_r} + S_{b2_r}S_{c2_r} + S_{c_r}S_{a2_r}$$

Step-8: Compute the dwell times T_{x_r}, T_{y_r} and T_{0_r} correspond to V_{x_r},V_{y_r},V_{0_r}

if Q_r==*1* **then**
  $T_{x_r} = (2T_s/V_{dc})(V_{max_r} - V_{int_r})$;
  $T_{y_r} = (2T_s/V_{dc})(V_{int_r} - V_{min_r})$;
  $T_{0_r} = (2T_s/V_{dc})((V_{dc}/2) - (V_{max_r} - V_{min_r}))$;
else
  $T_{x_r} = (2T_s/V_{dc})(V_{int_r} - V_{min_r})$;
  $T_{y_r} = (2T_s/V_{dc})(V_{max_r} - V_{int_r})$;
  $T_{0_r} = (2T_s/V_{dc})((V_{dc}/2) - (V_{max_r} - V_{min_r}))$;
end
Here T_s is sampling time interval ($V_{dc}/2$) is the DC bus voltage of the individual inverter.

Step-9: Compute the capacitor current magnitude only for switching states corresponding to V_{y_r}

$$\begin{aligned} i_c = (3/4)m_a\cos(\delta) - [cos(\delta)(S_{a2_r}V_{as_r} + S_{b2_r}V_{bs_r} + S_{c2_r}V_{cs_r})sin(\delta)(S_{a2_r}\sqrt{1 - V_{as_r}^2} \\ + S_{b2_r}\sqrt{1 - V_{bs_r}^2} + S_{c2_r}\sqrt{1 - V_{cs_r}^2})] \end{aligned}$$

Step-10: Compute the sequence order logic based on the capacitor current polarity i_{c_r}

if $i_{c_r} = +ve$, $seq_r = 1$ else $seq_r = 0$

Step-11: Fill switching states with the computed dwell times in a sampling time interval based on the derived sequencing order

if $seq_r == 1$ **then**
  if $T_{count} \geq 0$ && $T_{count} < T_{y_r}$ **then**
    $S_{a_r} = S_{a2_r}$; $S_{b_r} = S_{b2_r}$; $S_{c_r} = S_{c2_r}$;
  end
  if $T_{count} \geq T_{y_r}$ && $T_{count} < (T_{y_r} + T_{x_r})$ **then**
    $S_{a_r} = S_{a1_r}$; $S_{b_r} = S_{b1_r}$; $S_{c_r} = S_{c1_r}$;
  end
  if $T_{count} \geq (T_{y_r} + T_{x_r})$ && $T_{count} < (T_{0_r} + T_{x_r} + T_{y_r})$ **then**
    $S_{a_r} = 0$; $S_{b_r} = 0$; $S_{c_r} = 0$;
  end
else
  if $T_{count} \geq 0$ && $T_{count} < T_{x_r}$ **then**
    $S_{a_r} = S_{a1_r}$; $S_{b_r} = S_{b1_r}$; $S_{c_r} = S_{c1_r}$;
  end
  if $T_{count} \geq T_{x_r}$ && $T_{count} < (T_{0_r} + T_{x_r})$ **then**
    $S_{a_r} = 0$; $S_{b_r} = 0$; $S_{c_r} = 0$;
  end
  if $T_{count} \geq (T_{0_r} + T_{x_r})$ && $T_{count} < (T_{0_r} + T_{x_r} + T_{y_r})$ **then**
    $S_{a_r} = S_{a2_r}$; $S_{b_r} = S_{b2_r}$; $S_{c_r} = S_{c2_r}$;
  end
end

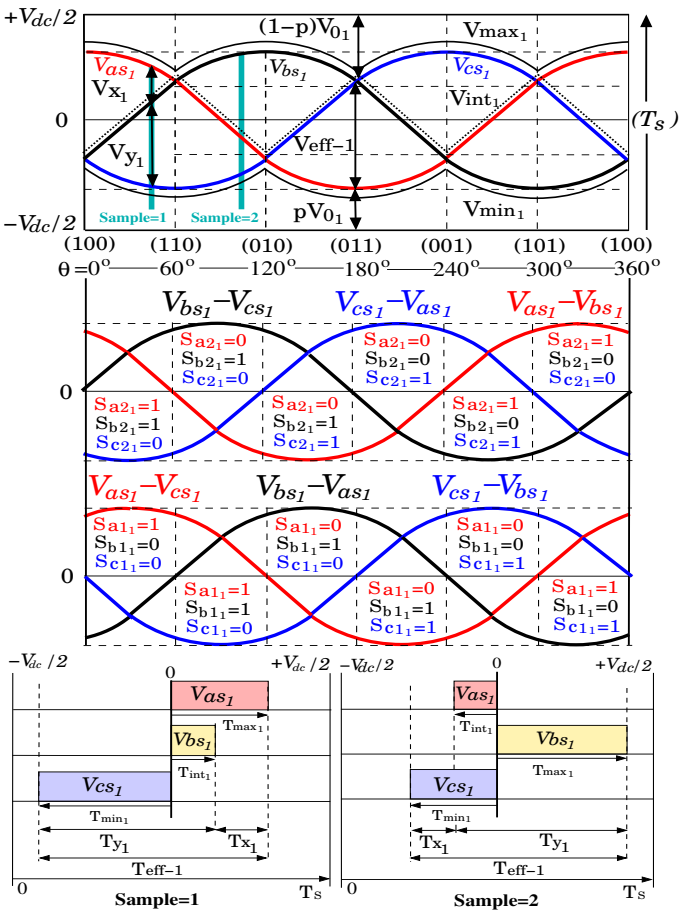


Figure 4.10: Top trace: The reference phase voltage, second trace: Generation of switching matrix for inverter-1 during T_{y_1}, third trace: Generation of switching matrix for inverter-1 during T_{x_1} and fourth trace: Computation of instantaneous T_{max_1}, T_{min_1} and T_{int_1} from the phase voltages

4.3.3 Designing of DC link capacitor

Consider the DC source current ripple for inverter-1 is Δi_{dcs_1}. The DC voltage ripple can be expressed as:

$$\Delta V_{dc_1} = R_s \Delta i_{dcs_1} \tag{4.25}$$

Where R_s is the DC source current ripple and ΔV_{dc_1} is the DC voltage ripple for inverter-1. During null switching state, all the DC source average current (i_{dcs_1}) will flow through the DC capacitor. In such a scenario, the DC capacitor current can be expressed as

$$i_{c_1} = i_{dcs_1} \tag{4.26}$$

Where i_{c_1} is the DC capacitor current for inverter-1. The generalized formula for capacitor current dynamics can be expressed as

$$i_c = C\frac{dV}{dt} \tag{4.27}$$

Where C is the DC capacitor value. For inverter-1, the (4.27) can be expressed as:

$$i_{c_1} = C\frac{\Delta V_{dc_1}}{m_a T_s} \tag{4.28}$$

Where m_a is the modulation index and T_s is the sampling time interval ($T_s = 1/F_s$). Where F_s is the switching frequency. Keeping (4.25), (4.26) in (4.28) and expanded to calculate the DC capacitance value as

$$C = \frac{m_a i_{dcs} T_s}{\Delta i_{dcs} R_s} \tag{4.29}$$

Keeping $m_a = 0.6$, $i_{dcs} = 0.4118$, $T_s = 1/2400$, $R_s = 1$ and $\Delta i_{dcs} = 0.09381$, the value of DC capacitor is coming out to be $C = 1097uf$. The value of DC capacitance is closed to 1200 uf. Due to this $C = 1200uf$ is chosen during experiment.

4.4 Results and Discussion

The proposed algorithm is tested on a dual inverter-based OEWIM drive fed from two isolated DC sources developed in the lab as shown in Fig. 4.11. Table- 4.1 shows the corresponding experimental operating parameters.

The hardware setup of the dual inverter-driven OEWIM was tested with V/F control at full load using the conventional SSCP and proposed OSCP switching. In order to show the efficacy of the proposed OSCP switching in deriving sinusoidal load current, the experimental validation is depicted in Fig. 4.12. The Fig. 4.12 shows the a-phase voltage and three-phase currents at null time placement using criteria p=0.5 and q=0.5 (left), p=0.7 and q=0.3 (middle), and p=1 and q=0 (right). From Fig. 4.12 it is evident that

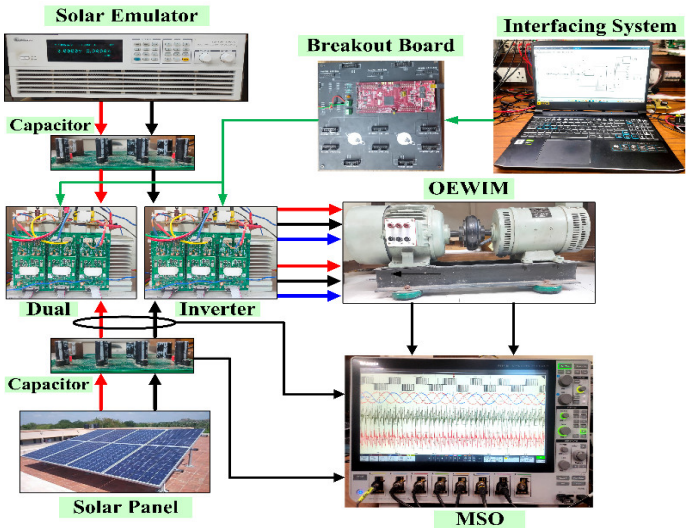
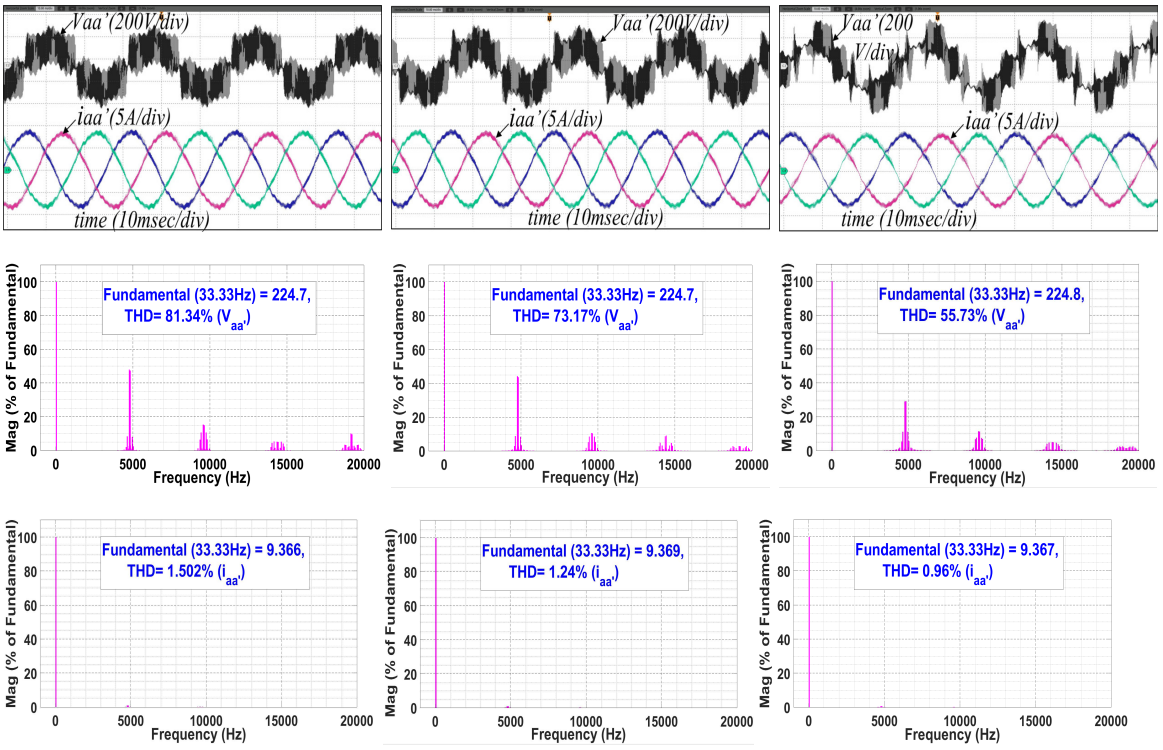


Figure 4.11: The dual inverter configuration lab experimental setup.

Table 4.1: Experimental parameters of dual inverter and OEWIM

Parameters	Symbols	Values	Units
Inverter Parameters			
DC Bus Voltage	$V_{dc_1} = V_{dc_2}$	295	Volt
Fundamental Frequency	F_0 (V/F)	33.33	Hz
Switching Frequency	F_s	2400	Hz
DC Link Capacitor	C_{dc}	1200	uf
Open end winding induction motor (OEWIM) parameters			
Power	P	5	HP
Line RMS voltage	$V_{LL(rms)}$	415	V
Rated current	I_{rms}	8.5	A
Rated speed	N_r	1440	RPM
Fundamental Frequency	F_o	50	Hz
Stator leakage inductance	L_s	22.48	mH
Stator resistance	R_s	4.835	Ω
Rotor leakage inductance	L_r	22.48	mH
Rotor resistance	R_r	4.835	Ω
Magnetising inductance	L_m	0.803	H
Magnetising resistance	R_m	768.93	Ω

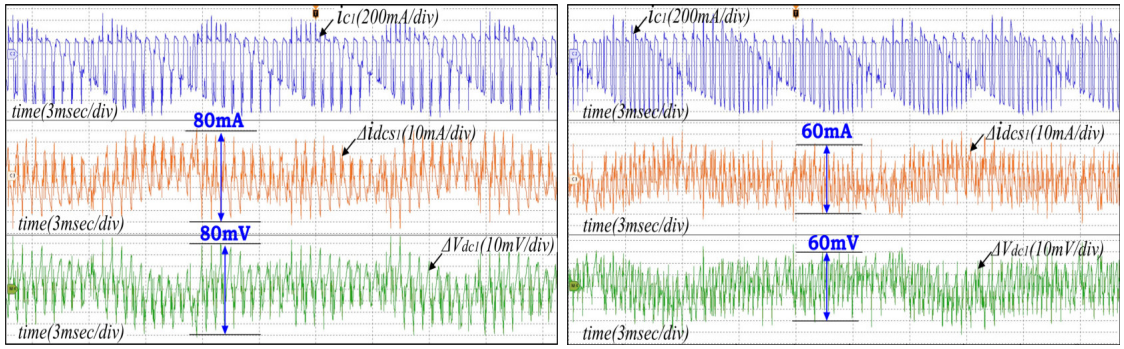


(c) p=0.5, q=0.5 (d) p=0.7, q=0.3 (e) p=1, q=0

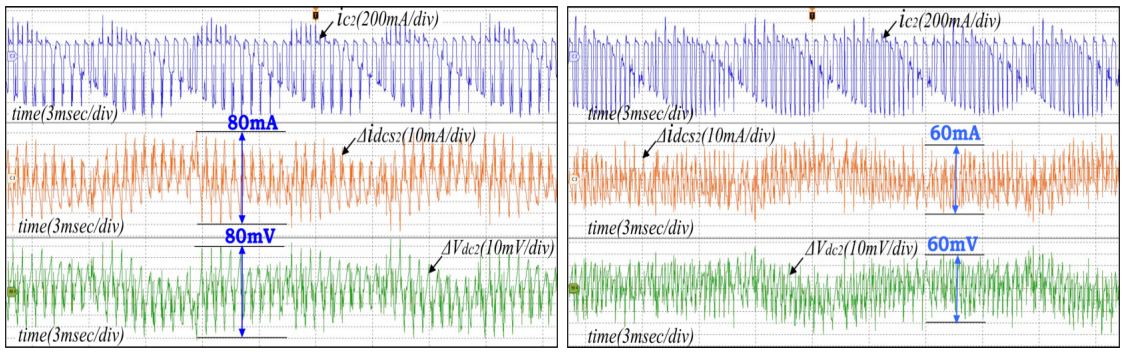
Figure 4.12: Experimental results of a-phase voltage (top trace), three-phase currents (second trace), FFT spectrum of phase voltage (third trace), and FFT spectrum of three-phase currents (Fourth trace) for proposed OSCP switching mechanisms.

the output phase voltage and currents total harmonic distortion (THD) is higher at p=0.5 (81.34% & 1.502%), moderate at p=0.7 (73.17% & 1.24%), and lowest at p=1 (55.73% & 0.96%). It confirms that the reduced %THD of phase voltage and phase current at p=1 (or p=0) i.e, placing the unsegregated null time on either side of the sampling time interval.

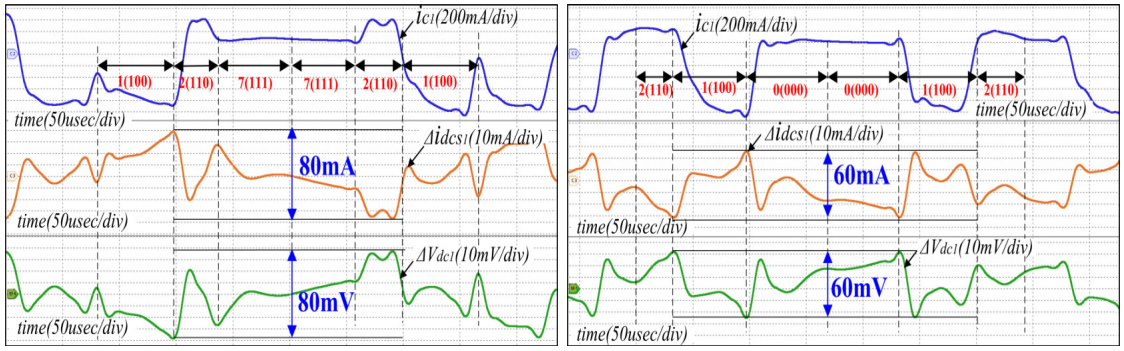
To demonstrate the influence of switching sequences, in this work, SSCP and OSCP are compared at no load and full load conditions by adjusting the null time in a sampling time interval through the appropriate selection of p and q. Fig. 4.13 describes the experimental ripple analysis by keeping unsegregated null time at the corner of the sampling time interval with p=0 and q=1. In this case, the DC capacitor current, the DC source current ripple and the DC bus voltage ripple are compared as shown in Fig. 4.13(a) and Fig. 4.13(b) for inverter-1 and inverter-2 with SSCP and OSCP switching respectively. With the proposed sequence, the DC source current ripple and DC bus voltage ripple are reduced to 60 mA from 80 mA and 60 mV from 80mV, respectively, compared to the conventional sequence (SSCP). It indicates the 25% reduction in the current ripple and voltage ripple in experimental validation as shown in Fig. 4.13. It means with conventional SSCP, to get the same DC source current ripple of OSCP, it is required to increase the capacitance value by 25% (from 1200 μF to 1600 μF). For clear visualization, zoomed portions of current and voltage ripple behavior of dual inverter at different switching states (at reference voltage



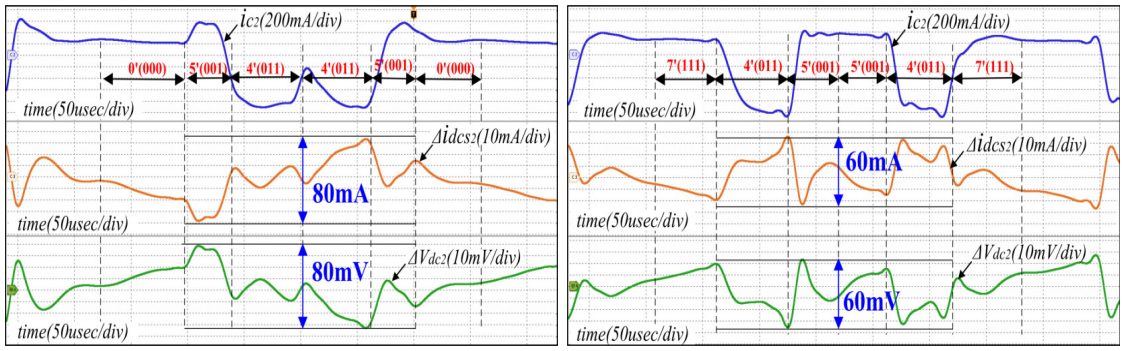
(a) The Inverter-1 DC capacitor current (top), source current ripple (middle) and DC voltage ripple (bottom).



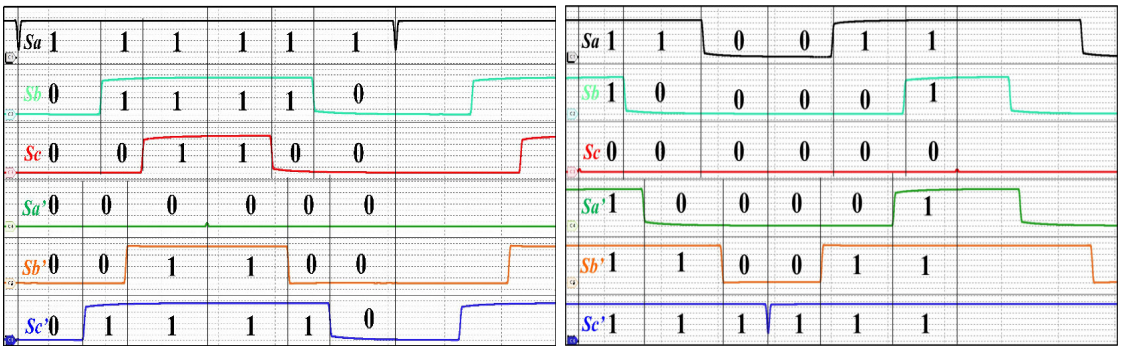
(b) The Inverter-2 DC capacitor current (top), source current ripple (middle) and DC voltage ripple (bottom).



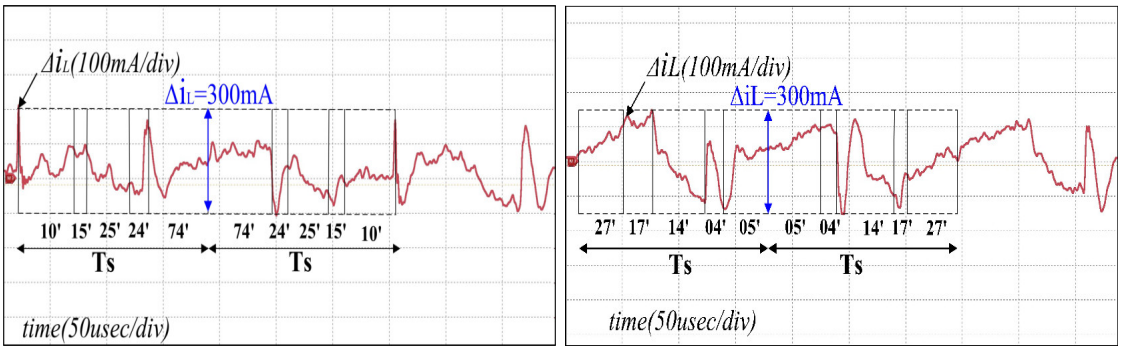
(c) The corresponding zoomed portion of Fig. 4.13(a).



(d) The corresponding zoomed portion of Fig. 4.13(b).

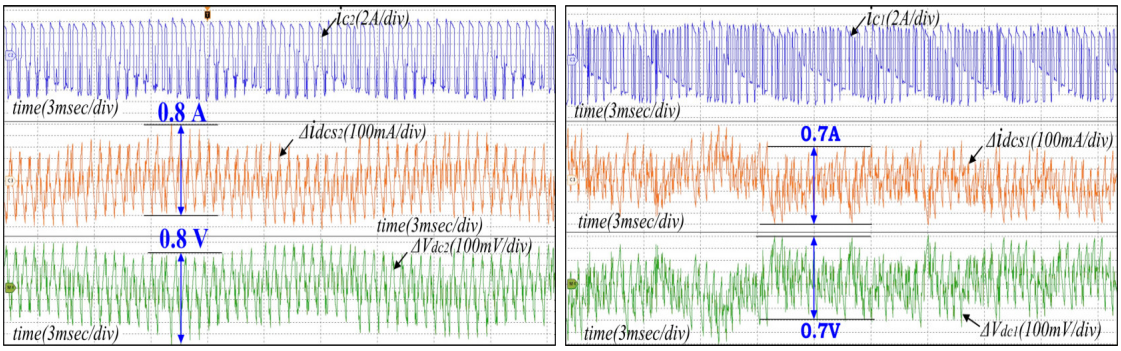


(e) The dual inverter switching pattern.

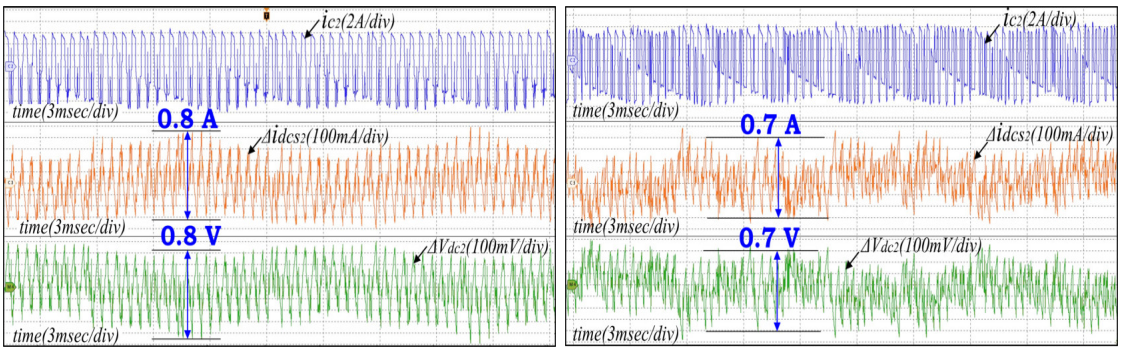


(f) The corresponding d-axis load current ripple.

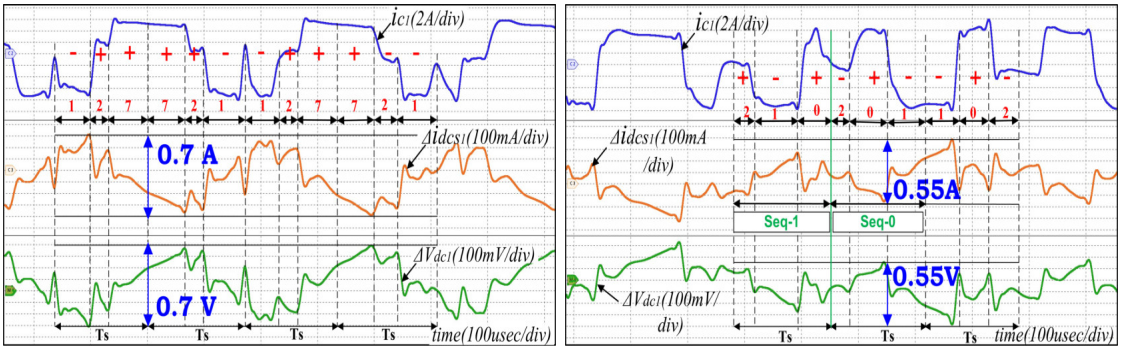
Figure 4.13: The experimental results with SSCP (left) and OSCP (right) switching by operating dual inverter drive with v/f control (frequency 33.33 HZ) at p=0 & q=1 in no-load condition.



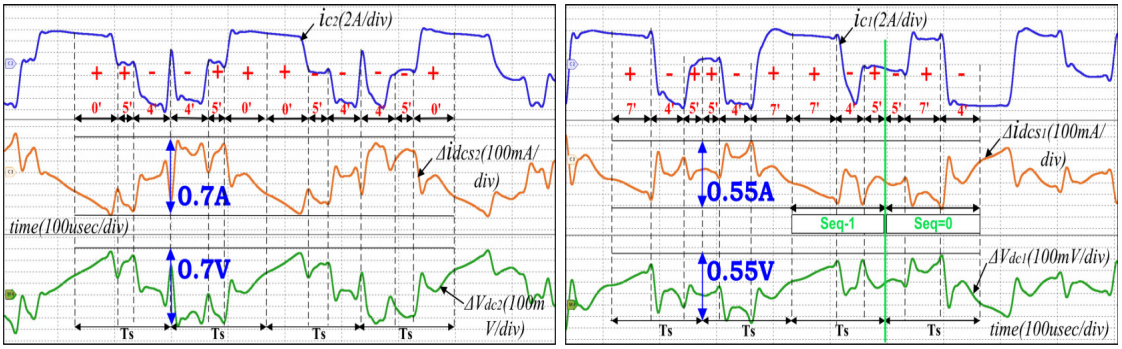
(a) The Inverter-1 DC capacitor current (top), source current ripple (middle) and DC voltage ripple (bottom)



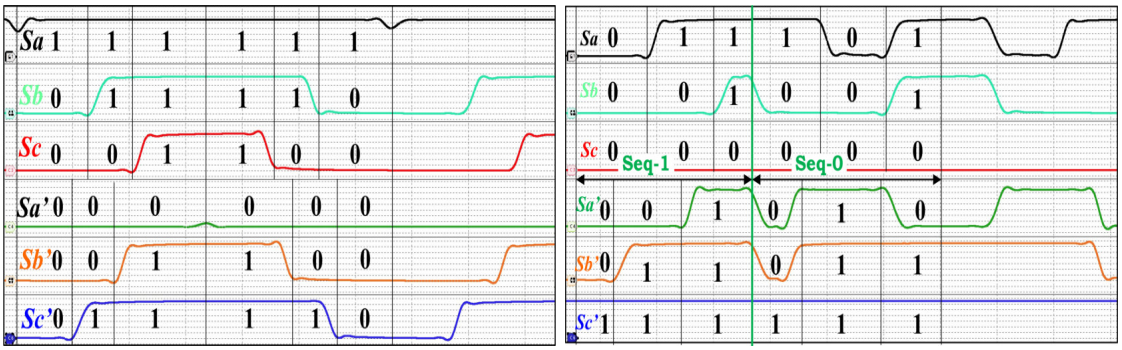
(b) The Inverter-2 DC capacitor current (top), source current ripple (middle) and DC voltage ripple (bottom)



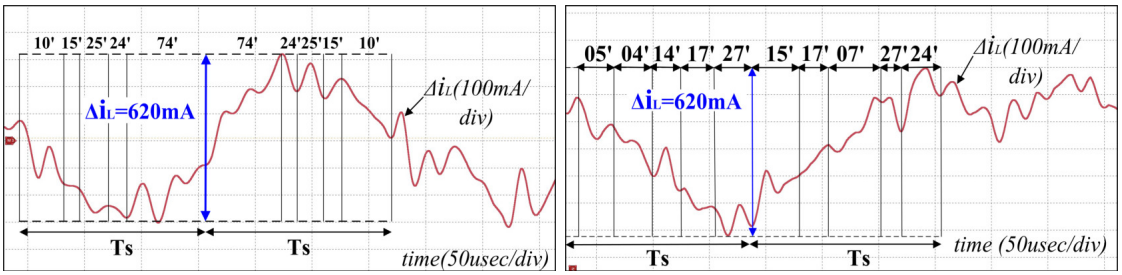
(c) The corresponding zoomed portion of Fig. 4.14(a)



(d) The corresponding zoomed portion of Fig. 4.14(b)



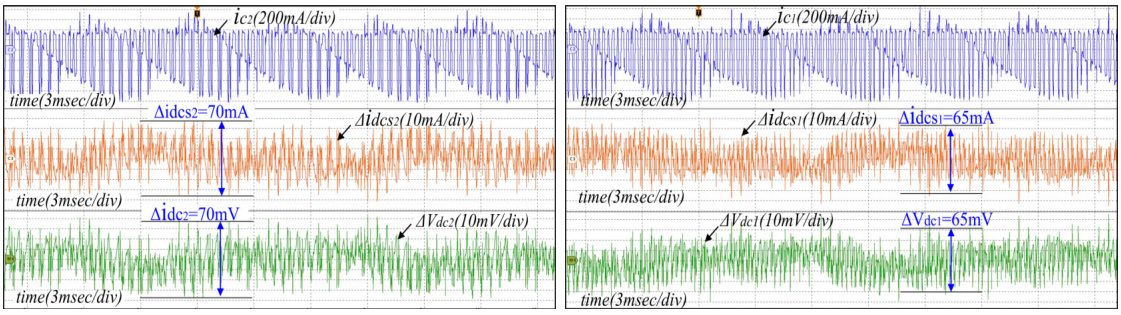
(e) The dual inverter switching pattern



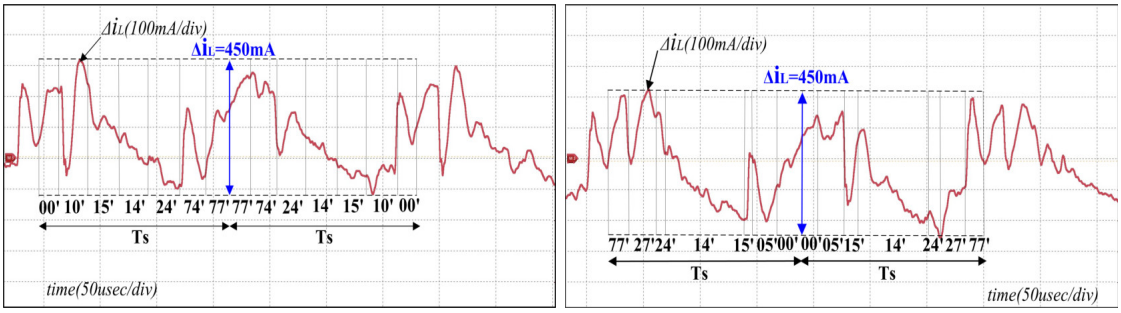
(f) The corresponding d-axis load current ripple

Figure 4.14: The experimental results with SSCP (left) and OSCP (right) switching by operating dual inverter drive with v/f control (frequency 33.33 HZ) at p=0 & q=1 in full-load condition.

angle $\theta = 15^o$) are shown in Fig. 4.13(c) and Fig. 4.13(d). From the zoomed portion, it is evident that the capacitor current pattern and voltage ripple pattern match with the theoretically analyzed capacitor current and voltage ripple patterns depicted in Fig. 4.5 in both SSCP and OSCP switching. As it is observed from Fig. 4.13(f), the load current ripple is unchanged in both SSCP (left) and OSCP (right) switching as claimed in this work. Similarly, at motor full load condition, the unsegregated null vector sequences i.e. SSCP and OSCP are further analyzed by comparing the DC capacitor current, DC source current ripple, and DC bus voltage ripple of inverter-1 and inverter-2 as shown in Fig. 4.14. At full load, the power factor angle is at $\delta = 28^o$. Based on the power factor angle, the switching algorithm automatically derives the switching sequence described in the preceding section to realize the lower voltage ripple as shown in Fig. 4.14(e). With the dynamic sequencing, the OSCP realizes the lower voltage and source current ripple compared to SSCP as demonstrated through Fig. 4.14(a) to Fig. 4.14(d). However, at full load, the DC bus voltage ripple decreases without influencing the current ripple as shown in Fig. 4.14(f). In order to show the superiority of unsegregated null time over the unequal null time segregation in terms of voltage ripple and source current ripple minimization, the experimental results are taken at p=0.3 & q=0.7 and shown in Fig. 4.15.



(a) The Inverter-1 DC capacitor current (top), source current ripple (middle) and DC voltage ripple (bottom)



(b) Zoomed portion of peak to peak load current ripple

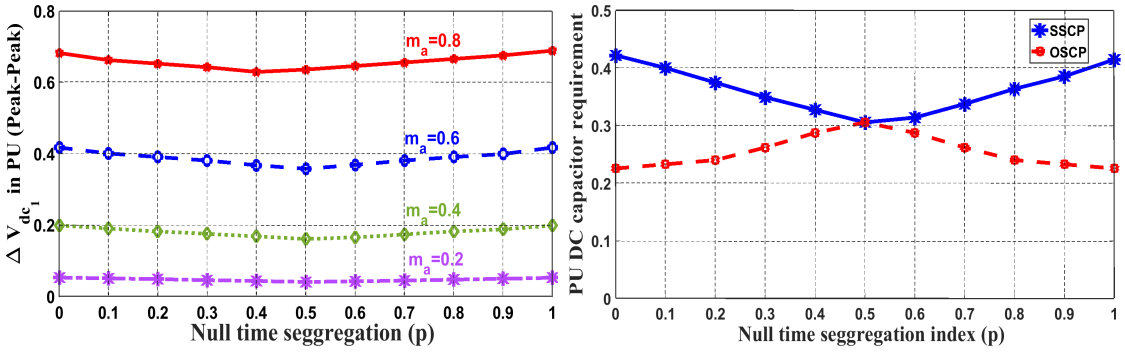
Figure 4.15: DC capacitor current(top trace), Source current ripple (middle trace) and DC voltage ripple (bottom trace) for inverter-1 (First figure), load current ripple at p=0.3 & q=0.7 operated in no load condition with speed of 1000 RPM for SSCP (left) and OSCP (right) switching.

It is observed from Fig. 4.15 that the DC voltage ripple is lesser in the case of OSCP switching as compared to SSCP switching at p=0.3 and q=0.7 while the load current

peak-to-peak ripple is same for both switchings. Further, with SSCP and OSCP sequences at different null time segregation are compared in terms of DC voltage ripple and DC source current ripple and presented in Table-4.2 at no load conditions. Table-4.2 confirms that the SSCP and OSCP yield the same current %THD at the unsegregated null time, but the minimum DC voltage ripple is generated from OSCP sequencing. At the same time, the conventional SSCP yields the maximum DC bus voltage ripple at the unsegregated null time. It confirms the superiority of the OSCP over the SSCP in reducing the DC bus voltage ripple without altering the AC current ripple.

Table 4.2: Variation of DC bus voltage ripple for SSCP and OSCP switching at No-load condition of OEWIM ($V_{dc_1} = 295V$ and $i_{dcs_1} = 0.4118A$)

p	ΔV_{dc_1} in mV		Δi_{dcs_1} in mA		% reduction	Load Current THD (SSCP & OSCP)
	SSCP	OSCP	SSCP	OSCP		
p=0	**93.81**	**60.77**	**93.81**	**60.77**	**35.20 %**	**4.761 %**
p=0.1	90.89	64.50	90.89	64.50	29.03 %	4.982 %
p=0.2	87.40	68.28	87.40	68.28	21.87 %	5.321 %
p=0.3	84.16	71.34	84.16	71.34	15.23 %	5.723 %
p=0.4	80.58	75.13	80.58	75.13	6.7 %	6.342 %
p=0.5	**77.72**	**77.72**	**77.72**	**77.72**	**0 %**	**7.633 %**
p=0.6	80.58	75.13	80.58	75.13	6.7 %	6.342 %
p=0.7	84.16	71.34	84.16	71.34	15.23 %	5.723 %
p=0.8	87.40	68.28	87.40	68.28	21.87 %	5.321 %
p=0.9	90.89	64.50	90.89	64.50	29.03 %	4.982 %
p=1	**93.81**	**60.77**	**93.81**	**60.77**	**35.20 %**	**4.761 %**



(a) (b)

Figure 4.16: (a)Variation of per unit peak to peak DC bus voltage ripple with varying p at different modulation index (m_a) for SSCP switching, ($\Delta V_{dc_1(base)} = 200mV$) (b)The comparison of peak to peak DC bus voltage ripple with the variation of p at $m_a = 0.6$ for SSCP and OSCP switching

Further, the DC capacitance requirement at different loading conditions and null time segregation are computed using the reference minimum DC voltage ripple condition (i.e., no load with OSCP condition) as tabulated in Table-4.3. From Table-4.3, it is clear that the OSCP (proposed sequence) demands lesser DC capacitance compared to SSCP at a

Table 4.3: Requirement of DC link capacitor in μF with respect to loading of OEWIM and null time segregation by considering the no load DC capacitor requirement at $p = 0$ and $q = 1$ as base value(cell top value corresponds to SSCP and cell down value corresponds to OSCP)

Loading / p and q	**No load (N.L.)**	**0.25 F.L.**	**0.5 F.L.**	**0.75 F.L.**	**Full load (F.L.)**
p=0,q=1	1857(μF) / 1200(μF)	3216(μF) / 2007(μF)	6686(μF) / 4970(μF)	10682(μF) / 9025(μF)	14931(μF) / 12865(μF)
p=0.3,q=0.7	1634(μF) / 1385(μF)	2768(μF) / 2140(μF)	5497(μF) / 3859(μF)	8128(μF) / 6140(μF)	10584(μF) / 9298(μF)
p=0.5,q=0.5	1354(μF) / 1354(μF)	2456(μF) / 2456(μF)	4697(μF) / 4697(μF)	6608(μF) / 6608(μF)	8401(μF) / 8401(μF)
p=0.7,q=0.3	1634(μF) / 1385(μF)	2768(μF) / 2140(μF)	5497(μF) / 3859(μF)	8128(μF) / 6140(μF)	10584(μF) / 9298(μF)
p=1,q=0	1857(μF) / 1200(μF)	3216(μF) / 2007(μF)	6686(μF) / 4970(μF)	10682(μF) / 9025(μF)	14931(μF) / 12865(μF)

given voltage ripple percentage. It can be further observed that the capacitance saving is maximum if the null time is unsegregated (p=0, q=1) and no change in the case of equal segregation (p=0.5 and q=0.5) as evident from the Table-4.3. The reason is that when p=0.5 and q=0.5, the null switching time is evenly distributed within the sampling time interval. Half of the null time is placed at the beginning of the sampling interval, and the other half is placed at the end. In the case of OSCP switching, the negative capacitor current-generating switching state should be positioned adjacent to the highest null time distribution. This helps reduce the DC bus voltage ripple, as shown in Fig. . However, at p=0.5 and q=0.5, the null states are evenly distributed. This means that the negative capacitor current-generating switching state can be placed next to any null time, as they are equally distributed. As a result, the DC voltage ripple generated in SSCP and OSCP switching will have the same magnitude at p=0.5 and q=0.5. For a consolidated comparison of SSCP and OSCP, the DC bus voltage ripple variation with different modulation indices by varying the null time segregation percentage is presented in Fig. 4.16. In this comparison, the same polarity capacitor current yield switching states are placed together (SSCP); thus, the minimum DC voltage ripple can be seen at equal null vector segregation (p=0.5) at all modulation indices as shown in Fig. 4.16(a). Whereas in the case of alternative capacitor current yield switching states (OSCP), the minimum voltage ripple can be seen at p=0 and q=1 (unsegregated null time) at all modulation compared to null time segregated PWMs; thus, the requirement of the DC

capacitor is reduced by 10% compared to SVPWM (p=0.5 and q=0.5), and 35% compare to unsegregated null time with SSCP as shown in Fig. 4.16(b).

4.5 Conclusion

This work presented in this chapter identifies that the DC voltage ripple and DC source current ripple in a dual inverter configuration is a function of individual inverter switching and motor impedance. The switching sequence dependency on the DC voltage ripple and DC source current ripple is studied by segregating null time and placing it at different locations along with the active vector in a sampling time interval. The analysis revealed that placing switching vectors with the alternative capacitor current along with the unsegregated null time yields the minimum DC voltage ripple and DC source current ripple. With the identified constraints to derive the minimum DC voltage and DC source current ripple, a new active and null vector placement methodology is proposed in this work. The proposed method is simplified by computing the polarity of only one switching vector as the null vector and another switching state always exhibit the unaltered capacitor current polarity. By following the proposed switching sequence, it is clearly identified that the DC capacitance value can be reduced to 12% ($\frac{0.8-0.7}{0.8} * 100$) at a given voltage ripple for OSCP switching with full load condition .

Chapter 5

Conclusion

In conclusion, this thesis successfully presents a comprehensive approach to analyze and minimize the DC link ripple for VSIs through innovative algorithms and methodologies. Chapter 1 lays the foundation by proposing a novel algorithm to select the minimum DC voltage ripple generating PWM. The approach begins with a detailed mathematical modeling of the DC capacitor current using d-q axes error voltage computation, projected onto the load reference frame. This modeling facilitates the identification of operating regions crucial for minimizing DC voltage ripple. Through exhaustive examination, it is found that DPWM-4 and SVPWM are the prime contenders for achieving minimal DC voltage ripple, with empirical validation demonstrating remarkable reductions. Through analysis and hardware results, it is identified that the SVPWM achieves a DC bus voltage ripple of 480 mV at $\delta = 30^o$, while DPWM-4 achieves 500 mV at $\delta = 60^o$, highlighting the practical applicability and effectiveness of the proposed algorithm.

Chapter 2 builds on this by demonstrating a DC bus voltage ripple computational method that exploits AC error voltage vector information for dual inverter with the common DC link. This model is independent of instantaneous current information, making it an offline model suitable for assessing PWM techniques for minimum voltage ripple. The method identifies that the AEVSS switching sequence yields a lower voltage ripple compared to the CEVSS sequence when load angle greater than 0^o and less than 90^o. This conclusion is supported by computing the voltage ripple RMS value at various modulations and loading conditions. The analysis confirms that using the AEVSS method reduces the required DC capacitor size by 35% compared to the CEVSS method to achieve the designated DC voltage ripple at m_a= 0.6 and $\delta = 60^o$. Considering the worst case scenario, the DC capacitor requirement is reduced by 8.82% at $\delta = 10^o$ and 27.16% at $\delta = 30^o$ for AEVSS switching compared to CEVSS switching.

Chapter 3 explores the relationship between DC voltage ripple, DC source current ripple, individual inverter switching, and motor impedance in a dual inverter configuration with separate DC link. The chapter studies the dependency of switching sequences on DC voltage ripple and DC source current ripple by segregating null time and placing it at different locations along with the active vector in a sampling time interval. The analysis reveals that placing switching vectors with alternative capacitor current along with unsegregated null time results in the minimum DC voltage ripple and DC source current ripple. Based on these insights, a new active and null vector placement methodology

is proposed. This method simplifies the computation process by requiring the polarity computation of only one switching vector as the null vector and other switching state maintains an unaltered capacitor current polarity. This approach demonstrates that the maximum DC capacitance value can be reduced by 35% with unsegregated null time distribution (p=0/1 and q=1/0) at m_a=0.6 and $\delta = 60^o$, whereas no reduction is observed with equal null time distribution (p=0.5 and q=0.5) with the proposed OSCP switching at a given voltage ripple. In worst case scenario, the DC capacitance can be reduced by 12% for OEWIM operating from dual inverter with separate DC link.

Overall, this thesis makes significant contributions to the field of power electronics and inverter design by presenting innovative methodologies and algorithms that effectively minimize DC voltage ripple. The findings underscore the practical applicability and efficiency of the proposed solutions, offering valuable insights for the design and optimization of three-phase, two-level voltage source inverters in real-world applications.

5.1 Scope of Future Research

1. **Exploration of DC Link Ripple Analysis:** Future research will delve into conducting DC link ripple analysis to explore its applicability in active filtering and enhancing fault ride-through capabilities. This investigation aims to understand how DC link ripple affects system performance and the potential for mitigating its effects through active filtering techniques and fault ride-through capability.

2. **Development of ESR Prediction Models:** Subsequent studies will focus on developing prediction models for the equivalent series resistance (ESR) of DC capacitors. This research endeavor seeks to establish reliable methods for estimating ESR values, which are crucial for assessing capacitor performance and ensuring optimal operation of power electronic systems.

3. **Life Analysis of DC Capacitors:** Future work will involve conducting life analysis studies on DC capacitors for both motor drive and grid-connected inverter applications. This analysis aims to investigate the longevity and reliability of DC capacitors under different operating conditions, providing insights into their suitability for specific applications and informing maintenance and replacement strategies.

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