Exploration of Gate-all-around MOSFETs for Digital, RF, and Neuromorphic Applications

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by

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Dedicated to My God, Family, and Mentors

Declaration of Originality

I hereby declare that the work which is being presented in the thesis entitled **Exploration of Gate-all-around MOSFETs for Digital, RF, and Neuromorphic Applications** has been solely authored by me. It presents the result of my own independent investigation/research conducted during the time period from Jan, 2021 to August, 2024 under the supervision of Dr. Brajesh Rawat, Assistant Professor, Department of Electrical Engineering. To the best of my knowledge, it is an original work, both in terms of research content and narrative, and has not been submitted or accepted elsewhere, in part or in full, for the award of any degree, diploma, fellowship, associateship, or similar title of any university or institution. Further, due credit has been attributed to the relevant state-of-the-art and collaborations (if any) with appropriate citations and acknowledgments, in line with established ethical norms and practices. I also declare that any idea/data/fact/source stated in my thesis has not been fabricated/ falsified/ misrepresented. All the principles of academic honesty and integrity have been followed. I fully understand that if the thesis is found to be unoriginal, fabricated, or plagiarized, the Institute reserves the right to withdraw the thesis from its archive and revoke the associated Degree conferred. Additionally, the Institute also reserves the right to appraise all concerned sections of society of the matter for their information and necessary action (if any). If accepted, I hereby consent for my thesis to be available online in the Institute's Open Access repository, inter-library loan, and the title & abstract to be made available to outside organizations.

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Anjali Goel

Certificate

This is to certify that the thesis entitled **Exploration of Gate-all-around MOSFETs for Digital, RF, and Neuromorphic Applications**, submitted by **Anjali Goel (2020EEZ0027)** for the award of the degree of **Doctor of Philosophy** of Indian Institute of Technology Ropar, is a record of bonafide research work carried out under my (our) guidance and supervision. To the best of my knowledge and belief, the work presented in this thesis is original and has not been submitted, either in part or full, for the award of any other degree, diploma, fellowship, associateship or similar title of any university or institution.

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Lay Summary

The need for Gate-All-Around (GAA) MOSFET arises from the ongoing effort to scale transistors in line with Moore's Law, which predicts the doubling of transistor density on integrated circuits (ICs) approximately every 18 to 24 months. As traditional MOSFET architectures, such as planar and Fin-FETs, struggle to scale down beyond the 5nm technology node, GAA MOSFET, including nanowire field-effect transistor (NW-FET) and nanosheet field-effect transistor (NS-FET), offer improved electrostatic control and reduced short-channel effects due to their innovative four-sided gate design that fully encloses the channel. This enables further miniaturization while maintaining performance and power efficiency. These architectures could allow the semiconductor industry to push the boundaries of Moore's Law by supporting smaller, faster, and more energy-efficient devices. However, a comprehensive evaluation of their performance is needed to assess their full potential.

Thesis analyzes the performance of GAA devices for digital, radio frequency (RF), and neuromorphic applications using fully calibrated three-dimensional technology computer-aided design (TCAD) simulations. The objective is to understand the behavior of these devices and contribute to the development of next-generation neuromorphic computing systems in the future technology node. The study begins with an in-depth analysis of the analog and RF performance of GAA devices for system-on-chip (SoC) and system-in-package (SiP). The analysis explores the impact of various design parameters, such as gate length, channel width/height, number of channels, and channel orientation. In addition, novel stacking architectures, such as forksheet (FSH) and complementary field-effect transistor (CFET) are investigated through process simulations to address design-technology co-optimization (DTCO) challenges, highlighting their advantages for scaling beyond the 5 nm technology node.

A distinctive aspect of this work is the detailed analysis of the neuronal and synaptic functionalities of nanowire field-effect transistors (NW-FETs) for neuromorphic applications. A key part of this investigation involves evaluating and implementing an artificial synapse using HfO_x-based nanowire charge trap transistor (NW-CTT), which aim to develop a highly scalable and CMOS-compatible neuromorphic computing system. Further, the assessment of NW-CTT is carried out by designing a fully CMOS-compatible spiking neural network for digital digit recognition. The thesis demonstrates the potential of GAA devices to deliver superior speed and energy efficiency for digital, RF, and neuromorphic applications.

Abstract

The dimensional and functional scaling of MOSFET dimensions has been a key enabler of advancements in the semiconductor industry, enhancing both performance and integration density. As MOSFET scaling approaches its fundamental physical limits, new material and architecture are being explored to sustain progress. Gate-all-around (GAA) devices, particularly nanowire (NW) and nanosheet (NS) FETs, have demonstrated exceptional switching performance, which positions them as strong candidates for ultra-scaled CMOS technology. Additionally, the charge-trapping mechanism in these devices offers a compelling opportunity to develop brain-inspired neuromorphic computing systems, which address the energy and speed constraints inherent in traditional von Neumann computer architecture. As experimental advancements in GAA devices accelerate, several key questions emerge regarding their integration into advanced circuits:

(i) What is the most promising GAA architecture for digital and radio frequency (RF) applications?

(ii) Which CMOS inverter stacking configuration with NS-FET provides the most significant performance improvements with high integration density at ultra-scaled gate lengths?

(iii) How can the charge-trap mechanism in NW-FETs be better utilized to achieve multiple stable states for emulating biological synapses?

(iv) Is it possible to develop energy-efficient and highly scalable spiking neural networks with NW-FET by exploiting the charge-trap mechanism?

The thesis work is focused on answering the above questions by performing device-to-circuit level co-optimization of GAA devices using a well-calibrated 3D TCAD tool, based on self-consistent solutions of the Boltzmann's transport equation and Poisson's equation with incorporating quantum corrections and mobility degradation effects. Initially, GAA devices, including NW-FET and NS-FET, are investigated for analog/RF applications and benchmarked against their Fin-FET counterparts. The findings indicate that NS-FET is well-suited for analog/RF applications due to their high voltage gain, superior cut-off frequency, and maximum oscillation frequency for sub-5 nm technology nodes. Subsequently, innovative CMOS inverter configurations, such as forksheet (FSH) and complementary FET (CFET), are explored in conjunction with nanosheet to develop high-speed and low-power digital ICs with high integration density.

This analysis demonstrates that CFET delivers optimal and robust switching performance in the inverter, SRAM, and ALU configurations at the ultimate scaling limit.

In the next phase, a systematic analysis was conducted to assess the viability of NW channel as charge-trap transistor (CTT) for emulating synapses at the 5 nm technology node. This study focuses on understanding the role of device parameters on short-term and long-term memory. Importantly, the nearly linear conductance modulation of NW-CTT as a synapse promises high recognition accuracy of around 94.7% and low write energy (2.3 mJ) in a neural network configuration (784 $\times$ 100 $\times$ 10) for handwritten digit recognition. Finally, the successful co-integration of neurons and synapses using NW-CTT is demonstrated for scalable neuromorphic hardware with CMOS-compatible processing techniques. The neurons and synapses are co-integrated to develop a spiking neural network, which exhibits noise-tolerant and energy-efficient recognition for handwritten digits. The comprehensive analysis suggests that NW-CTT presents a promising solution for high-density and low-power hardware implementations of brain-inspired spiking learning systems.

Keywords: Nanowire-FET; Nanosheet-FET; Forksheet; Complementary FET, Gate-all-around FET; CMOS Inverter; Neuron; Synapse; Spiking neural network

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Chapter 1

Introduction

The continuous scaling of complementary metal-oxide-semiconductor (CMOS) technology has been a key driver in the advancement of semiconductor processing techniques and the enhancement of the functionality of electronic devices. Over the past four decades, the dimensions of metal-oxide-semiconductor field-effect transistors (MOSFETs) have shrunk according to Moore's law. In the early phase, the miniaturization of bulk MOSFET has encountered several challenges, such as short-channel effects (SCEs), which lead to a loss of electrostatic integrity, high body doping, which results in increased threshold voltage (V_{Th}) variation, and band-to-band tunneling, which induces OFF-state leakage and substrate leakage currents [1]. To mitigate these limitations, MOSFETs have been extensively researched, which leads to innovations, such as strained semiconductors, silicon-on-insulator (SOI) technology, and ultra-thin body (UTB) SOI [2]. The demand for high performance and enhanced integration density has driven the scaling of nearly every device parameter, including channel length, gate dielectric thickness, body and substrate thickness, doping levels, and supply voltage [3]. The emergence of Fin-FET architecture at the 22-nm technology node has significantly enhanced the gate control over the channel region and enabled the device dimension scaling down to the 7-nm technology node [4]. However, Fin-FET is struggling to further scale down the channel length below the 7-nm technology node due to limitations in the electrostatic control and carrier mobility [5].

To ensure scaling and performance benefits, gate-all-around (GAA), particularly nanowire (NW) and nanosheet (NS) FETs, have emerged as promising device architectures for sub-5-nm technology nodes [6]. These advanced device architectures offer enhanced electrostatic control compared to Fin-FET, enabling continued transistor scaling. They also provide improved performance, operate at lower supply voltages, and exhibit reduced variability in threshold voltage (V_{TH}) due to their ability to function effectively with low channel doping [7]. NS-FET and NW-FET can be produced in two configurations: horizontal [8] and vertical [9]. Horizontal stacked NWs, as shown in Fig. 1.1, are used in the traditional 2-D layout, where space for contact and gate placement is restricted [10]. However, the vertical NW configuration shifts the layout from a 2D to a 3D structure, allowing a longer gate length without occupying a large area on the wafer. However, this approach requires extensive research into process design co-optimization. Especially,

NW-FET configuration necessitates significant spacing between adjacent nanowires, which poses major fabrication challenges and increases the aspect ratio of the entire channel stack [11]. Recent research on highly stacked NS-FET (see Fig. 1.1) indicates that vertical stacking channels can significantly boost drive current and transistor density and addresses the limitations associated with traditional NW-FET architectures [12]. These developments underscore a shift toward more complex nanosheet stacking arrangements, which promise enhanced performance while addressing the inherent challenges of scaling in semiconductor technology. Thus, while NW-FET and NS-FET present viable solutions to overcome short-channel effects and improve performance, ongoing research continues to explore innovative configurations that will be essential for meeting the demands of future electronic devices.

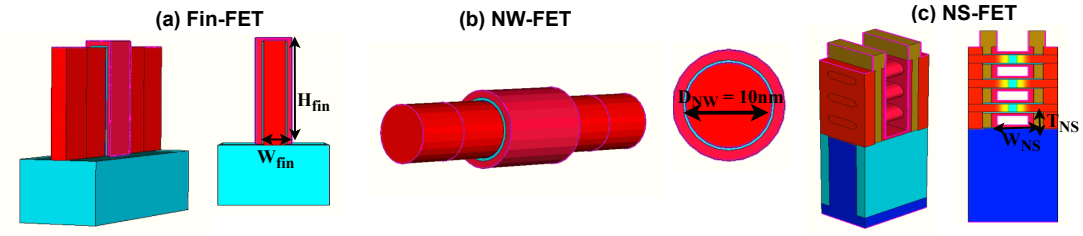

Figure 1.1: 3D schematic view along with cross-sectional channel-view of: (a) Fin-FET, (b) NW-FET and (c) NS-FET.

Remarkably, NS-FETs have demonstrated seamless integration into advanced electronic systems while addressing the challenge of integration density by implementing novel inverter configurations, such as Forksheet (FSH) and Complementary FET (CFET) [13, 14]. FSH architecture improves the integration density by using dielectric separation between n-type and p-type MOSFETs, allowing them to be placed closer together [15]. Meanwhile, CFET enables vertical stacking of these devices and further optimizes space and power efficiency [13]. These advances offer significant benefits, including reduced footprint, lower power consumption, and improved performance for high-speed digital circuits. However, several challenges remain, such as the complexity of fabricating these intricate structures, mitigating parasitic effects, and evaluating their performance in advanced logic circuits [16, 17]. Therefore, exploring the design and optimization of FSH and CFET architectures with Si NS-FETs presents a valuable opportunity to advance device performance and overcome the scaling limitations of next-generation semiconductor technologies.

Another emerging recent application is charge trap mechanisms in advanced transistor architectures, which can potentially develop the device for nonvolatile memory

applications and neuromorphic computing [18, 19]. Unlike conventional transistors, charge trap transistor (CTT) stores charge in a dielectric layer or a trap site within the gate dielectric, which can alter the threshold voltage of the device and allow multiple states to be stored [20]. This ability to retain information even when powered off makes them highly attractive for next-generation nonvolatile memory technology [21, 22, 23]. Moreover, CTT is gaining attention in neuromorphic computing, as its multilevel states can mimic the behavior of biological synapses. Recent developments have explored the implementation of charge trap mechanisms in planar and Fin-FET device architectures, which are highly susceptible to short-channel effects [18, 24]. This could exacerbate variability and reliability issues in neural network implementation [21]. Therefore, there is a pressing need for the advancement of synaptic and neuron characteristics with CTT, which can support technology scaling and enable the development of high-density neural networks.

1.1 Transistor Performance Metrics and Trade-offs

1.1.1 Digital Applications

Semiconductor devices are crucial in two main areas: digital integrated circuits (ICs) and radio-frequency (RF) ICs. Digital ICs comprise logic gates, including NOR and NAND gates, which use a combination of p-type and n-type transistors to perform specific logical functions. It is found that by controlling these gates, transistors act as switches, which allows high currents to pass when in the ”on” state and minimal currents in the ”off” state. Therefore, with a wide array of expectations and requirements, it is beneficial to define Figures of Merit (FOMs) that cover essential aspects of transistor performance, from the device level to the circuit level.

- The application of gate voltage to the channel is essential for utilizing MOSFET as switches, and this necessitates a high current value in the ON-state and a low current value in the OFF-state. A substantial ON-state current facilitates the rapid charging of capacitive loads, typically comprising the gates of one or more following transistors. In contrast, a low OFF current minimizes the leakage current, which predominantly governs static power dissipation. The ON/OFF current ratio is a critical FOM for digital switches, with higher values indicating superior performance. According to the 2023 requirements outlined by the International Roadmap for Devices and Systems (IRDS), 1 nm technology node GAA MOSFETs are expected to possess an ON state current of 775 $\mu A/\mu m$ at an OFF current of 10 nA/μm and

an ON/OFF current ratio within the range of $10^5 - 10^7$ for high-performance logic applications [25]. Achieving such an ON/OFF current ratio is dependent on the semiconductor bandgap and gate control efficiency.

- Another significant FOM used to evaluate switching characteristics is the subthreshold swing (SS). It quantifies the rate at which the current increases below the threshold voltage (i.e. when $V_{\mathrm{GS}} < V_{\mathrm{TH}}$ for n-FETs) as

$$SS = \frac{dV_G}{d(\log_{10}(I_{DS}))} \tag{1.1}$$

  where SS is typically measured in millivolts per decade of current (mV/dec), V_{G} is the gate voltage, and I_{DS} represents the drain to source current. A steeper subthreshold slope indicates a more abrupt transition between the OFF-state and ON-state with respect to gate voltage. Ideally, SS should be as small as possible. Conventional Si MOSFET has a lower limit of 60 mV/dec.

- Drain-induced barrier lowering (DIBL) is another important FOM. In the short-channel MOSFET, the source-drain potential has a strong effect on the band bending over a significant portion of the device. This results in the variation in the sub-threshold current of the device. This effect is referred to as DIBL. In simpler terms, the DIBL occurs when the depletion regions of the drain and the source interact near the channel surface to lower the source potential barrier. Further, it is assessed by computing the change in the threshold voltage (V_{TH}) between the drain voltages $V_{\mathrm{DS}} = 0.05$ V and $V_{\mathrm{DS}} = 0.5$ V and normalizing it by ΔV_{DS}, as given

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{1.2}$$

- The intrinsic device delay ($\tau = C_g V_{dd}/I_{ON}$) serves as another critical metric for evaluating the switching behavior of the device. Here, C_g, V_{dd}, and I_{ON} represent the gate capacitance, supply voltage, and ON-state current, respectively. It highlights the inherent constraints on the switching speed of the device and its ability to operate for distinct frequencies.

- The power delay product (PDP) represents a vital metric for evaluating the switching performance of a device. It quantifies the energy expenditure needed for the transition from the ON- to OFF-state transition. It is quantified as $P_{dyn} = \alpha \mathrm{PDP} f$, where f denotes the operating frequency, and α represents the activity factor.

- One of the crucial static performance metrics for the basic CMOS digital block includes maximum DC gain. In multistage logic circuits, an inverter with a maximum DC gain exceeding 1 is highly desirable due to its ability to enhance circuit robustness against errors and promote regenerative behavior.

- One of the crucial static performance metrics for the basic CMOS digital block includes noise margin. In the context of multilevel logic circuits, an inverter with a high noise margin is essential as it signifies the ability of an inverter to tolerate noise or unwanted voltage variations on its input without changing its intended output state.

1.1.2 Analog/Radio Frequency Applications

- The important performance metric for an RF transistor is the unity current gain frequency or cutoff frequency (f_T), which represents the maximum operating frequency at which a transistor might prove useful. It is also the most common measure of transistor speed. The intrinsic cutoff frequency defined as:

$$f_T = \frac{g_m}{2(C_{gs} + C_{gd})} \tag{1.3}$$

  Where C_{gs}, C_{gd} and g_m are the gate-to-source capacitance, gate-to-drain capacitance, and transconductance, respectively. To achieve high f_T, the transistor transconductance (g_m) should be high, and all other elements of the equivalent circuit should be as small as possible.

- The intrinsic gain (A_{V0}) is also an important performance metric of the RF transistor, which measures the maximum possible low-frequency small-signal voltage gain it can provide. The intrinsic gain is given as:

$$A_{V0} = \frac{g_m}{g_{ds}} \tag{1.4}$$

  The voltage gain of a transistor is generally maximized by lowering output conductance (g_{ds}) and hence operating it in the deep saturation mode.

- Another important parameter for the RF transistor is the maximum oscillation frequency or unit power gain frequency (f_{max}). It represents how fast the channel power transmission is modulated by the gate voltage. The f_{max} is defined as:

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_s + R_g) + 2\pi f_T R_g C_g}} \tag{1.5}$$

  Where R_g and R_s are respectively the resistance of the gate and source terminals,

and C_g is the gate capacitance. The low output conductance (g_{ds}) is also one of the key factors in increasing the f_{max}. Thereby, a high f_{max} can be attained when the transistor is driven into deep saturation.

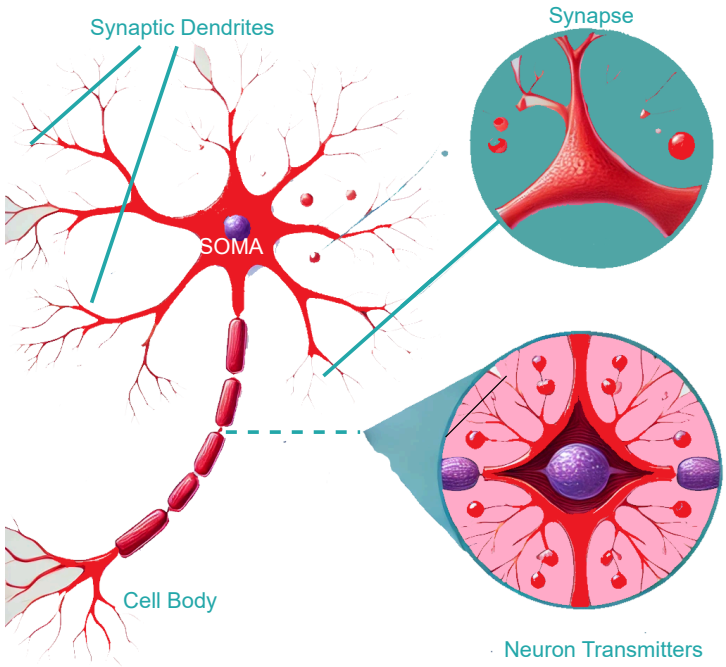

Figure 1.2: Schematic representation of biological neuron and synapse.

1.1.3 Neuromorphic Applications

Neuromorphic computing systems offer a promising alternative to overcome the limitations of von Neumann architecture by leveraging several key advantages, such as extensive parallelism, distributed processing, adaptability, self-organization, fault tolerance, stability, energy efficiency, and robustness. Various non-volatile memory technologies have demonstrated their effectiveness in mimicking the behavior of synapses and neurons [26]. In these systems, neurons serve as basic computational units that perform nonlinear activation or thresholding functions, while synapses act as local memory elements that are densely interconnected through communication channels, as shown in Fig. 1.2. Given the diverse expectations and requirements of neuromorphic systems, it is essential to outline the key characteristics that encompass the critical aspects of artificial synaptic and neuronal implementation [27], [28].

Neuronal Characteristic Requirements

- The neuron must exhibit a threshold-based response, similar to how biological neurons fire when the input signal surpasses a certain threshold. Artificial neurons should be capable of generating non-linear activation functions, where the output remains low for sub-threshold inputs and sharply increases when the input crosses a certain level, mimicking the all-or-nothing firing mechanism in biological neurons.
- Artificial neurons must be capable of receiving multiple input signals, which can be weighted to reflect their importance. This mimics the way biological neurons receive signals from various synapses.
- Artificial neurons must operate with low power consumption. Energy-efficient devices can mimic biological operations at a fraction of the energy cost of traditional computing elements.
- Artificial neurons should be able to process multilevel inputs and outputs, which represent various strengths of synaptic transmission or neural firing, to better capture the gradation seen in biological systems.
- Artificial neurons should exhibit resilience to noise in input signals, ensuring reliable performance even when faced with variations or inaccuracies in data.

Synaptic Characteristic Requirements

- Distinguishable multi-state capability is an important property of artificial synapse because the neuro-inspired algorithms often leverage these analog synaptic weights to facilitate pattern learning and feature extraction. Interestingly, a high number of multilevel states (e.g., exceeding hundreds of levels) can enhance learning capabilities and increase the robustness of the network.
- Dynamic range is another important FOM as it represents the ratio between maximum and minimum conductance. A wider dynamic range enhances the mapping accuracy of algorithmic weights to device conductance, as these weights are often normalized within a specific range, such as between 0 and 1.
- Linearity in weight serves as important criterion as it refers to the consistency of the relationship between device conductance and the number of identical programming pulses applied. Ideally, this relationship should be both linear and symmetric,

allowing for a straightforward mapping of algorithmic weights to the conductance of the device.

- Energy efficiency is one of the crucial criteria for artificial synapses because, in biological synapses, the energy required for each synaptic event is remarkably low, typically ranging from 1 to 10 femtojoules (fJ). This level of energy efficiency is a key benchmark for designing neuromorphic systems.

- Retention and Endurance are significant FOM for evaluating artificial synapses. Non-volatile synaptic devices should serve as long-term memory while retaining data for up to ten years at the maximum chip operating temperature (e.g., 85^{o}C). Moreover, endurance reflects the number of weight updates a device can withstand.

1.2 State-of-Art of GAA MOSFETs

Beyond the 7 nm technology node, Fin-FETs face significant challenges in scaling down the device dimensions due to the onset of short-channel effects [4]. To overcome these limitations and ensure continued performance improvements, GAA devices, such as NW-FET and NS-FET, have emerged as promising alternatives for sub-5 nm technology nodes. In recent years, substantial advancements have been made in the experimental fabrication and simulation studies of GAA devices for digital applications [6**?** , 29]. Especially, stacked NS-FET has demonstrated a higher ON/OFF ratio, reduced drain-induced barrier lowering (DIBL), and lower device delay compared to their Fin-FET and NS-FET counterparts under the same technology node [29, 30]. Despite the promising performance of GAA devices, several critical aspects remain unexplored, particularly for future technology nodes. Key areas that require further investigation include their scalability to sub-3 nm nodes, analog and RF performance, optimization of threshold voltage, and reliability study. Additionally, integrating NS-FETs with advanced circuit designs and their potential for enhancing power efficiency and performance in complex systems have yet to be fully understood. Addressing these gaps is essential for realizing the full potential of NS-FETs in next-generation semiconductor technologies. Key areas that require further investigation include

- Over the past few years, silicon multigate devices, such as Fin-FET, NW-FET, and NS-FET, have been explored for digital applications [29, 30]. However, the RF performance remains unexplored in the proper device design space. Therefore, it is necessary to find a promising FET for RF performance applications for

future technology nodes. Further, it becomes worth understanding their analog/RF performance for guiding experiments and encouraging more efforts in this direction using numerical simulations.

- The stacked NS-FET paved the way for the innovation of novel CMOS architectures, such as FSH and CFET [13, 31, 32]. These novel CMOS architectures present switching performance boosts and area efficiency over the conventional CMOS inverters for the advanced technology nodes [13, 32]. Moreover, these CMOS inverters-based SRAM have experimentally and theoretically proven to demonstrate exceptional read and write noise margin, operating frequency, and lower power consumption [32, 33, 34, 35, 36]. The studies indicate that these novel CMOS inverters could reduce routing congestion due to their exceptional performance benefits with the p-n separation scaling. To our knowledge, no qualitative studies have uniformly benchmarked the inverter-level performance of CFET, FSH, and s-NSH configurations in a single systematic study. Therefore, it becomes increasingly important to understand the performance and scaling advantages of CFET and FSH inverter configurations for developing high-speed and low-power digital ICs with high-density integration capability.

- The exploration of stacked nanosheet-based in six transistors static random access memory (6T SRAM) [14, 34, 37, 38, 39] and logic gates [40, 41] have underscored its potential in memory and logic applications. However, no study has presented the performance advantages of 6T SRAM cells with CFET, FSH, and s-NSH inverter configurations for future technology nodes. In the case of logic aspects, many recent studies on CFET inverters have designed common logic gates [40, 42]. However, the performance analysis of ALU blocks using FSH and s-NSH configurations has not been thoroughly presented. Therefore, there is a pressing need for a detailed investigation of SRAM and ALU performance with s-NSH inverter architectures to implement efficient memory and logic circuits, respectively.

- A three-terminal CTT with a high-k oxide gate, such as HfO_2, Si_3N_4, and Al_2O_3, has emerged as a promising synaptic element due to their full CMOS compatibility with three-dimensional (3-D) integration capability, high dynamic range, and superior retention capability [18]. Interestingly, the enhancement of charge trapping using radiation doses in high-k CTT has made significant progress in achieving high threshold voltage modulation (ΔV_{Th}) [18, 21], which renders

them potential candidates for facilitating multistate operations in analog synaptic devices. Ansari *et al.* have recently reported a charge trap mechanism using Si_3N_4-based stacked NS-FETs [43, 44]. However, their model assumes a negligible impact from the oxide layer trap to validate the current characteristics of both the simulated and experimental device geometry, which results in inaccurate predictions. Additionally, the effect of self-heating caused by the trap mechanism has not been considered. Thus, for accurate device performance and reliable modeling, careful modeling and analysis of GAA-based CTT is essential, particularly to achieve superior non-volatile memory characteristics and enhanced synaptic performance in neuromorphic applications.

- The integration of CTT in neuromorphic systems has seen rapid advancements. Several studies have explored CTT-based synaptic crossbars to evaluate their performance in spiking neural networks (SNNs) for brain emulation with off-chip training [20]. However, these crossbar arrays, utilizing planar SOI MOSFET has reported significant training times and only moderate power efficiency [20]. Additionally, no research has been carried to understand the neuronal behavior in CTT. Thus, this highlights a pressing need to develop fully CTT-based spiking neural networks that implement both synapses and neurons to create more energy-efficient brain-emulating systems.

Addressing these challenges is crucial for realizing the potential of Si-based GAA devices and facilitating their integration into a wide range of electronic devices and systems.

1.3 Problem Definition

NS-FET and NW-FET have demonstrated remarkable advancements and scalability in the implementation of inverter configurations, while an in-depth exploration of GAA-based inverters at device, circuit, and block levels is still missing. Apart from conventional computation, few studies have highlighted the potential of GAA devices in neuromorphic computing, which requires in-depth exploration. Therefore, the current scope of this research is motivated by extensive performance benchmarking and rigorous optimization of device design parameters of GAA devices for digital and neuromorphic computing system applications. Specially, the work in this thesis aims to address the following specific aspects of silicon-based GAA devices for the future integrated design aspects:

- Identifying the most suitable GAA architecture for analog/RF applications in sub-5 nm technology nodes.
- Analyzing and benchmarking silicon stacked nanosheet-based novel CMOS inverter configurations, such as CFET, FSH, and conventional stacked nanosheet (s-NSH) with a Buried Power Delivery Network (BPDN) for future technology nodes.
- Determining the optimal stacked nanosheet-based CMOS inverter configurations, such as CFET, FSH, and s-NSH, for memory and logic applications.
- Investigating the synaptic characteristics of NW-CTT for CMOS-compatible neuromorphic systems.
- Designing and analyzing spiking neural networks using nanowire-based CTT as neurons and synapses to develop energy-efficient neuromorphic systems.

  This comprehensive study will provide insights into GAA architectures and facilitate advancements in analog/RF, memory, logic, and neuromorphic applications.

1.4 Thesis Framework Overview

The thesis is organized into seven chapters. The brief descriptions of each chapter are as follows.

Chapter 1 briefly describes the motivation, problem definition, and outline of the thesis.

Chapter 2 focuses on the analysis and design of silicon-based multigate devices, such as fin field effect transistors (Fin-FET), gate all-around nanowire field effect transistors (NW-FET), and nanosheet field effect transistors (NS-FETs) for sub-5 nm technology node. The chapter primarily centers around the comparative analysis of Fin-FET, NW-FET and NS-FET, highlighting their potential performance benefits for analog/RF applications. Initially, the chapter introduces a 3-D TCAD simulation methodology that accurately describes the electronic transport of multigate devices, which highlights its accurate captivity of short channel and quantum effects. Subsequently, it explores the advantages of Fin-FET, NW-FET, and NS-FET for analog/RF applications, comparing important metrics such as transconductance, output conductance, voltage gain, cut-off frequency, and maximum oscillation frequency with respect to channel length scaling, geometrical parameters scaling (fin width and height, nanosheet thickness and width, nanowire diameter), surface orientation and multichannel stacks.

Chapter 3 discusses the power performance area analysis of silicon CMOS inverters, such as CFET, FSH, and s-NSH with BPDN for 5 nm and beyond technology node. The chapter begins by discussing the process steps involved in designing the CMOS inverters in Synopsys 3-D TCAD tool. It then examines the transfer characteristics and short-channel performance metrics of p-FET and n-FET of CMOS inverters. Subsequently, it will analyze the static performance metrics, such as gain and noise margin, and dynamic performance metrics, including power versus frequency. Finally, the chapter explores the inverter performance dependence on supply voltage V_{DD}, load capacitance with and without the back end of lines, device scaling, and p-n separation.

Chapter 4 delves into an in-depth investigation of memory and logic applications by designing the 6T SRAM and 32-bit arithmetic logic unit, respectively, using CFET, FSH, and s-NSH inverters. The chapter begins by discussing the process flow of 6-T SRAM using CFET, FSH, and s-NSH inverters. Subsequently, it compares the read and write static noise margin, and read and write delay of CFET-, FSH- and s-NSH-based SRAM with respect to the technology node. It then discusses the power performance area benefits of device scaling. Finally, it investigates the device scaling performance of CFET-, FSH-, and s-NSH-based ALU in terms of energy, power delay product, and throughput.

Chapter 5 focuses on a systematic suitability analysis of HfO_2-based nanowire charge trap transistor (NW-CTT) as artificial synapses in the 5 nm technology node. The chapter investigates both short-term and long-term memory characteristics while evaluating recognition accuracy and energy efficiency in a $784 \times 100 \times 10$ neural network configuration. The synaptic characteristics of NW-CTT are examined using a fully calibrated technology computer-aided design (TCAD) tool, based on the self-consistent solutions of Poisson's equation, Boltzmann transport equation, and self-heating equations. The chapter initially investigates the non-volatile characteristics of NW-CTT in the presence of interface oxide charges (N_{it}). Subsequently, we delve into an in-depth analysis of synaptic properties, focusing on long-term memory metrics. To evaluate the NW-CTT performance in the neural network's operation, the $784 \times 100 \times 10$ neural network is designed to analyze the reading accuracy using the MNIST dataset. The conductance values obtained from TCAD simulations serve as synaptic weights in the NeuroSIM neural network simulator [45]. Furthermore, the chapter discusses the short-term and long-term memory characteristics along with reading accuracy and energy consumption as functions of crucial device design parameters, such as nanowire diameter, charge trap layer thickness, gate length, and metal gate work function. Finally, we benchmark the device and neural

network performance metrics of NW-CTT against state-of-the-art synaptic devices.

Chapter 6 delves into the implementation of a fully CMOS-based neuromorphic computing system using NW-CTT. Initially, the chapter introduces a 3-D TCAD simulation methodology that accurately captures the charge-trapping mechanism in NW-CTT. It then proceeds by examining the neuronal performance of NW-CTT. After that, it explores the spike timing dependent plasticity (STDP) behavior in NW-CTT as a synapse. Subsequently, it discusses the design of leaky integrate fire neuron and synaptic crossbar array, which is implemented in the TCAD simulator. Finally, the performance of NW-CTT-based SNN is thoroughly examined under noise and process, temperature and voltage (PVT) variations using a fully calibrated three-dimensional TCAD tool.

Chapter 7 mainly includes the conclusion of the current research and outlines a few directions for future work from a modeling perspective.

1.5 Novel Findings in this Thesis

As the GAA devices are still being developed, the work in this thesis contributes in numerous ways to the field of modeling, physics, and application. The major contributions and the respective conclusions are as follows.

■ The initial work involves the exploration of multigate devices (Fin-FET, NW-FET, NS-FET) with a focus on finding suitable devices for analog/RF applications in sub-5 nm technology nodes.

- Among Fin-FET, NW-FET, and NS-FET, NS-FET exhibits excellent current characteristics for sub-5 nm technology nodes with a larger voltage gain, transconductance, output conductance, cut-off frequency, and maximum oscillation frequency.

- The cut-off frequency and maximum oscillation frequency of 5-nm NS-FET is observed to be around 373 GHz and 389 GHz, respectively, which provides the best opportunity to boost the high-frequency performance limit of silicon technology.

- Our findings indicate that the performance benefits of NS-FET are retained with decreasing the channel length, increasing the effective device width, and stacking the multichannels.

■ To determine the performance of GAA devices for digital ICs, we have developed and benchmarked stacked NS-FET-based CMOS inverters with BPDN, including CFET, FSH, and s-NSH using process simulation for sub-5 nm technology node.

- Our findings reveal that the CFET inverter presents a promising opportunity to achieve high operating frequency and reduced power consumption with area efficiency compared to its counterparts in the nanoscale regime.
- The results show that the device gate capacitance and the fringing field play an essential role in the inverter-level performance degradation that can be minimized by optimizing the p-n separation.
- The CFET inverter consistently outperforms FSH and s-NSH inverters across all evaluated technology nodes and design parameters, underscoring its potential as the preferred choice for future ultra-dense and low-power logic applications.

■ With the ever-increasing demand for power and area-efficient memory and logic applications, we investigate the device-to-circuit level performance of CFET, FSH, and s-NSH inverters by developing 6T SRAM and 32-bit arithmetic logic unit (ALU) using process simulation for sub-5 nm technology node.

- Our findings reveal that CFET-based SRAM with lower power consumption and superior frequency than FSH- and s-NSH-based SRAM at iso-frequency and iso-power, respectively, presents chip-level improvement in advanced technology nodes.
- At basic logic block level for 1 nm technology node, CFET inverter exhibits reduced delay and power delay product over FSH inverter, while FSH inverter offers improved performance than s-NSH inverter.
- Our device-to-circuit performance analysis and benchmarking show that the CFET inverter configuration is well suited for low-power and high-speed digital IC applications in the ultimate scaling limits.

■ To develop a CMOS-compatible non-volatile memory and electronic synaptic device, this research explores the NW-CTT through fully calibrated TCAD simulations.

- The charge trapping and de-trapping of interface states in NW-CTT has demonstrated the memory window of around 1 V between programming and erase pulse when the $N_{\mathrm{it}} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$ present in HfO_2 layer.
- Our analysis highlights the critical role of optimal nanowire diameter, the thickness of the charge trapping HfO_2 layer, gate length, and metal gate work function in enhancing short- and long-term memory characteristics while concurrently preserving recognition accuracy and energy efficiency.

- Our results provide valuable insights into the synaptic behavior of conventional NW-CTTs and offer guidance for further harnessing their weight-update capabilities in neuromorphic computing applications.

■ To develop highly scalable and energy-efficient spiking neural networks (SNNs), neurons and synaptic elements using silicon NW-CTT are designed using a fully calibrated TCAD tool.

- Our findings highlight the capability of NW-CTT to attain multi-threshold states, which is similar to bio-neuron.
- Our findings indicate that NW-CTT as a synapse has the capability of demonstrating spiking timing-dependent plasticity characteristics.
- Our analysis shows that the NW-CTT-based SNN exhibits superior recognition accuracy in the presence of noise and process variations.
- Our results show that the integration of NW-CTT in advanced neuroelectronic systems holds the potential to enable energy-efficient neural signal analysis with high spatiotemporal precision, positioning it as a promising candidate for brain-inspired neuromorphic applications.

Chapter 2

Gate-all-around MOSFETs for Analog/RF Applications

2.1 Introduction

Several experimental and theoretical works have systematically explored and benchmarked the benefits of NS-FET over NW-FET and Fin-FET for logic applications in sub-5-nm technology node [6, 30, 46]. Despite multigate devices, such as Fin-FET, NW-FET, and NS-FET, promise excellent switching performance in the ultimate scaling limit, they can be an outstanding contender for high-gain and high-frequency RF operations. Since Silicon-based multigate devices have excellent noise performance, low power consumption, high integration, low cost, and the ability to be integrated into a system on chip (SoC) [47, 48], it becomes worth understanding their analog/RF performance for guiding experiments and for encouraging more efforts in this direction using numerical simulations.

Early experimental work on 14 nm channel RF Fin-FET demonstrated a record peak cut-off frequency (f_T) and maximum oscillation frequency ($f_{\max}$) of roughly 314 and 180 GHz, respectively, indicating a considerable improvement in RF performance over planar-FET technology [49]. In addition, Fin-FET is emerged as an viable choice for RF system designing with the f_T greater than 6 GHz [50]. It is observed in the recent studies that NS-FET could offer 10% better voltage gain and cut-off frequency over the Fin-FET architecture at 5-nm technology node because of the reduced Miller capacitance [51]. More recently, gigahertz f_T and $f_{\max}$ have been reported with NW-FET and NS-FET in sub-5-nm technology node [8, 52]. Several simulation works have been devoted to understand analog/RF performance of two or multiple channel stacked NS-FET [51, 53, 54], but single channel NS-FET are yet remained unexplored. Moreover, no qualitative studies have been conducted to properly investigate the benefits of NS-FET over NW-FET in the proper device design space. Therefore, NS-FET needs the detailed analog/RF performance investigation that will be useful for assessing their performance potential and for understanding issues that are related to device design parameters scaling.

In this chapter, we systematically explore and compare the analog/RF performance metrics of Fin-FET, NW-FET, and NS-FET for the sub-5-nm technology node. In the

initial performance analysis, we consider single channel geometries of Fin-FET, NW-FET, and NS-FET with (100) surface orientation as this orientation could be a more favorable for enhancing the electron mobility [55]. Further, single channel is found to be more suitable for achieving lower parasitic capacitance [53]. Subsequently, we find the analog/RF performance metrics variation with device design parameters, such as channel length, channel width, height/thickness and diameter, surface orientation, and multichannel stacking. The performance investigation is carried out using a fully calibrated technology computer-aided design (TCAD) platform, which accurately captures the fundamental essential physics of Silicon material with short channel device physics. Our studies not only reveal the performance potential of multigate devices in ultimate scaling limit but also identify optimization directions and windows for determining important analog and RF figure-of-merits (FoM).

2.2 Simulation Technique

2.2.1 Device Design and Simulation Methodology

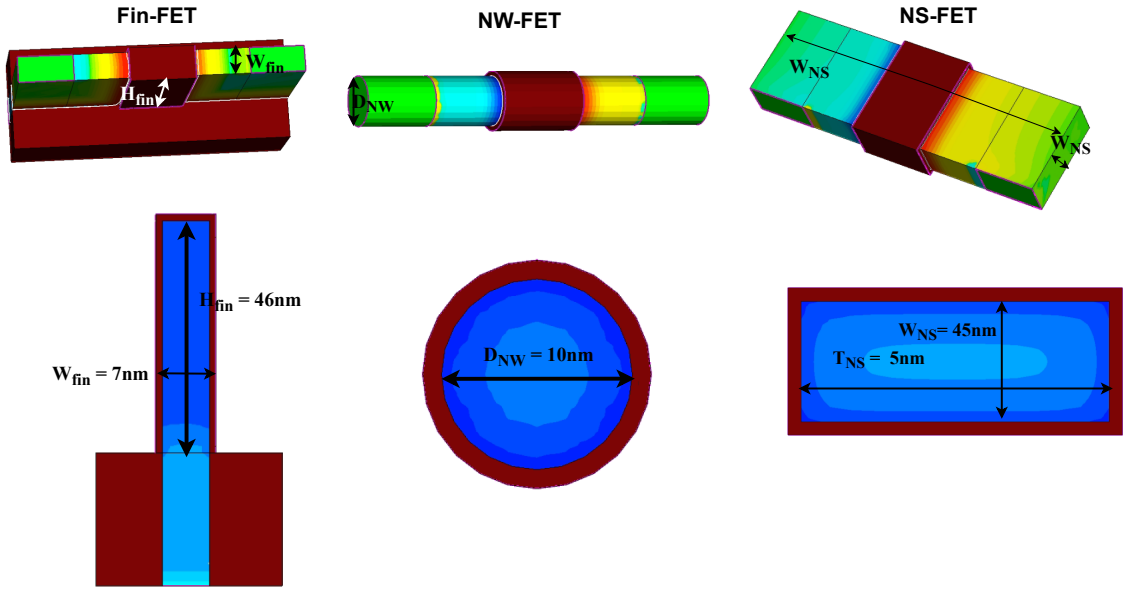

Figure 2.1: Simulation geometries: cross-section view (top) and side view (bottom) of Fin-FET, NW-FET, and NS-FET at 5-nm technology node (18 nm channel length).

Fig. 2.1 shows the device schematics of 18-nm channel length Fin-FET, NW-FET and NS-FET, which are used for initial performance analysis. The device dimensions for 18-nm to 12-nm channel lengths are selected from IRDS 2020 projection that represents 5-nm to 1-nm technology node [56]. Further, the channel length below 12 nm is scaled down from low power International Technology Roadmap for Semiconductors roadmap

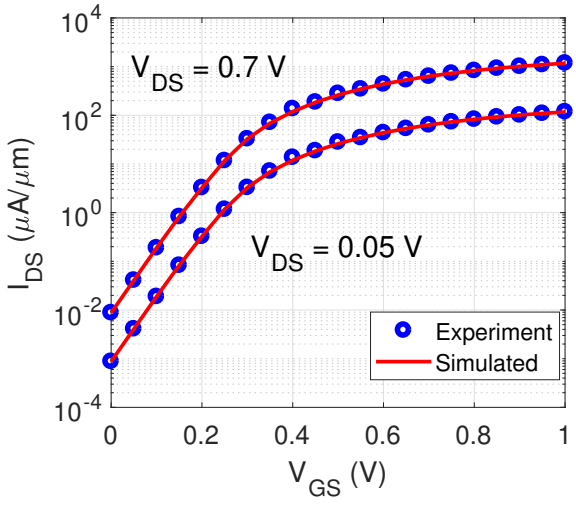

Figure 2.2: Experimental verification of simulation approach: transfer characteristics of 3 channel stacked NS-FET from our 3-D TCAD simulation and experimental results [8] at $V_{DS} = 0.05$ V and $V_{DS} = 0.7$ V for 1-nm technology node (12 nm channel length).

2013 requirements [57] as IRDS specifications are limited to 1-nm technology node. The fin width (W_{fin}) and fin height (H_{fin}) for Fin-FET are taken to be around 7 nm and 46 nm, respectively, which is considered from previous experimental studies [58]. In the case of NW-FET, the diameter (D_{nw}) of NW is assumed to be around 10 nm as the recent experiment demonstrated excellent switching performance at this width [59],[60]. The thickness (T_{ns}) and width (W_{ns}) of NS-FET is considered around 5 nm and 45 nm, respectively, which is close to experimental geometry [8]. Further, the effective width (W_{eff}) of Fin-FET, NW-FET and, NS-FET is found to be around 99 nm ($W_{eff\_fin} = 2H_{fin} + W_{fin}$), 31.4 nm ($W_{eff\_nw} = \pi D_{nw}$) and, 100 nm ($W_{eff\_ns} = 2T_{ns} + 2W_{ns}$), respectively. The stack of 0.6 nm SiO_2 and 1.7 nm HfO_2 is used as the gate oxide in the three devices that correspond to the effective oxide thickness (EOT) of 0.9 nm. Further, the source (S) and drain (D) regions of length $L_{S/D} = 10$ nm are doped to n-type with the doping concentration of $N_{S/D} = 1 \times 10^{20}$ cm^{-3}. By keeping other parameters constant, we have varied the structural parameters, such as channel length, channel width, height/thickness and diameter, and channel number in later simulations.

The performance investigation of multigate devices is done using fully calibrated three-dimensional (3-D) Sentaurus TCAD simulation [61], based on self-consistent solutions of the drift-diffusion equation, continuity equation, and Poisson's equation. The Density-Gradient quantization model is employed to account for the quantum confinement effect and source-to-channel tunneling current [62]. Further, the low field ballistic model is incorporated to account for the quasi-ballistic transport. Furthermore, the Slotboom bandgap narrowing model is considered to account for the bandgap narrowing from high

doping of the source and drain regions [63]. Lombardi mobility, and inversion and accumulation layer mobility models are used to incorporate the mobility degradation at the silicon and SiO_2 interface due to the remote phonon surface and Coulomb scatterings [64]. Further, the Shockley-Read-Hall recombination model is incorporated to activate the generation and recombination conditions of carriers in the continuity equation [46]. For computing the analog/RF performance metrics, the devices are operated in the mixed-mode simulation and small-signal equivalent circuits are constructed from Y-function method [51]. A more realistic value of the cut-off frequency (f_T), and maximum oscillation frequency (f_{max}) are computed by exploiting the short circuit current gain ($H_{21} = |Y_{12}/Y_{11}|$), and maximum available gain (MAG) to 0 dB [65].

2.2.2 Setup and Calibration of TCAD Simulation

Fig. 2.2 shows the I-V characteristics of 3-channel stacked NS-FET from our simulation approach and experimental results [8] for 12-nm channel length. It is observed that simulated $I_{DS} - V_{GS}$ characteristics show an excellent match with the experiment results for all gate and drain voltages. This proves that simulation consideration accurately captures the short channel essential physics of NS-FET. Further, Fin-FET and NW-FET are simulated using the same methodology.

2.3 Performance of Si Multigate FETs

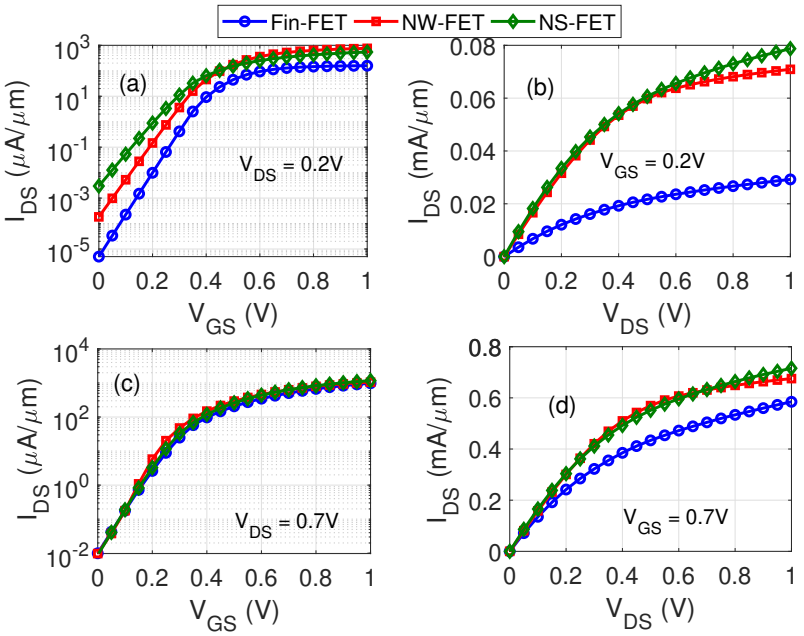

Figure 2.3: Device I-V characteristics of Fin-FET, NW-FET and NS-FET at room temperature: Transfer characteristics ($I_D - V_{GS}$) at (a) $V_{DS} = 0.2$ V and (c) $V_{DS} = 0.7$ V; and output characteristics ($I_D - V_{DS}$) at (b) $V_{GS} = 0.2$ V and (d) $V_{GS} = 0.7$ V.

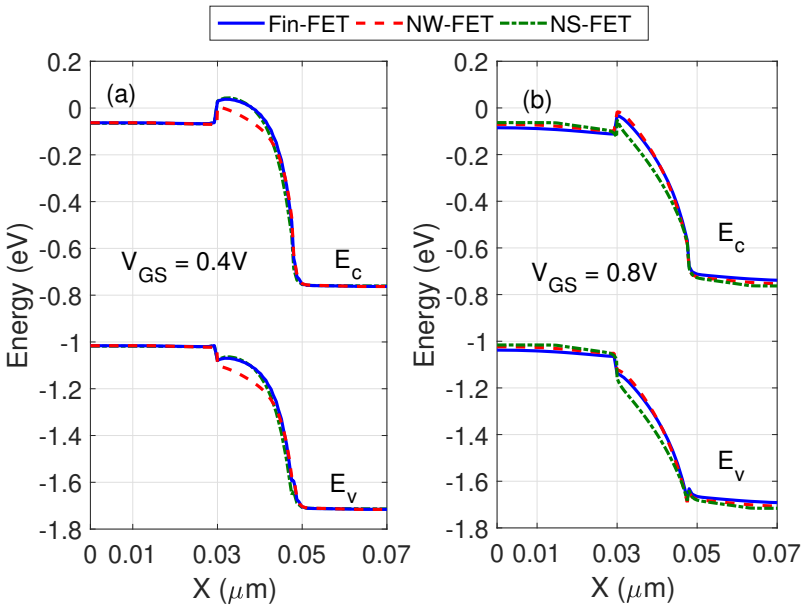

Figure 2.4: Energy band profile along the transport direction for Fin-FET, NW-FET, and NS-FET at distance 1 nm below the top oxide-semiconductor interface at $V_{DS} = 0.7$ V for (a) $V_{GS} = 0.4$ V, and (b) $V_{GS} = 0.8$ V.

Fig. 2.3(a) and (c) show the transfer characteristics of Fin-FET, NW-FET, and NS-FET at $V_{DS} = 0.2$ V and $V_{DS} = 0.7$ V, respectively for 5-nm technology node. For uniform performance benchmarking, the transfer and output characteristics of the three devices are obtained at the fixed OFF current $[I_{DS}(V_{GS} = 0\,\text{V}$ and $V_{DS} = 0.2/0.7\,\text{V})]$ of around 10 nA/μm by adjusting the gate-metal work function difference. NS-FET and NW-FET offer higher drive current over Fin-FET because the surrounding gate from all sides produces a significant inversion charge in the channel region. Importantly, NW-FET exhibits marginally higher drive current over NS-FET for $V_{GS} < 0.6$ V, while NS-FET observes slightly higher drive current for $V_{GS} > 0.6$ V. To get an insight into the difference in the current density, Fig. 2.4(a) and (b) plots the band profile of Fin-FET, NW-FET, and NS-FET at a distance 1 nm below the top oxide-semiconductor interface at $V_{GS} = 0.4$ V and $V_{GS} = 0.8$ V, respectively. It is seen that, at low V_{GS}, NW-FET enhances the gate modulation of the channel conduction band profile, which increases the contribution of the thermionic current component. When V_{GS} increases beyond 0.6 V, a larger effective width allows to appear the full V_{GS} across nanosheet that results in higher gate modulation of channel region band profile. Consequently, it leads to a larger drive current for NS-FET at high V_{GS}. It is observed that three devices have identical difference in $\text{I}_\text{D} - \text{V}_\text{GS}$ characteristics for both $V_{DS} = 0.2$ V and $V_{DS} = 0.7$ V. It is found that the peak electric field in the channel region is around 400 kV/cm at $V_{DS} = 1$ V, which is considerably smaller compared to avalanche breakdown fields [66].

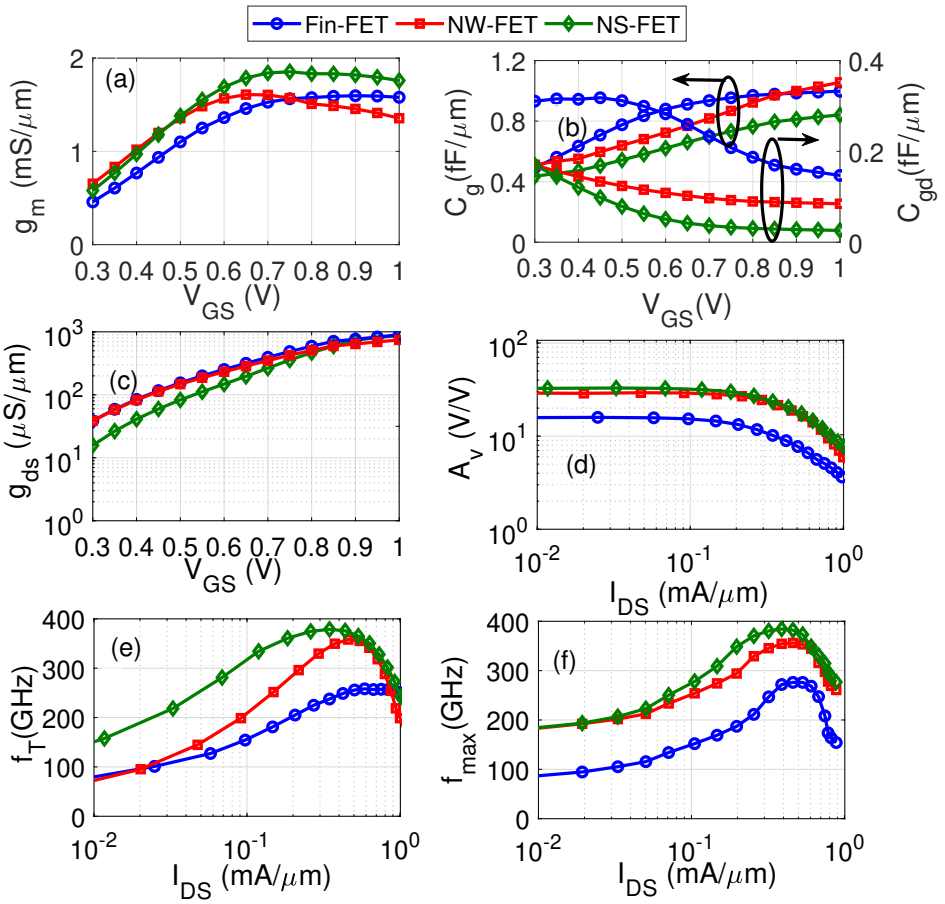

Figure 2.5: Analog/RF performance metrics of Fin-FET, NW-FET and NS-FET at V_{DS} = 0.7 V: (a) transconductance (g_m), (b) gate-capacitance (C_g),and gate-capacitance (C_{gd}) (c) output conductance (g_{ds}) as a function of V_{GS}, (d) voltage gain ($A_V = g_m/g_{ds}$), (e) cut-off frequency (f_T), and (f) maximum oscillation frequency (f_{max}) as a function of I_{DS}.

Fig 2.5 shows the important analog/RF figure of merits (FoM) for Fin-FET, NW-FET and NS-FET at V_{DS} = 0.7 V. It is observed from Fig. 2.5(a) that the three devices exhibit the similar trend in transconductance (g_m)-V_{GS} characteristics. The linear increment in g_m for low V_{GS} is observed, while the peak in the g_m value appears and decreases further with increasing V_{GS}. The reason for the g_m decrements is that the gate modulation of the channel potential is not perfect and degrades with increasing V_{GS}. This g_m decrements at high V_{GS} is also reported in previous works on multigate devices [53][67]. A maximum value of g_m for NS-FET is obtained around 1.8 $mS/\mu m$, which promises high cut-off frequency and voltage gain. Fig 2.5(b) shows the gate capacitance (C_g) which is a combination of (C_{gs} + C_{gd}) where C_{gs} is the gate-to-source capacitance and C_{gd} is the gate-to-drain capacitance, as a function of V_{GS}. It is observed that the C_g increases rapidly with increasing the V_{GS}. This is due to source originating charge increases in the channel region that linearly increases the C_{gs} component. It is found that C_{gd} decreases at low V_{GS} and appears nearly constant for high V_{GS} values. This is due to inversion charge in

the channel region for a given V_{DS} becomes less susceptible to the change of V_{GS}.

It is also observed from Fig. 2.5(a) and Fig 2.5(b) that g_m of Fin-FET is higher than NW-FET at high V_{GS}, but C_g of NW-FET is higher at high V_{GS}. The Fin-FET has better gate modulation of the channel conduction band profile over NW-FET due to higher drain-induced barrier lowering (DIBL) (shown in Fig. 2.6), which increases the g_m values. However, a higher drain charge contribution for Fin-FET significantly rises the C_{gd} component in the C_g, as shown in Fig. 2.5(b). Consequently, it results in C_g over NS-FET for $V_{GS} > 0.7$ V. Fig 2.5(c) shows that Fin-FET has higher values of output conductance (g_{ds}) due to higher DIBL, while NS-FET observes the least value of g_{ds}. Therefore, the multigate device, which effectively suppresses the short channel effects, could benefit the performance in multiple ways by enhancing the drive current, decreasing C_g, and decreasing the g_{ds}.

Fig. 2.5(d) shows the voltage gain ($A_V = g_m/g_{ds}$) as a function of I_{DS}. It is observed that NS-FET and NW-FET has nearly same A_V, while this A_V is around 2× higher as compared to Fin-FET. The NS-FET, offers the A_V of around 32 V/V, which is around 2.6 × higher than that of planar double gate MOSFET technology at 0.4 mA/μm I_{DS} for the same device geometry. Therefore, the multigate device architectures seems to be a strong candidate for high-gain amplifier due to improvement in g_m and g_{ds} values.

Fig. 2.5(e) shows the unity current gain/cut-off frequency (f_T) as a function of I_{DS} for Fin-FET, NW-FET and NS-FET at $V_{DS} = 0.7$ V. The peak f_T of NS-FET is found to be around 373 GHz at I_{DS}= 0.4 mA/μm, which is around 1.5× higher than that for Fin-FET. Further, this f_T value for NS-FET is nearly 1.6 × higher than that for planar double gate MOSFET (229 GHz) at 0.4 mA/μm I_{DS} for the same device geometry that makes them a promising candidate for enhancing RF performance limit at short channel length. Further, a high value of f_T reveals that external fringing parasitic capacitance does not limit the performance of multigate devices. Fig. 2.5(f) shows unity power gain/maximum oscillation frequency (f_{max}) as a function of I_{DS} for Fin-FET, NW-FET and NS-FET at $V_{DS} = 0.7$ V. The model equation for f_{max} can be given as $f_{\max} = f_T/2\sqrt{g_{ds}(R_s + R_g) + 2\pi f_T R_g C_g}$ [65]. It is observed from Fig. 2.5(f) that NS-FET has considerably higher value of $f_{\max}$ as compared to NW-FET and Fin-FET. This is due to the dependence of $f_{\max}$ on g_{ds} and gate resistance (R_g). NS-FET exhibits smaller values of g_{ds} and R_g, which allows the peak f_{max} of around 389 GHz. Therefore, NS-FET outperforms Fin-FET and NW-FET in analog/RF FoM, and appears to be a strong candidate for high-frequency applications at 5-nm technology node.

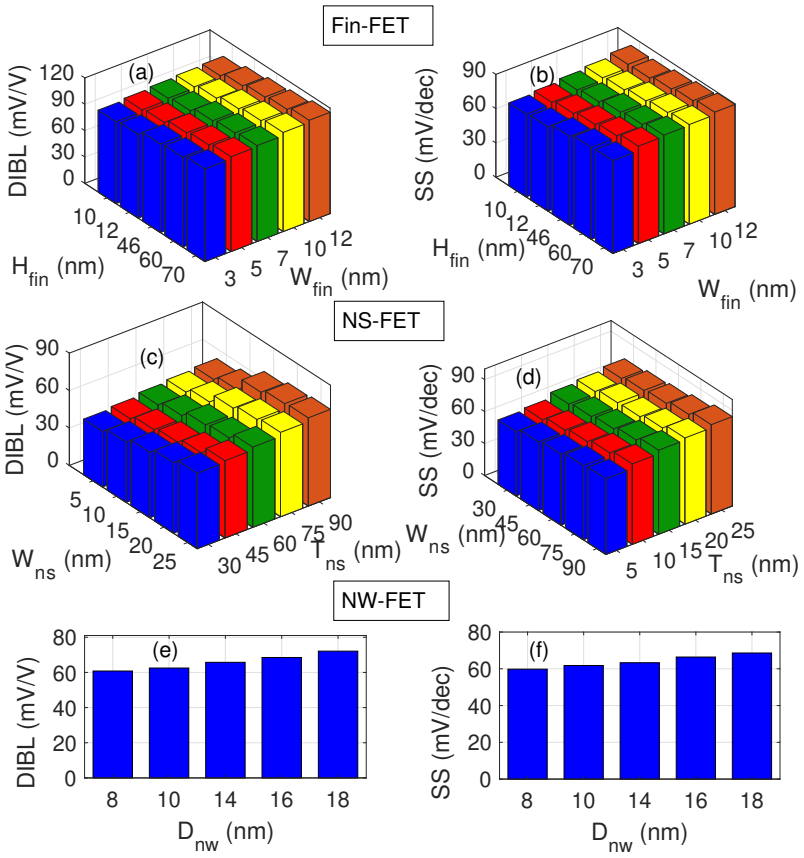

Figure 2.6: Impact of geometrical parameters on the short channel performance metrics of Fin-FET, NW-FET and NS-FET at $V_{GS} = 0.7$ V and $V_{DS} = 0.7$ V for the fixed OFF current of around 10 nA/μm: (a) DIBL and (b) sub-threshold slope (SS) as a function of fin width and fin height, (c) DIBL and (d) SS as a function of nanosheet width and thickness, (e) DIBL and (f) SS as a function of nanowire diameter.

2.3.1 Impact of Geometrical Parameters

Since the gate efficiency can be improved by tailoring the geometrical parameters of multigate channels, this section explores short channel and analog/RF performance metrics dependency on the geometrical parameters of Fin-FET, NW-FET and NS-FET. Fig. 2.6 explores the DIBL and sub-threshold slope (SS) as a function of Fin-FET, NW-FET and NS-FET geometrical parameters. The gate length of devices are kept fixed to 18 nm, when the geometrical parameters are varied. It is observed that the DIBL of Fin-FET increases with increasing the fin height and width because the gate control over channel region reduces, while SS shows marginally increment. In the case of NS-FET, DIBL increases significantly with increasing channel width and thickness due to significant loss in the gate controllability. Further, the increment of SS is observed marginally when the NS-FET width and thickness are scaled up. The SS and DIBL of NW-FET increases rapidly with the increase in nanowire diameter. This is because wider channel weakens the gate electrostatic control on the channel regions and increases the influence from the

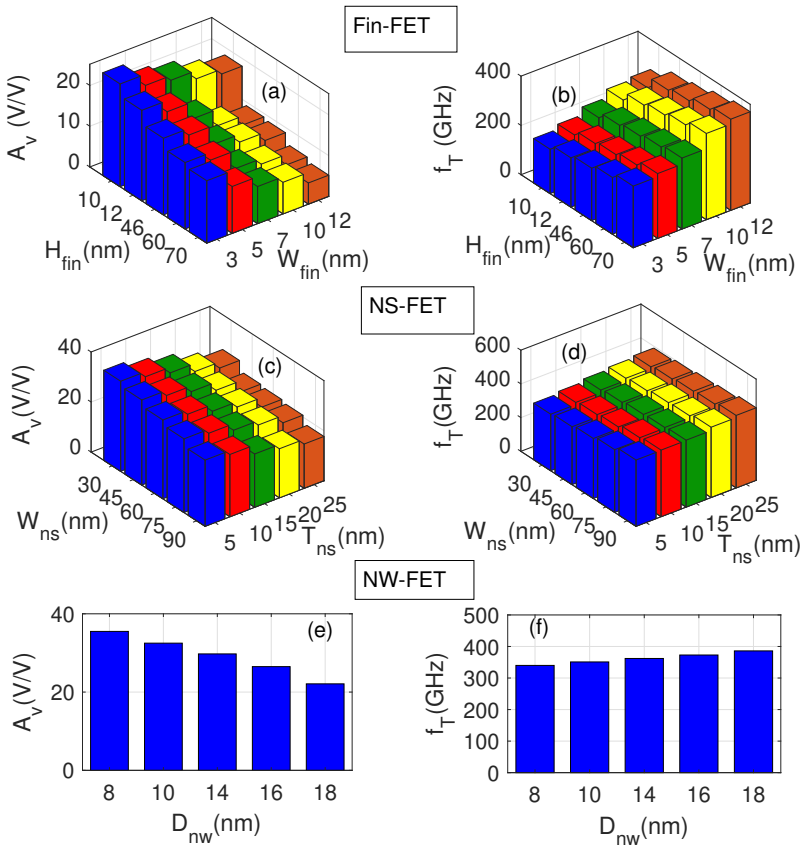

Figure 2.7: Impact of geometrical parameters on the analog/RF performance of Fin-FET, NW-FET and NS-FET at V_{GS} = 0.7 V and V_{DS} = 0.7 V for the fixed OFF current of around 10 nA/μm: (a) A_V and (b) f_T as a function of fin width and fin height, (c) A_V and (d) f_T as a function of nanosheet width and thickness, (e) A_V and (f) f_T as a function of nanowire diameter.

drain voltage.

The minimum value of SS is found to around 72.5 mV/dec, 60.8 mV/dec, and 61 mV/dec for 3 nm (W_{fin}) & 10 nm (H_{fin}), 8 nm (D_{nw}), and 30 nm (W_{ns}) & 90 nm (T_{ns}), respectively, which are lower than that of planar MOSFET [68]. The SS of NW-FET is very close to the thermodynamic limit for MOSFET because the cylindrical nature of the channel effectively suppresses the short channel effects. On the other hand, the switching performance of NS-FET is affected by larger sheet width and rectangular channel cross-section, which requires considerably higher V_{GS} to achieve the channel inversion. Further, the minimum DIBL is observed around 93.2 mV/V, 60.8 mV/V, and 45 mV/V for 3 nm (W_{fin}) & 10 nm (H_{fin}), 8 nm (D_{nw}), and 30 nm (W_{ns}) & 90 nm (T_{ns}) respectively. A smaller value of DIBL suggests that NS-FET can be more immune to change in drain field effects over Fin-FET and NW-FET.

Fig 2.7 shows the A_V and f_T as a function of Fin-FET, NW-FET and NS-FET geometrical parameters. It is observed that A_V and f_T for multigate devices have a

fundamentally different dependency: f_T increases and A_V reduces with increasing the channel width and height/thickness of NS-FET and Fin-FET. It is important to note that A_V of NS-FET marginally reduces with the width, but a significant reduction is observed with increasing the sheet thickness. The reason is that a larger nanosheet width and thickness offer higher g_m, but g_{ds} increases considerably as the thickness of the sheet increases. It is observed that a larger fin width and height reduce the gate efficiency in Fin-FET that increases the g_{ds} values. Moreover, g_m is found to be increased for both increasing the fin width and height. In the case of f_T, a larger height considerably reduces the C_g values and thus increases f_T rapidly. However, increasing the fin width shows a marginal variation in C_g, resulting in marginally higher f_T. For NS-FET, a marginal increment in f_T is observed with width and thickness variation due to simultaneous variation in g_m and C_g. Further, a similar trend in A_V and f_T of NW-FET is observed due to increment g_m and g_{ds}, and decrements in C_g with increasing the nanowire diameter. Thus, the best A_V can be achieved using thinner and narrower sheet/fin that enhances the gate controllability, but the high f_T demands wider and thicker fin/sheet by increasing current drivability.

It could be inferred from Fig. 2.7 that, at nearly the same effective width, NS-FET offers higher A_V and f_T over the NW-FET and Fin-FET. In comparison to Fin-FET, NW-FET offers better A_V and f_T at the same effective width. Further, A_V and f_T of NW-FET has around 2× and 1.3×, respectively, over the Fin-FET under the same effective width. It is observed that the A_V of Fin-FET is reduced by 5× when the effective width is scaled from 23 nm to 152 nm, but NS-FET exhibits a marginal decrement in A_V with the factor of around 2× when the effective width is scaled from 70 to 230 nm. Further, in the case of f_T, NS-FET and Fin-FET exhibit around 1.28× and 2.05× increment, respectively, with the above effective width scaling. Further, NW-FET is having around 1.6× decrement and 1.1× increment for A_V and f_T, respectively, with scaling the effective width from 25.12 nm to 56.52 nm. Thus, NS-FET has displayed more robust analog/RF performance with geometrical parameter variations.

It is observed from Fig. 2.6 and Fig. 2.7 that, at the same DIBL, NW-FET exhibits higher A_V over NS-FET due to lower g_m, while NS-FET exhibits higher f_T because the C_g is lower compared to NW-FET. For the Fin-FET case, it becomes difficult to match DIBL with NS-FET due to considerably higher DIBL values at the selected geometrical parameters. Therefore, it can be observed from Fig. 2.6 and Fig. 2.7 that NS-FET provides more freedom to optimize the geometrical parameters for better short channel

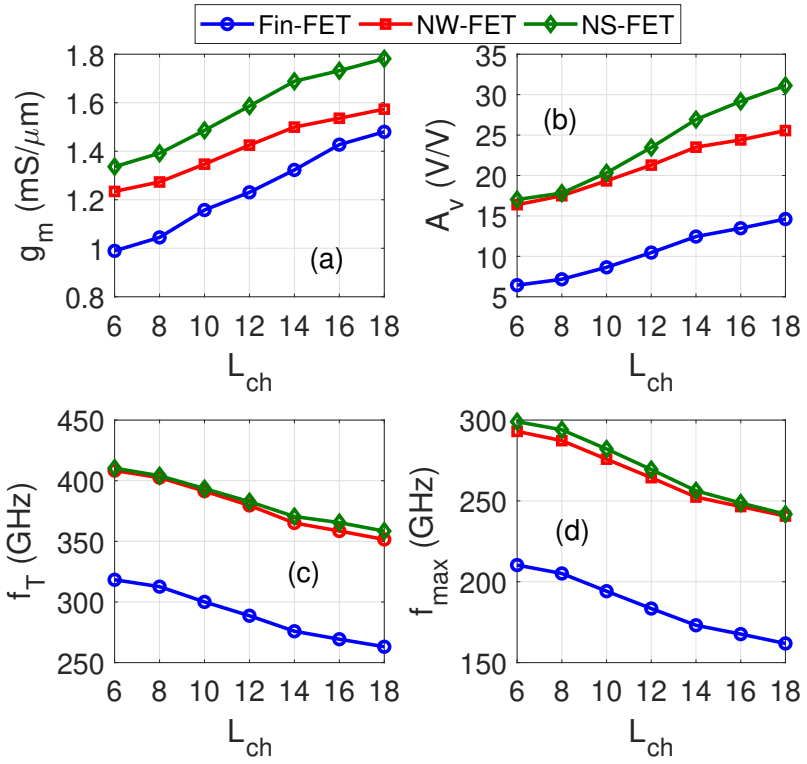

Figure 2.8: Impact of channel length scaling on analog/RF performance of Fin-FET, NW-FET and NS-FET at $V_{DS} = 0.7$ V and $V_{GS} = 0.7$ V : (a) transconductance (g_m), (b) voltage gain (A_V), (c) cut-off frequency (f_T) , and (d) oscillation frequency (f_{max}) as a function of channel length (L_{ch}).

and analog/RF performance over Fin-FET and NW-FET.

2.3.2 Impact of Channel length

Fig. 2.8 shows analog/RF performance metrics of Fin-FET, NW-FET, and NS-FET as a function of channel length at the fixed OFF current of around 10 nA/μm. The device geometrical parameters, such as fin width and height, sheet width and thickness, and nanowire diameter, are kept the same when the channel length is scaled down. It is observed from Fig. 2.8(a) that g_m for the three devices decrease considerably with decreasing the channel length. This is because the sub-14-nm devices are affected substantially by the source-to-channel tunneling current at the OFF-state. The increment in the source-to-channel tunneling current enhances the drive current for a fixed V_{DS}, and the device requires a much smaller V_{GS} to achieve the OFF-state. Thus, decreasing the channel length decreases the drive current and hence, g_m. Importantly, NS-FET exhibits higher performance degradation with reducing the channel length, but it still maintains a considerably higher value of g_m when the channel length is scaled down to 6 nm. Further, a significant reduction in the g_m value is because the small mean free path of electrons increases the mobility degradation in the presence of a greater number of scattering events

at short channel length.

It is observed from Fig. 2.8(b) that A_V for multigate devices decreases considerably with decreasing the channel length. Due to significant degradation in g_m and g_{ds}, the voltage gain of NS-FET drops from 32 V/V to 17 V/V when the channel length is scaled down from 18 nm to 6 nm. It is found that NW-FET has nearly the same gain as compared to NS-FET for $L_{ch} < 10$. Further, the NS-FET and NW-FET display a voltage gain of around 17 V/V at 6-nm channel length, which is more desirable for amplification applications. Therefore, it is evident that multigate devices can offer sufficient voltage gain even at the 6-nm channel length, and the NS-FET has an advantage over Fin-FET and NW-FET in the ultimate scaling limit.

Fig. 2.8(c) shows that, despite g_m reduction, the f_T of NS-FET and Fin-FET considerably increases with decreasing the channel length. This is due to the presence of discrete quantum states that reduces C_g because the gate capacitance reduces at shorter channel lengths [69]. Further, the f_T of NW-FET becomes nearly equal to NS-FET beyond 14-nm channel length. This is because a smaller effective width NW-FET results in much smaller gate capacitance over NS-FET. The f_T of NS-FET and NW-FET is found to be enhanced by 1.14× when channel length scale down to 6 nm, while Fin-FET exhibits around 1.2× improvement. Further, NS-FET and NW-FET offer nearly around 1.2× higher f_T over Fin-FET for 18-nm to 6-nm channel length. Fig. 2.8(d) shows that f_{max} significantly increases with the decreasing channel length. This is because f_T increases, while R_g and g_{ds} decreases with decreasing the channel length. In summary, A_V, f_T, and f_{max} values suggest that NS-FET could be a more prominent option for high-gain and high-frequency RF circuits, but NW-FET can also be preferred at very short channel lengths.

2.3.3 Impact of Surface Orientation

Fig. 2.9 shows the performance of Fin-FET, NW-FET, and NS-FET as a function of surface orientations, such as (100), (110), and (111), which could be achieved by rotating the device layout in the wafer plane [70]. It is observed from Fig. 2.9(a) that maximum effective electron mobility (μ_{eff}) for n-type multigate devices is found along (100) surface due to lower effective electron mass and surface density of atoms. The μ_{eff} in three devices is modulated significantly with surface orientation because of the variation in electron masses at the different orientations. It is observed that the μ_{eff} of NS-FET and NW-FET are found to be nearly the same, but their mobility is around 1.29× higher compared to Fin-FET in all orientations. The Fin-FET is significantly affected by higher drain field

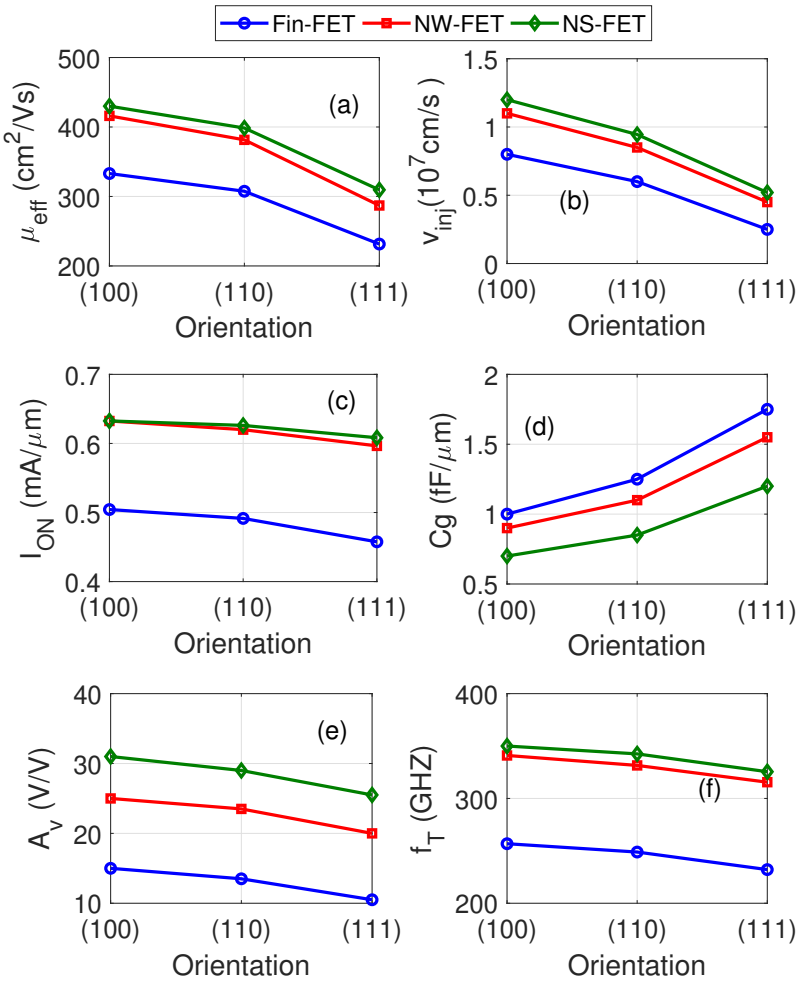

Figure 2.9: Impact of surface orientation on analog/RF performance of Fin-FET, NW-FET and NS-FET at V_{DS} = 0.7 V and V_{GS} = 0.7 V : (a) effective electron mobility (μ_{eff}), (b) injection velocity (v_{inj}), (c) ON current (I_{ON}) , (d) gate capacitance (C_g), (e) voltage gain (A_V), and (e) cut-off frequency (f_T) as a function of surface orientation.

in the channel region. Fig. 2.9(b) shows that NS-FET with (100) surface orientation with the highest mobility also displays higher injection velocity (v_{inj}) and vice versa. The mobility and v_{inj} for three devices are in good agreement with experiment and previous simulation results [29],[54]. It is observed that NS-FET with (100) orientation has around 15% and 25% higher v_{inj} over NW-FET and Fin-FET with the same surface orientation, respectively. However, mobility and v_{inj} are highly dependent on the orientation, bias, and geometrical parameters. Thus, selecting the optimum channel orientation and geometrical parameters could enhance the silicon-based device performance.

Fig. 2.9(c) shows that despite the significant change in mobility and injection velocity, ON current for three devices shows marginal variation with surface orientation due to more immune to short channel effects [71]. The NS-FET and NW-FET have nearly the same ON current due to their nearly same μ_{eff}, but the NS-FET with (100)

orientation exhibits advantage in C_g, A_V and f_T as compared with other orientations. It is observed in Fig. 2.9(d) that a larger C_g is observed in (111) orientation over (110) and (100) orientations due to strong anisotropic feature. Fig. 2.9(e) shows that A_V for NS-FET (100) orientation is around 1.24 × and 2.13 × higher than that for NW-FET and Fin-FET with same surface orientation. The A_V of NS-FET show around 1.14× and 1.29× degradation in (110) and (111) orientations due to significant reduction in g_{ds} values. It is observed from Fig. 2.9(f) that f_T does not show the strong dependency on orientation due to g_m reduction and C_g increment in (110) and (111) orientations. Therefore, NS-FET with (100) channel orientation is more suited for analog/RF applications, μ_{eff}, A_V and f_T over (110) and (111) surface orientations.

2.3.4 Impact of Multichannel Stacks

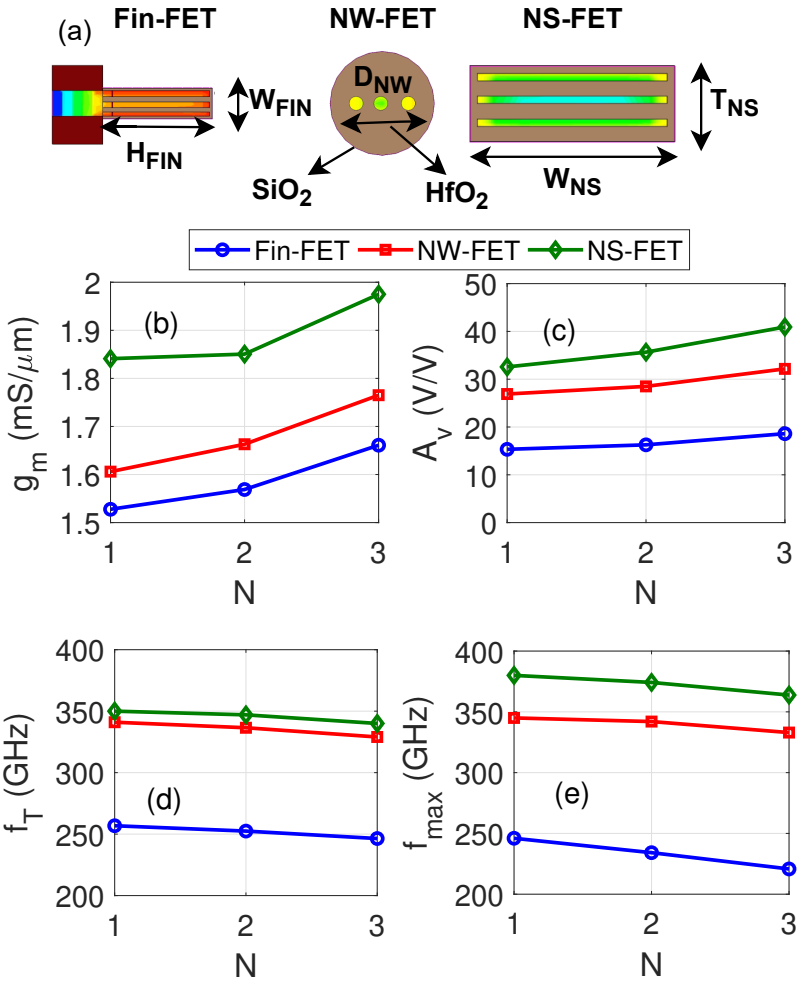

Figure 2.10: Analysis of multichannel structure on the analog/RF performance of Fin-FET, NW-FET and NS-FET at V_{DS} = 0.7 V and V_{GS} = 0.7 V: (a) side schematic of the three-channel device structures of Fin-FET, NW-FET and NS-FET, (b) transconductance (g_m), (c) voltage gain (A_V), (d) cut-off frequency (f_T), and (e) maximum oscillation frequency (f_{max}) as a function of number of channels (N).

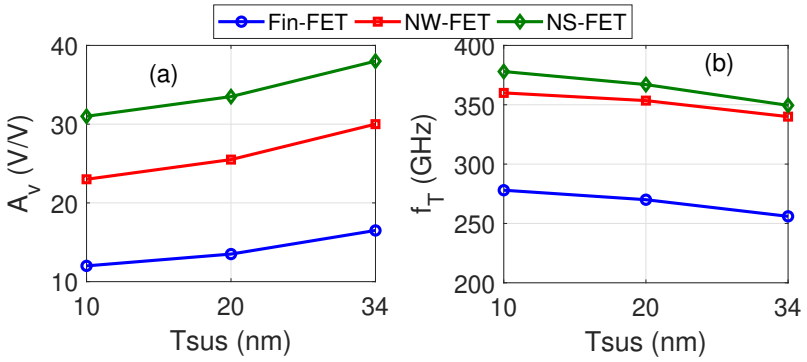

Figure 2.11: (a) Voltage gain (A_V), and (b) cut-off frequency (f_T) for three channels Fin-FET, NW-FET, and NS-FET as a function of suspension thickness (T_{sus}) at $V_{DS} = 0.7$ V and $V_{GS} = 0.7$ V.

Fig. 2.10 shows the analog/RF performance of Fin-FET, NW-FET, and NS-FET as a function of single, double, and triple channel stacks. The considered single, double, and triple stack architectures are shown in Fig. 2.10(a). Here, we increase the number of channels stacked and fins by keeping the same area footprint for uniform benchmarking. The Fin pitch and suspension thickness (T_{sus}) are considered to be fixed around 34 nm and 10 nm, respectively. Fig. 2.10(b) shows that g_m of multigate devices increases with increasing the number of the channels due to the increment in the electron-conducting paths. The g_m of NS-FET shows significant improvement with increasing the number of channel stacks because of increment in the same width channels. In contrast, g_m for NW-FET shows marginal increment as the effective channel area is reduced with increasing the number of channels.

Fig. 2.10(c) shows that A_V for multigate devices increases with increasing the number of channels. It is found that the g_m of NS-FET and Fin-FET is enhanced by 1.1× and 1.08×, respectively, but A_V of NS-FET and Fin-FET exhibits 1.25× and 1.21× improvement with single to three channels increment. The reason for a considerable gain increment is that narrower sheet and fin width results in lesser drain field penetration in the channel region, which decreases the g_{ds} values. It is found from Fig. 2.10(b) and (d) that, despite increment in g_m, the cut-off frequency (f_T) of multigate devices reduces with increasing the channel stacks. This is because the multichannel stacking considerably raises the contribution of coupling and parasitic capacitance in the C_g values. Fig. 2.10(e) shows that f_{max} for these multigate devices deteriorate with increasing the number of channels because of increment in R_g and g_{ds}. Thus, multichannel stacks can enhance the g_m and A_V, but increasing the channel stacked is not the right choice for RF performance improvement.

Fig. 2.11 shows the A_V and f_T for three channels Fin-FET, NW-FET, and NS-FET with various suspension thickness (T_{sus}). It is observed that A_V increases with increasing the T_{sus} because the channel gets narrower, which restricts the carrier scattering and leads to an increase in g_m. The g_{ds} also decreases due to reduced drain field effect in the narrower channel region. Fig. 2.11(b) shows that the f_T marginally decreases with increasing T_{sus} due to increment in C_g values, despite increment in g_m. Therefore, it is found that the A_V can be improved by optimizing the T_{sus}, but f_T exhibits marginally decrement with increasing T_{sus}.

2.4 Summary

This chapter presented a comprehensive analog/RF performance comparison between Fin-FET, NW-FET, and NS-FET for sub-5-nm technology nodes. It is found that NS-FET has promised higher voltage gain, cut-off frequency, and maximum oscillation frequency over NW-FET and Fin-FET that makes them a promising option for high-frequency RF applications. Specially, the cut-off frequency and maximum oscillation frequency of 5-nm NS-FET have found to be around 373 GHz and 389 GHz, respectively, which provides the best opportunity to boost the high-frequency performance limit of silicon technology. The results show that voltage gain could maximize by increasing the channel length, selecting proper surface orientation, and reducing the channel's width and height/thickness. In contrast, RF performance metrics of multigate devices have significantly enhanced by decreasing the channel length and increasing the geometrical parameters. Further, multichannel stacking will not be the best choice for RF applications. Our performance analysis and benchmarking provide analog/RF ultimate performance limit of sub-5-nm multigate devices and stimulate experiment work is expected to exceed the high-frequency performance of Silicon-based MOSFET technology.

Chapter 3

CMOS Inverters based on Si Stacked Nanosheet FET

3.1 Introduction

The stacking of Si nanosheets in both horizontal and vertical configuration in stacked NS-FET has demonstrated outstanding switching performance by combining the benefits of area [8, 9]. However, the scaling advantages of a standard stacked nanosheet (s-NSH)-based inverter are significantly impacted by the separation between p-FET and n-FET (p-n separation). Optimizing p-n separation poses challenges, particularly as it is determined by mask edge placement and lateral etch control during metal gate deposition [17]. Moreover, a smaller p-n separation notably constrains operating speed and power efficiency due to enhanced Miller capacitance [16, 17].

FSH and CFET inverters have been proposed to be scaling booster architectures with nanosheets that could reduce the device footprint and ensure high-performance gain [13, 14]. Interestingly, inserting dielectric between p-FET and n-FET, and controlling the channel using the forked gate in the FSH inverter has demonstrated 12% cell area reduction with 13% lower power dissipation over s-NSH inverter for 3 nm technology node (N3) [31]. More interestingly, the CFET inverter, which vertically stacks the n-FET and p-FET with a common gate, has demonstrated a 55% lesser cell area with 2.3× higher speed over s-NSH inverter for the N3 [16]. Furthermore, a few recent studies have concentrated on analyzing the power-frequency performance benefits of CFET by comparing it with the s-NSH inverter configuration for the N3 [16, 72, 73]. To the best of our knowledge, no qualitative studies have uniformly benchmarked the inverter-level performance of CFET, FSH, and s-NSH configurations in a single systematic study. In addition, there is a lack of detailed static and dynamic performance of these inverter configurations for future technology nodes. Therefore, it becomes increasingly important to understand the performance and scaling advantages of CFET and FSH inverter configurations for developing high-speed and low-power digital ICs with high-density integration capability.

In this chapter, we examine and benchmark the performance of CFET, FSH, and s-NSH inverter configurations at the ultimate scaling limit using S-process simulation in a fully calibrated three-dimensional (3D) Sentaurus technology computer-aided design

(TCAD) tool. Specially, the process-dependent performance analysis of CFET, FSH, and s-NSH inverters are carried out to accuraly capture the parasitic and buried power delivery network (BPDN) effects. The novel s-NSH-based inverters are uniformly compared to identify a promising configuration, which can offer greater design versatility with excellent switching and scaling performance. The major contributions of this work are stated as follows:

- Current studies on CFET and FSH inverters rely on Sentaurus Device Structure Editor (SDE) or BSIM models, which focus on isolated structures with limited 3D simulations and inconsistent benchmarking across nodes [16], [74], [41], [75]. Our work bridges this gap by systematically benchmarking CFET, FSH, and s-NSH inverters using a unified 3D S-Process simulation framework. By incorporating buried power delivery networks (BPDN), we optimize power efficiency, minimize parasitics, and highlight performance under advanced routing technologies.

- Process fluctuations present a significant challenge for the reliable design of s-NSH-based devices at 3 nm and smaller technology nodes [76]. Despite existing studies primarily examining process variation effects on CFET at the 3 nm node using the SDE framework [77], our work advances this by systematically comparing CFET, FSH, and s-NSH inverters at the 1 nm node through 3-D process simulations.

- Existing studies provide fragmented insights into the power performance area (PPA) metrics of CFET [16], FSH [41], and s-NSH inverters [78], with limited focus on a unified comparative analysis across technology nodes. Our work addresses these gaps by delivering a comprehensive PPA analysis for CFET, FSH, and s-NSH inverters with and without BPDNs, extending across nodes from N5 to N0.5. This effort highlights scaling behavior, BPDN impact, and optimization strategies, which offer critical guidance for future high-density circuit design.

- Despite previous studies have analyzed p-n separation in individual devices, such as FSH and CFET inverters [16, 14], our work provides uniform benchmarking across CFET, FSH, and s-NSH by systematically evaluating power and delay performance as a function of p-n separation (45 nm to 17 nm) at the 1 nm node. This comprehensive analysis offers novel insights for optimizing inverter design and ensures consistent evaluation across different device architectures.

3.2 Simulation Technique

3.2.1 CMOS Inverter Design

Fig. 3.1(a), 3.1(b), and 3.1(c) show the cross-sectional channel along with side views of s-NSH, FSH, and CFET inverters, respectively. For the initial performance analysis, the gate lengths of p-FET and n-FET are selected around 12 nm, which is taken from the projection of IRDS 2021 for the 1 nm technology node [79]. The source (S) and drain (D) regions of p-FET and n-FET are taken to be 18 nm long with a doping concentration of nearly $2 \times 10^{20}\,\mathrm{cm}^{-3}$. Further, the silicon nanosheet channels are considered identical with the width (W_{NS}) of around 45 nm and thickness (T_{NS}) of around 5 nm. The considered W_{NS} and T_{NS} of nanosheets are in good agreement with the reported experimental geometry of s-NSH inverters [8, 80, 81]. The vertical sheet-to-sheet spacing is chosen to be around 10 nm due to sacrificial layer limitation [8, 82]. The p-n separation for the CFET, FSH, and s-NSH inverters is initially considered to be around 25 nm, 17 nm, and 25 nm, respectively. However, in later simulation, we have varied the p-n separation by keeping other parameters fixed. Also, three nanosheet stacked channels are considered in our simulation as it is widely adopted in recent experiments to enhance the effective channel width [8, 53]. The gate oxide consists of 0.6 nm SiO_2 and 1.25 nm HfO_2 stack, which corresponds to the effective oxide thickness (EOT) of 0.9 nm. The effective width (W_{eff}) and contacted gate pitch (CGP) of both p-FET and n-FET are the same and taken to be around 330 nm and 42 nm, respectively.

3.2.2 Process Simulation Methodology

Fig. 3.1(a), 3.1(b), and 3.1(c) presents the fabrication process steps for realizing the s-NSH, FSH, and CFET inverters, respectively, which are performed in the S-process of Synopsys TCAD tool. Here, we present the detailed process steps for fabricating the s-NSH inverters and summarize the key fabrication steps for FSH and CFET inverters. The s-NSH inverter is realized using the following process steps: (i) the BPDN using Ruthenium metal is deposited in the substrate; (ii) thermal oxidation is performed to isolate BPDN; (iii) epitaxial growth of alternate silicon germanium ($Si_{0.7}Ge_{0.3}$)/silicon (Si) layers is carried out; (iv) thermal oxidation is performed to achieve shallow trench isolation (v) the sidewall image transfer (SIT) technique is used to achieve the desired width and thickness; (vi) polysilicon dummy gates are deposited on top of the sheets; (vii) silicon nitride is placed to form the inner and outer spacer in both n-FET and p-FET; (viii) the n-FET is masked, then the source and drain of p-FET are doped with ion energy

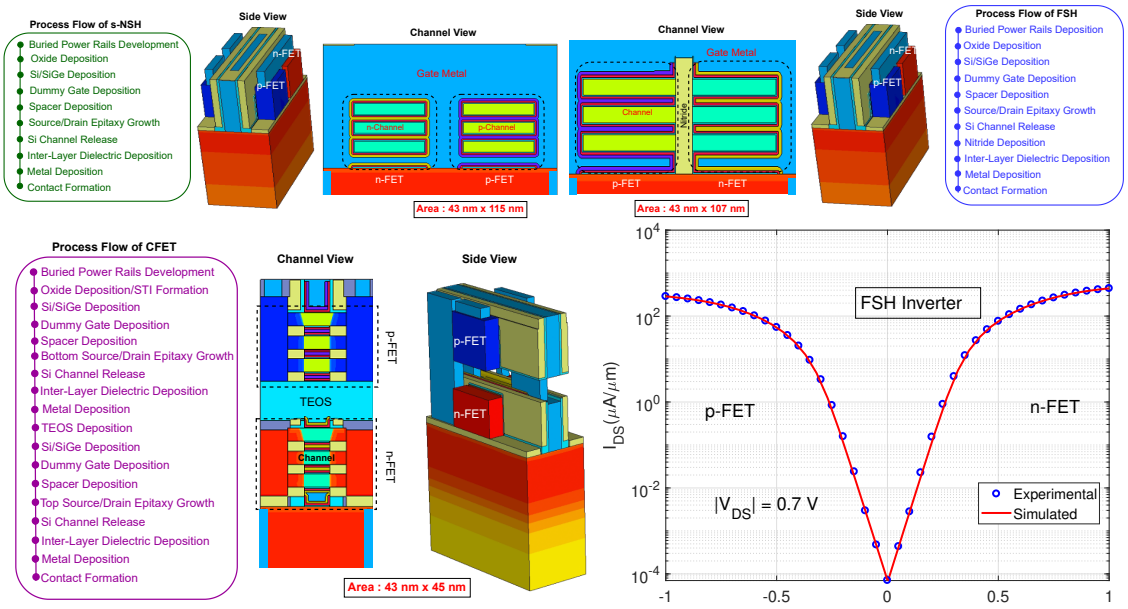

Figure 3.1: Synopsis of 3-D process simulation of novel s-NSH CMOS inverters: Cross-sectional channel and side views of (a) stacked nanosheet CMOS inverter (s-NSH), (b) forksheet inverter (FSH), and (c) complementary field-effect transistor (CFET) with their fabrication process flow, performed in S-process simulation. (d) Transfer characteristics of the three-channel p-FET (left) and n-FET (right) in the FSH inverter configuration from our 3D TCAD simulation and experimental results [83] at $|V_{DS}| = 0.7$ V for 22 nm gate length.

of around 4 KeV; (ix) after that p-FET is masked, the source and drain regions of n-FET are doped using Phosphorous dopant with ion energy of around 6 KeV; (x) the dummy gate and $Si_{0.7}Ge_{0.3}$ are then released using the anisotropic etching technique; (xi) the gate oxides for p-FET and n-FET are alternatively grown using thermal oxidation and followed by HfO_2 deposition; (xii) the metal inter-diffusion technology (MIG) is employed to develop the gate metal electrode; and (xiii) the source and drain contacts are formed on n-FET and p-FET; and (xiv) the contact trench is finally employed to connect the source and drain to BPDN.

The fabrication steps for the FSH inverter are similar to that of the s-NSH inverter, except that the SiO_2 layer is deposited as a placeholder in separation between p-FET and n-FET [in step (iv)]. After the spacer deposition and removal of the placeholder oxide layer, high-k dielectric separation (Si_3N_4, k ~7.4) between n-FET and p-FET is deposited is introduced as the final isolation material [after the step (xi) of s-NSH inverter]. Importantly, high-k dielectric deposition does not require any additional lithography step. On the other hand, p-FET and n-FET for the CFET inverter are grown sequentially. The BPDN is initially fabricated and isolated with the oxide underneath the substrate. The bottom n-FET is fabricated using steps (i) to (vi), which are identical to s-NSH inverter

fabrication steps. The gate patterning is then done by depositing the Titanium aluminide (TiAl) on n-FET. The source and drain are connected to BPDN through the contact trench. After that, the top p-FET is fabricated similarly to n-FET using Tetraethyl orthosilicate (TEOS) for p-n separation. Further, the source and drain regions of top p-FET are partially etched to form source/drain contacts in BPDN [84]. Finally, the gate patterning on p-FET is done using Titanium nitride (TiN) deposition, and the metal contacts are formed.

3.2.3 Setup and Calibration of Experimental Setup

Once the device geometry is developed, the transport properties of three CMOS inverters are modeled by self-consistently solving Boltzmann's transport and Poisson's equation with mobility and quantum correction terms. A more detailed discussion on mobility and quantum correction models for capturing the short channel physics can be found in our previous work [85]. To verify the accuracy of our simulation process and models, Fig. 3.1(d) shows the I-V characteristics of three-channel stacked p-FET and n-FET with FSH inverter configuration from our simulation approach and experimental results [83] for the 22 nm gate length with p-n separation of 17 nm. It is observed that our 3-D process simulation exactly reproduces the reported experimental $I_{DS}-V_{GS}$ characteristics for both p-FET and n-FET in FSH inverter at $|V_{DS}| = 0.7$ V. Further, the short-channel effects are calibrated in our previous work [85]. The calibrated results shows that our modeling methodology accurately describes the short channel effects and quantum-mechanical effects with the essential process dependency of three inverters.

3.3 Switching Performance of CMOS Inverters

3.3.1 Transfer Characteristics of CMOS Inverters

Fig. 3.2 shows the transfer characteristics ($I_{DS}-V_{GS}$) of p-FET and n-FET in CFET, FSH, and s-NSH inverter configurations at $|V_{DS}| = 0.7$ V for the 1 nm technology node. To better understand the performance advantages, these characteristics are plotted at the fixed OFF current of approximately 5 nA/μm (I_{DS} at $V_{GS} = 0$ V and $|V_{DS}| = 0.7$ V). It is observed that three CMOS inverters have nearly identical $I_{DS} - V_{GS}$ characteristics for n-FET and p-FET configurations. The p-FET is observed to have nearly 1.73× lower drive current because the width of p-FET is chosen to be the same as the width of n-FET. It is also found from Fig. 3.2 that the subthreshold slope (SS) for the p-FET in CFET, FSH, and s-NSH inverters is identical at around 77 mV/dec, while the SS of the n-FET in all three configurations is observed approximately 72 mV/dec. Further, the drain-induced

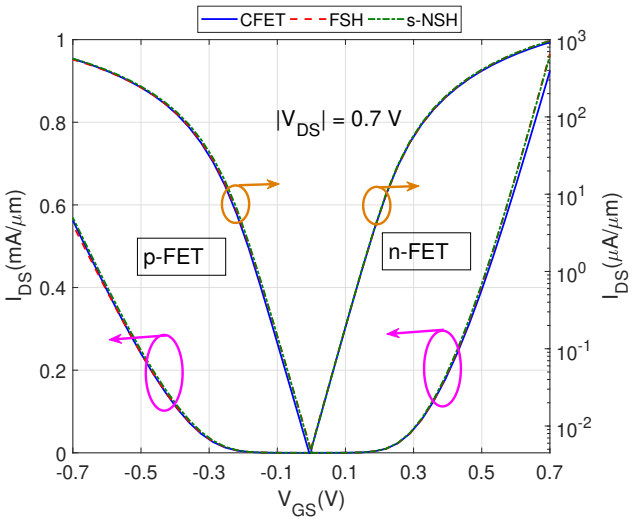

Figure 3.2: Transfer characteristics ($I_{DS}-V_{GS}$) of p-FET (left) and n-FET (right) in CFET, FSH, and s-NSH inverter configurations at $|V_{DS}| = 0.7$ V.

barrier lowering (DIBL) for p-FET in CFET, FSH, and s-NSH inverters is observed to be around 26 mV/V, 27 mV/V, and 31 mV/V, respectively. In contrast, the DIBL of n-FET in CFET, FSH, and s-NSH inverters exhibits approximately 33 mV/V, 34 mV/V, and 36.7 mV/V, respectively. A lower DIBL of devices in the CFET inverter suggests that a vertically stacked arrangement of p-FET over n-FET could effectively minimize the drain field effect due to reduced fringing field between n-FET and p-FET.

3.3.2 Static Performance of CMOS Inverters

Fig. 3.3(a) shows the voltage transfer characteristics (VTC) of CFET, FSH, and s-NSH inverters for $V_{input} = 0 - 0.7$ V at $V_{DD} = 0.7$ V. It is found that three CMOS inverters have perfectly matched VTC with peak output voltage for low input voltages and vice versa. The reason for well-shaped VTC is that the subthreshold leakage currents of p-FET and n-FET are considerably low and do not degrade low- and high-logic states, respectively. A sharp high-to-low transition is observed for a narrow input transition zone in the range of 0.29-0.36 V. Specially, CFET inverter exhibits switching threshold voltage (V_m) at exactly $V_{DD} = 0.33$ V, which is very close to $V_{DD}/2$. Therefore, the highly symmetric VTC of the CFET inverter promises high peak DC gain and better noise margins than the FSH and s-NSH inverters.

Fig. 3.3(b) shows the peak DC gain (A_{vo}) of CFET, FSH, and s-NSH inverters for V_{DD} values in the range of 0.1-0.7 V. It is observed that A_{vo} of the three inverters decreases considerably with the down-scaling of the supply voltage. This trend is attributed to the increment in the gate electric field across the channel region, which results in considerable

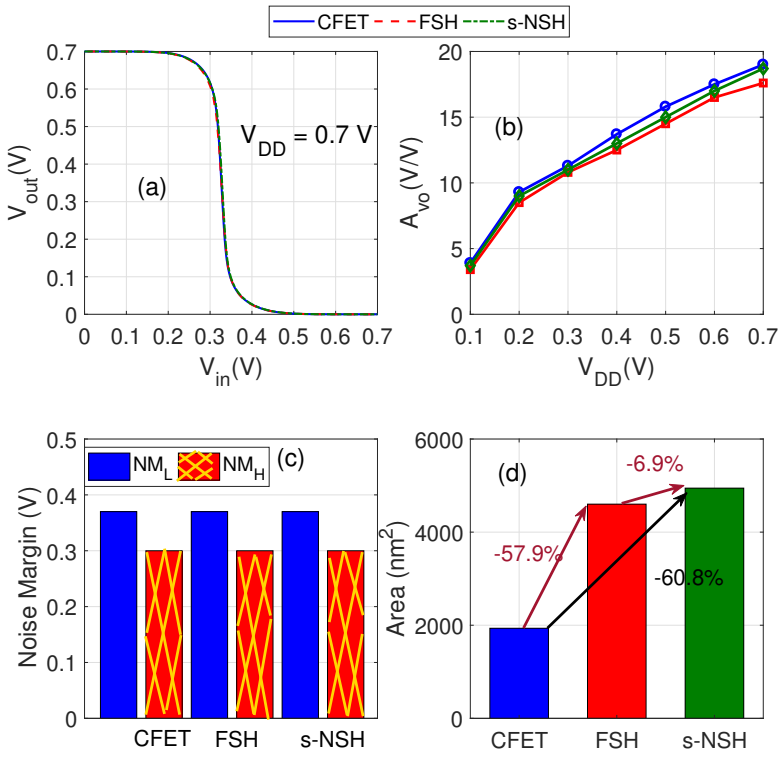

Figure 3.3: Static performance metrics of CFET, FSH, and s-NSH inverters at $V_{\mathrm{DD}} = 0.7$ V: (a) voltage transfer characteristics (VTC) for V_{in} in the range of 0-0.7 V and (b) peak DC gain (A_{vo}) as a function of supply voltage (V_{DD}); (c) high level ($\mathrm{NM_H}$) and low level ($\mathrm{NM_L}$) noise margins, and (d) area footprint.

carrier mobility degradation. The A_{vo} of the CFET, FSH, and s-NSH inverters is found to be around 18.5 V/V, 17.6 V/V, and 18.4 V/V, respectively, at $V_{\mathrm{DD}} = 0.7$ V. This marginal difference in A_{vo} is attributed to the saturation current level of n-FET and p-FET. At iso-peak DC gain (15 V/V), it is observed that the CFET inverter requires -17.8% and -11.1% lower supply voltage than the FSH and s-NSH inverter, respectively. This is because of higher inversion charge density. Specifically, the FSH inverter demonstrates inferior performance, with around -8.3% lower A_{vo} over s-NSH inverter at $V_{\mathrm{DD}} = 0.4$ V. The reason for this is that the highly asymmetric inversion charge density inside the channels of the n-FET and p-FET, caused by reduced gate control. Fig. 3.3(c) shows the high-level noise margin ($\mathrm{NM_H}$) and the low-level noise margin ($\mathrm{NM_L}$), which are calculated from VTC as $\mathrm{NM_H} = \mathrm{V_{OH}} - \mathrm{V_{IH}}$ and $\mathrm{NM_L} = \mathrm{V_{IL}} - \mathrm{V_{OL}}$, respectively. The three CMOS inverters exhibit nearly identical $\mathrm{NM_L}$ and $\mathrm{NM_H}$ of around 0.3 V and 0.36 V of three inverters, respectively. These excellent noise margin levels indicate strong tolerance to signal fluctuations. Therefore, the CFET inverter with higher peak DC gain and noise margins could be a more viable candidate for multistage logic circuits comparable to those of FSH and s-NSH inverters.

Fig. 3.3(d) displays the area footprint of CFET, FSH, and s-NSH inverter cells

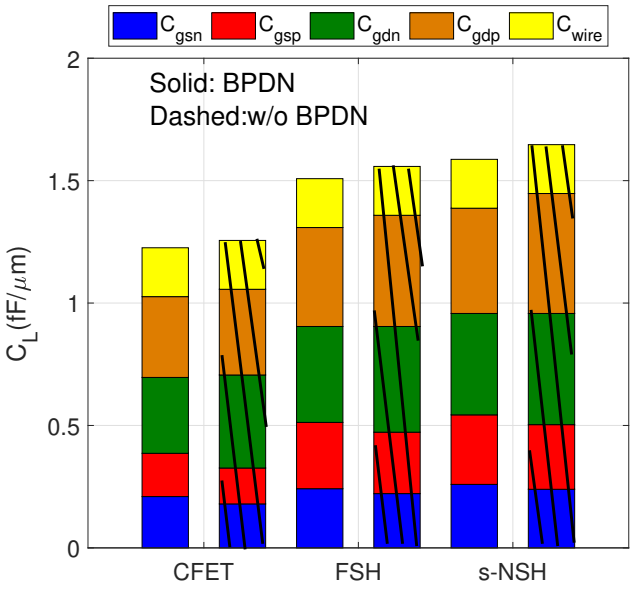

Figure 3.4: Load capacitance (C_L) of CFET, FSH, and s-NSH inverters with buried power rails with frontside connectivity (BPDN) and traditional frontside power delivery network (without BPDN) at $|V_{\mathrm{DS}}| = |V_{\mathrm{GS}}| = 0.7\,V$.

for the 1 nm technology node. The inverter cell area footprint is primarily influenced by gate length (L_g), sheet width ($\mathrm{W_{NS}}$), spacer thickness (t_{sp}), and p-n separation ($D_{N/P}$). The CFET inverter is observed to have a cell area of nearly -60.8% lower than the s-NSH inverter due to the vertical stacking of devices, reducing the contribution of $\mathrm{W_{NS}}$. Additionally, the FSH inverter achieves a -6.9% reduction in area footprint compared to the s-NSH inverter because of significant gate covering from the dielectric side and dummy fin gate tuck. Therefore, the CFET inverter, with its smaller area footprint, could allow high-density integration of digital logic blocks over FSH and s-NSH inverters for the sub-5 nm technology node.

3.3.3 Dynamic Performance of CMOS Inverters

Fig. 3.4 shows the load capacitance (C_L) for CFET, FSH, and s-NSH inverters without and with considering BPDN effects. In this design, BPDN incorporates buried power rails with frontside connectivity. To determine C_L without BPDN, we redesigned the inverters using a traditional frontside power delivery network. The C_L is calculated as $C_L = C_{gdp} + C_{gsp} + C_{gdn} + C_{gsn} + C_{wire}$, where C_{gdp} is the gate-to-drain capacitance of p-FET, C_{gsp} is the gate-to-source capacitance of p-FET, C_{gdn} is the gate-to-drain capacitance of n-FET, C_{gsn} is the gate-to-source capacitance of n-FET, and C_{wire} is the wiring capacitance of the CMOS inverter. The C_{wire} is selected around 0.1996 fF/μm from the IRDS 2021 projection at the 1 nm technology node [79]. The C_{gs} and C_{gd} of p-FET and n-FET are computed using the Y-parameter model by constructing the small-signal

equivalent model [51, 65, 86]. It is observed that the C_L with BPDN for CFET, FSH, and s-NSH CMOS inverters is reduced by around -2.45%, -3.3%, and -4%, respectively. This signify that CFET over FSH and s-NSH inverters could effectively minimize back-of-line parasitic capacitances. It is observed from Fig. 3.4 that the vertical stacking of devices in CFET inverter with BPDN leads to the reduction of C_L around -22.9% and -29.51% than FSH and s-NSH inverters, respectively. This significant improvement in C_L of CFET is primarily due to improvement in DIBL and decrement in coupling capacitances [16]. On the other hand, in comparison to the s-NSH inverter with BPDN, the FSH inverter provides around -5.3% lower C_L because of fringing capacitance reduction with high-k separation. Thus, the CFET inverter with BPDN provides the lowest C_L, making them a potential candidate for high-speed digital ICs.

3.3.4 Impact of Process Variation

Fig. 3.5 shows the coefficient of variation (σ/μ) for threshold voltage (V_{TH}) of n-FET and p-FET in the CFET, FSH, and s-NSH inverter configurations as a function of the device geometrical parameters, such as doping concentration ($N_{S/D}$), EOT, interface trap charges (N_{it}), and channel thickness (t_{ch}). It is observed that the variation in V_{TH} increases significantly with a marginal variation in geometrical parameters. Among the three configurations, the CFET consistently demonstrates superior resistance to V_{TH} fluctuations across all considered geometrical parameters. This improved performance is attributed to its enhanced electrostatic control and tightly packed vertical layout. In comparison, the FSH inverter strikes a balance by offering better isolation between the n-FET and p-FET by reducing cross-coupling effects. However, their lateral proximity results in higher sensitivity to geometrical parameter variations compared to CFET. On the other hand, the s-NSH inverter exhibits the highest sensitivity to variations in the geometrical parameters, particularly those involving dopants and channel thickness. This increased susceptibility arises from strong fringing field effect and pronounced inter-device coupling. Thus, the CFET design inherently mitigates the impact of process parameter variations more effectively than the FSH and s-NSH configurations, which offer a robust solution for achieving stable device performance under varying conditions.

3.3.5 Scaling Performance of Novel CMOS Inverters

Fig. 3.6 shows the key performance metrics for CFET, FSH, and s-NSH inverters as a function of the technology node (N) at a fixed OFF current of around 5 nA/μm. Table 3.1 presents the device design parameters, which are scaled with the technology node. It is

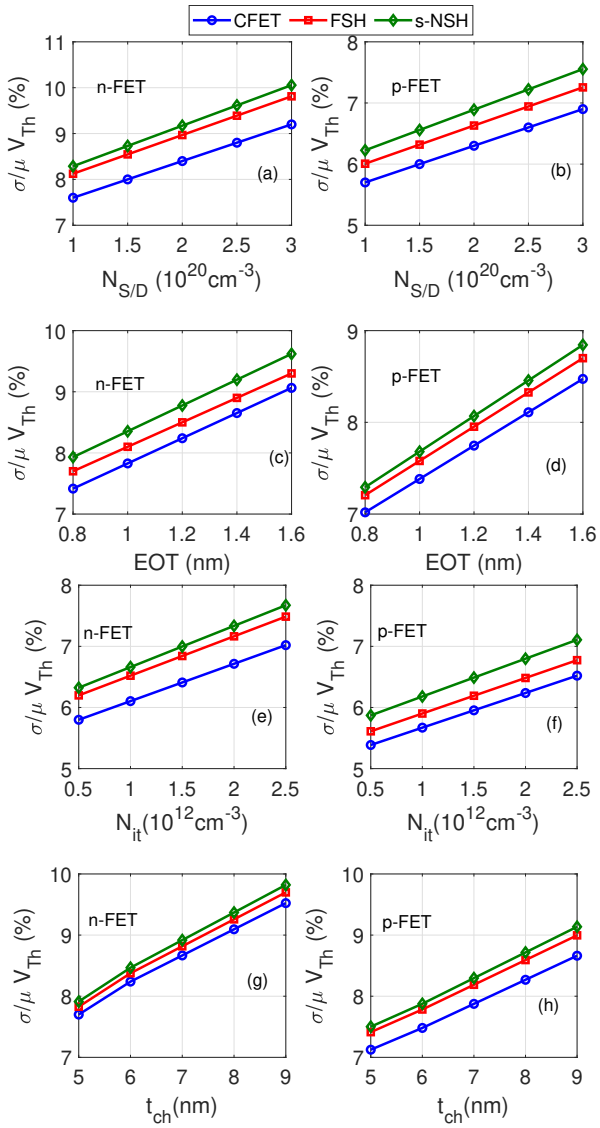

Figure 3.5: Coefficient of variation ($\sigma/\mu \times 100$) for threshold voltage (V_{TH}) of n-FET and p-FET in the CFET, FSH, and s-NSH inverter configurations as a function of (a) and (b) source and drain doping concentration ($N_{S/D}$), (c) and (d) effective oxide thickness (EOT), (e) and (f) interface trap charges (N_{it}), and (g)-(h) channel thickness (t_{ch}).

Table 3.1: Parameters of technology nodes describing the corresponding gate lengths (L_g) and spacer thicknesses (t_{sp}) as per the IRDS 2021 (N1-N5) [79] and the ITRS 2013 roadmap (N0.5-N0.7) [57].

Technology Node (N)	**N0.5**	**N0.7**	**N1**	**N2**	**N3**	**N5**
Gate Length (L_g) (nm)	8	10	12	14	16	18
Spacer thickness (t_{sp}) (nm)	1	1.2	1.4	1.6	1.8	2

observed from Fig. 3.6(a) that the ON current [$I_{DS}(|V_{GS}| = V_{DD}, |V_{DS}| = V_{DD})$] of p-FET and n-FET in three inverter configurations decreases considerably with scaling down the technology node. The reason for that is twofold: (i) source-drain tunneling increases the OFF-state current and thereby requires much lower V_{GS} to achieve the fixed OFF current;

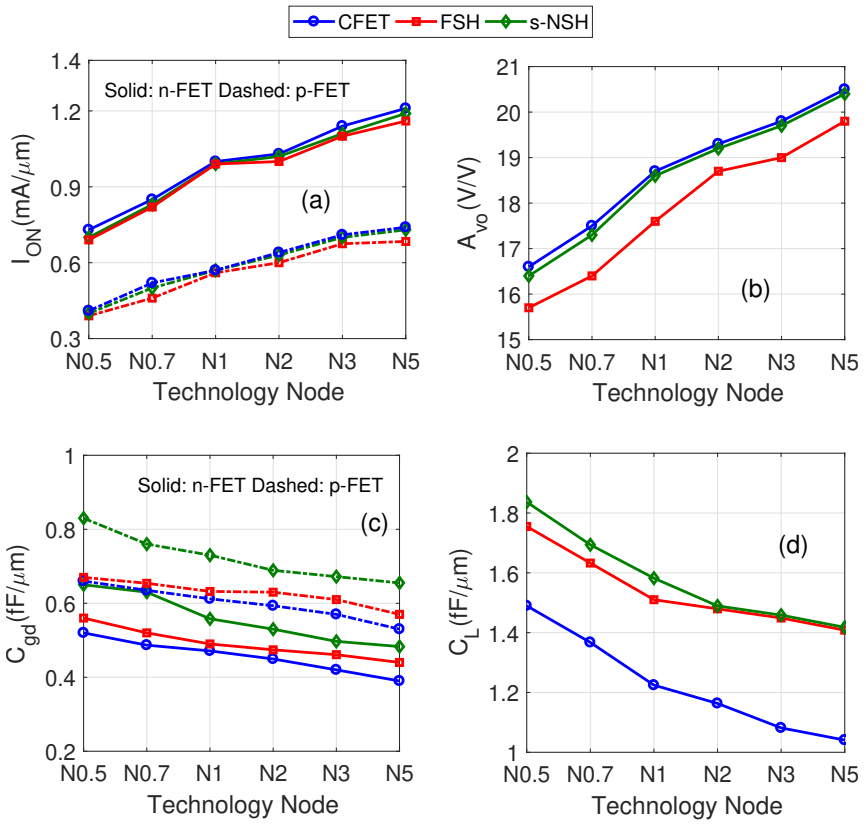

Figure 3.6: Key performance metrics of CFET, FSH, and s-NSH inverters dependency on technology node at $V_{\mathrm{DD}} = 0.7$ V: (a) ON current of p-FET (solid line) and n-FET (dash line) $[I_{\mathrm{DS}}(|V_{\mathrm{GS}}| = V_{\mathrm{DD}}, |V_{\mathrm{DS}}| = V_{\mathrm{DD}})]$, (b) peak DC gain ($A_{vo}$), (c) gate-to-drain capacitance (C_{gd}) (Solid : n-FET, Dashed : p-FET); and (d) load capacitance (C_L) as a function of technology node.

and (ii) the enhanced electric field in the channel region increases the mobility degradation due to a greater number of scattering events. Importantly, the drive current of the n-FET and p-FET in the FSH inverter is marginally lower among the three inverters for all technology nodes. This is due to the fork gate structure, which provides electrostatic control from only three sides. As the technology node scales down from N5 to N0.5, the n-FET of CFET, FSH, and s-NSH inverters experiences -65.75%, -68.12% and -70% degradation in I_{ON}, which is 21.21%, 9.1% and 17.8% higher than that for p-FET. Fig. 3.6(b) shows that the A_{vo} of three inverters decreases considerably with scaling down the technology node due to the decrement in the drive current of n-FET. The A_{vo} of CFET and s-NSH inverters follows the I_{ON} trend, displaying nearly identical A_{vo} across all technology nodes. However, the FSH inverter exhibits the least A_{vo} among the three inverter configurations due to highly asymmetric inversion charge in p-FET and n-FET.

From Fig. 3.6(c), it is found that C_{gd} for p-FET and n-FET in the three inverters show a marginal increment with scaling down the technology node (N). For all N, p-FET and n-FET of CFET inverter demonstrates significantly lower C_{gd} compared to FSH and

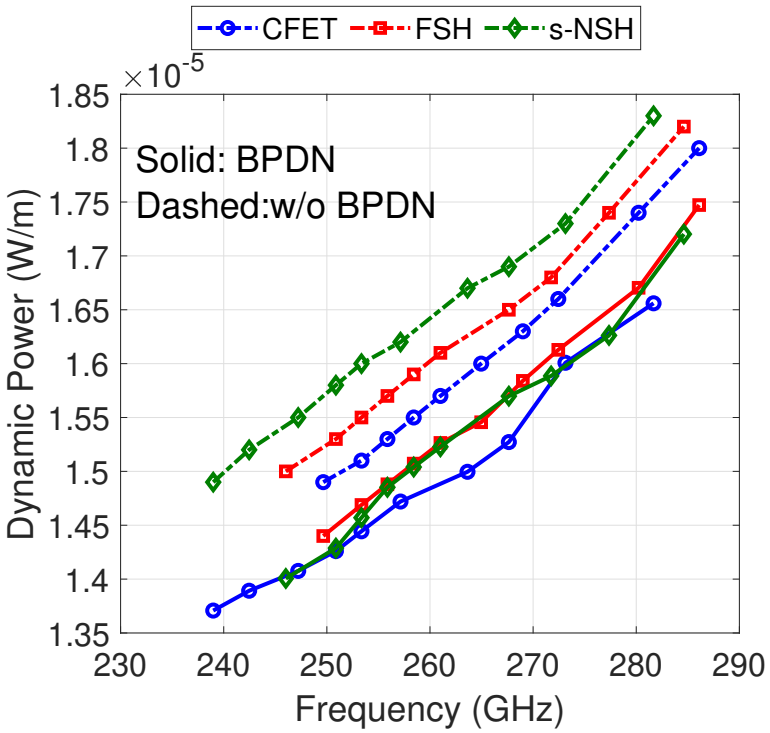

Figure 3.7: Power versus frequency characteristics of CFET, FSH and s-NSH inverters for varying V_{DD} and technology node.

s-NSH inverters. Despite showing inferior A_{vo}, the FSH inverter exhibits a lower C_{gd} compared to the s-NSH inverters due to the reduced fringing field effect. It is observed from Fig. 3.6(d) that the C_L for three inverters increases significantly as the technology node scales down. This increment is primarily due to a significant increment in DIBL, which enhances the contribution of C_{gd} and C_{gs} components. The C_L of the CFET inverter is found nearly 1.49 $fF/\mu m$ at N0.5, which is about 44.6% higher than its value at the N5 node. On the other hand, the C_L for the FSH and s-NSH is gained around 27.14% and 28.17%, respectively, when the technology node scales down from N5 to N0.5. Although CFET has significant increment in C_L from N5 to N0.5, they are observed to maintain their advantage of lower C_L compared to the FSH and s-NSH inverter counterparts across all technology nodes. At N0.5, the C_L of CFET is around -18.67% and -21.33% lower than that for FSH and s-NSH inverter. On the other hand, for technology nodes N1 and below, the FSH inverter has improved C_L over s-NSH inverter. This trend is due to the decrement in the fringing field capacitance with high-k in p-n separation. Thus, as technology nodes continue to scale down, the CFET inverter consistently outperforms its counterparts in I_{ON} and C_L, promising superior performance for advanced technology nodes.

3.3.6 Power Performance Analysis

Fig. 3.7 shows the power-frequency characteristics of CFET, FSH, and s-NSH CMOS inverters by varying V_{DD} and technology node (N) without and with including the BPDN. As demonstrated by the rightward shift, the frequency and power efficiency of CFET with and without BPDN are leading above FSH and NSH-based CMOS inverters. This performance enhancement is attributed to reduced C_L values and improved device currents [as observed in Fig. 3.6]. At the iso-frequency (270 GHz), the CFET inverter with BPDN demonstrates -4.29% and -2.5% power reduction compared to the FSH and s-NSH inverters, respectively. At the iso-power (1.7×10^{-5} W/m), the CFET inverter delivers around 2% and 3.7% frequency improvement compared to the FSH and s-NSH inverters, respectively. Further, the difference in the power consumption between BPDN and without BPDN is observed to be around -9.1%, -4.6% and -6.67% for CFET, FSH, and s-NSH inverters, respectively for N1. This indicates that there is a reduction in parasitic capacitance drop with BPDN. Moreover, due to lower C_L values, the CFET, FSH, and s-NSH inverters with the BPDN have around -4.28%, -4.3% and -7.29% lower operating frequency compared to those without the BPDN at 1.55×10^{-5} W/m. Therefore, among the three inverters, the CFET inverter with BPDN stands out as a promising candidate for future high-speed and low-power logic applications due to its capability to operate at higher frequencies with less dynamic power dissipation.

3.3.7 Impact of p-FET and n-FET Separation

Fig. 3.8 illustrates key performance metrics of CFET, FSH, and s-NSH inverters as a function of p-n separation ($D_{N/P}$) at $V_{\mathrm{DD}} = 0.7$ V. Fig. 3.8(a) shows that the voltage gain (A_{vo}) of the three inverters decreases with increasing the $D_{N/P}$. This trend is due to the increment in the fringing field between n-FET and p-FET, which marginally reduces the drive currents. Specifically, the A_{vo} of CFET, FSH, and s-NSH inverters decreases by -6.9%, -10%, and -8.1%, respectively, when $D_{N/P}$ is increased by a factor of 2.64×. Due to a higher reduction in their device currents, A_{vo} of the FSH inverter is observed to be more sensitive to p-n separation. Fig. 3.8(b) indicates that the C_{gd} for p-FET and n-FET in the three inverters show a marginal increment with decreasing $D_{N/P}$. For all $D_{N/P}$, the devices in the CFET inverter exhibit marginally lower C_{gd} compared to FSH and s-NSH inverters. Further, the FSH inverter is found to attain lower C_{gd} compared to the s-NSH inverters for even higher p-n separation. Fig. 3.8(c) reveals that the C_L of CFET, FSH, and s-NSH inverters increases more significantly compared to C_{gd} with decreasing the

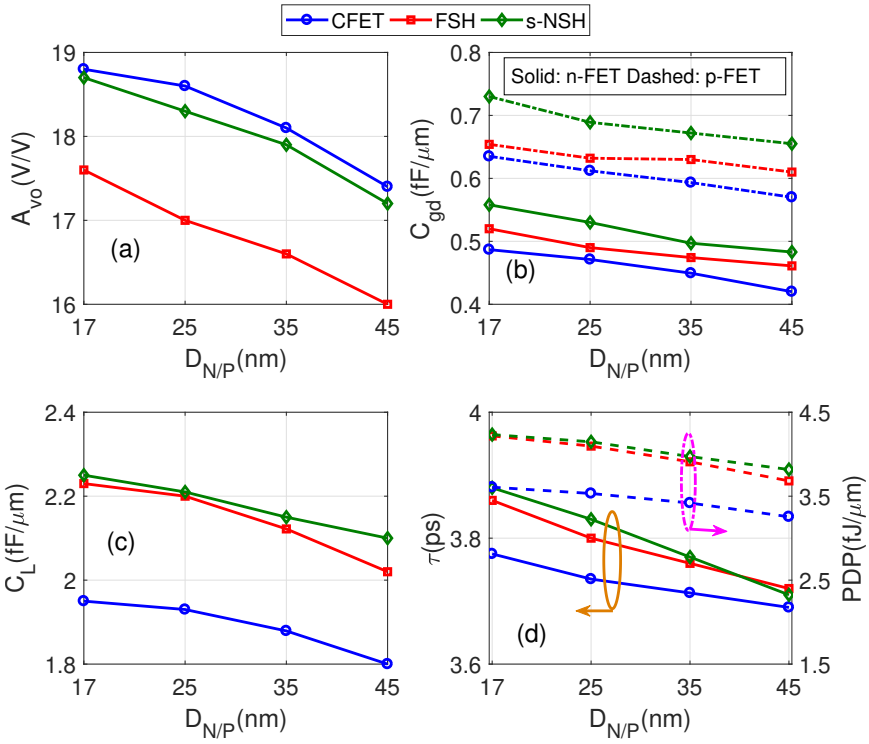

Figure 3.8: Influence of p-n separation ($D_{N/P}$) on important performance metrics of CFET, FSH,and s-NSH inverters at V_{DD} = 0.7 V: (a) peak DC gain (A_{vo}), (b) gate-to-drain capacitance (C_{gd}) (Solid : n-FET, Dashed : p-FET), (c) load capacitance (C_L), and (d) inverter delay (τ) and power delay product (PDP).

$D_{N/P}$ because C_{gs} also rises. It is important to note that the CFET inverter maintains a lower C_L than both FSH and s-NSH inverters for wide range of $D_{N/P}$ values.

Fig. 3.8(d) shows that the delay (τ) and power-delay product (PDP) of the considered inverter configurations marginally rise with decreasing $D_{N/P}$. The CFET and FSH inverters exhibit 1.61% and 3.75% increment in τ whereas 12.5% and 14.13% higher PDP, respectively, when $D_{N/P}$ is scaled down from 45 nm to 17 nm. Further, the s-NSH inverter is highly affected, with around -4.58% and -10.9% degradation in τ and PDP, respectively, when $D_{N/P}$ is scaled down from 45 nm to 17 nm. At $D_{N/P}$ = 17 nm, the CFET demonstrates -2.25% and -2.78% lower inverter delay, while exhibiting -16.9% and -17.38% lower PDP than that for FSH and s-NSH inverters, respectively. Moreover, the FSH inverter exhibits marginally lower delay and PDP compared to the s-NSH inverter. It is found that the three inverters have a marginal difference in performance with $D_{N/P}$, and selecting the optimum $D_{N/P}$ could significantly enhance the performance advantages of particular inverter configuration. Further, the CFET inverter consistently outperforms the s-NSH and FSH inverters across all values of $D_{N/P}$ due to lower C_L. Therefore, CFET inverter with minimum $D_{N/P}$ could be a viable choice to develop high density digital IC.

Table 3.2: Performance Benchmarking of CFET, FSH, and s-NSH at V_{DD} = 0.7 V and fixed I_{OFF} = 10 nA/μm for N1 node.

Inverters	CFET	FSH	s-NSH
Peak DC gain (V/V)	18.5	17.6	18.4
Area Footprint (nm^2)	1935	4601	4945
Load Capacitance (fF/μm)	1.895	2.01	2.12
Power (10^{-5}W/m)	1.62	1.64	1.68
Frequency (GHz)	270	268	260

3.4 Summary

We have conducted a comprehensive performance analysis of CFET, FSH, and s-NSH inverters for the 1 nm technology node using a fully calibrated 3-D process simulation. Our work not only identifies the performance limits of novel s-NSH-based CMOS inverters for sub-5 nm technology nodes but also provides critical insights into the performance of CFET and FSH, which can aid in scaling and device-level analysis. Table 3.2 shows that the CFET inverter offers approximately a 3.7% higher operating frequency and a -3.7% lower dynamic power consumption, with a -60.8% smaller area footprint compared to the s-NSH inverter counterpart for the 1 nm technology node. Moreover, the advantageous characteristics of CFET are observed to persist when scaling down the technology node beyond 1 nm. The results indicate that device gate capacitance play a crucial role in inverter-level performance degradation, which can be optimized by p-n separation. Our device performance analysis and benchmarking demonstrate that the CFET inverter delivers optimal and robust switching performance at the ultimate scaling limits.

Chapter 4

6T SRAM and 32-bit ALU Design Using Novel CMOS Inverter Configurations Based on Stacked Nanosheet FET

4.1 Introduction

In the previous chapter, we perform a comprehensive performance analysis and benchmarking of Si stacked nanosheet (NSH)-based CMOS inverter configurations, including complementary FET (CFET), forksheet (FSH), and standard stacked nanosheet CMOS (s-NSH), using a fully calibrated TCAD simulation. Our study revealed that the CFET inverter demonstrates superior scaling and switching characteristics in terms of peak DC gain, noise margin, operating frequency, and power efficiency compared to FSH and s-NSH inverter counterparts for sub-5 nm technology nodes. Extending this analysis to static random access memory (SRAM) cell and arithmetic logic unit (ALU) is crucial to fully understanding their performance advantages in system-on-chip (SoC) design [87]. The speed and energy efficiency of these systems are critical in defining the performance of modern memory and processor ICs [88]. Thus, evaluating the performance of SRAM and ALU blocks could enable the prediction of system-level behavior and aid in identifying high-performance inverter configurations for next-generation memory and processor development.

6T SRAM cells utilizing CFET and FSH inverters have been actively studied for their potential to enhance cell area scaling and power frequency performance [14, 34, 35, 37, 39]. However, significant attention has been given to understanding the interconnect design and process integration efforts on power efficiency. Simulation work predicts that 6T FSH SRAM could achieve 40% and 10% reduction in read and write energy consumptions, respectively, compared to the s-NSH configuration for the 15 nm gate length (A14), due to reduced interconnect capacitances [34]. Notably, 6T CFET SRAM has shown excellent area and power efficiency, with improvements of approximately 48.2% and 29.4%, respectively, compared to 6T s-NSH SRAM for the 3 nm technology node [89]. Additionally, 6T CFET SRAM with buried power delivery network (BPDN)

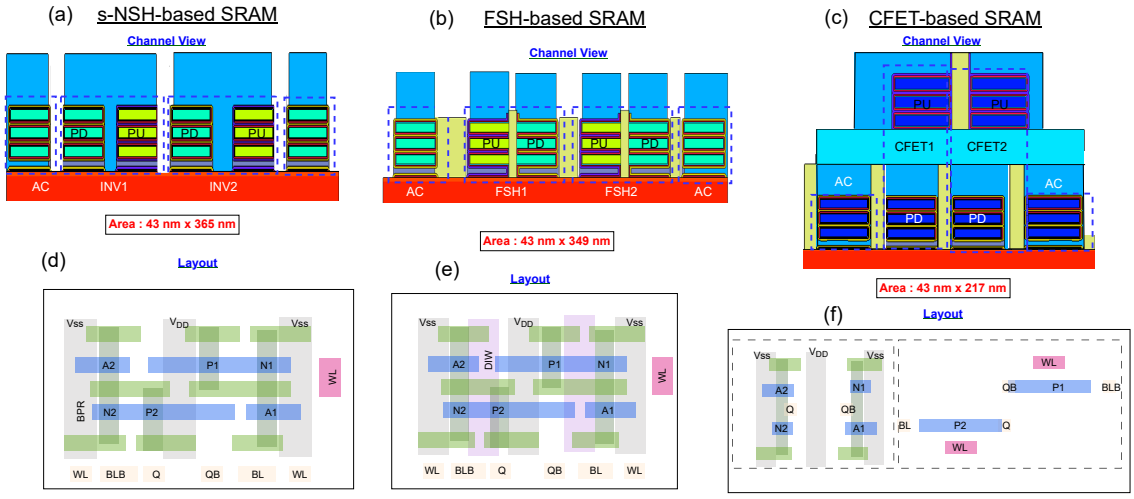

Figure 4.1: Channel view and layout for 6T SRAM cells using (a) and (d) stacked nanosheet (s-NSH), (b) and (e) forksheet (FSH), and (c) and(f) complementary field-effect transistor (CFET) inverter configurations. The legends used in the layouts are explained in the text.

for the 12 nm gate length (A3) has demonstrated the 77% improvement in energy-delay product compared to 15 nm gate length (A14) 6T s-NSH SRAM [33]. Despite recent studies have extensively focused on routing and energy efficiency aspects of 6T SRAM [13, 90], the uniform performance evaluation and benchmarking of CFET, FSH, and s-NSH inverters, particularly with BPDN, is still missing. Furthermore, no study has presented the performance advantages of 6T SRAM cells with CFET, FSH, and s-NSH inverter configurations for future technology nodes. In the case of logic aspects, many recent studies on CFET inverters have designed common logic gates [40, 42]. However, the performance analysis of ALU blocks using FSH and s-NSH configurations has not been thoroughly presented. Therefore, there is a pressing need for a detailed investigation of SRAM and ALU performance with s-NSH inverter architectures to implement efficient memory and logic circuits, respectively.

In this chapter, we examine the scaling and switching performance metrics of 6T SRAM cell and 32-bit ALU employing CFET, FSH, and s-NSH-based inverter architectures, which are designed using BPDN. The performance analysis of the 6T SRAM cell is carried out using 3-D process simulation within a fully calibrated TCAD tool, which is based on the self-consistent solutions of Poisson's equation and the Boltzmann transport equation. Additionally, the ALU is designed by modifying the BCB 4.0, where the I-V and C-V characteristics of CFET, FSH, and s-NSH inverters are included to find computational and energy efficiency. Specifically, the contributions of this work are stated below:

- A process-dependent comprehensive assessment is carried out to understand the

performance of 6T SRAM cells using CFET, FSH, and s-NSH inverters. Thus, our work presents performance and scalability projection in the design technology co-optimization (DTCO) paradigm within advanced technology nodes.

- Extensive effort is devoted to reducing the process steps in fabricating the 6T SRAM cell, as this can serve as a critical bottleneck in technology node scaling. The proposed SRAM layouts offer a solution to mitigate routing congestion challenges for the sub-5 nm technology node.

- Reasonable performance prediction of CFET, FSH, and s-NSH inverters from logic aspects is done by examining the power and computation efficiency of 32-bit ALU.

4.2 Performance of CMOS Inverters in 6T SRAM Configuration

4.2.1 Structure Design

Fig. 4.1(a), (b), and (c) illustrate the channel view of the simulated 6T SRAM cell using s-NSH, FSH, and CFET inverters, respectively. Additionally, Fig. 4.1(d), (e), and (f) present the layout of SRAM cells designed using s-NSH, FSH, and CFET inverter architectures, respectively. It is seen from the SRAM layout that the 6T SRAM cell comprises two pull-up (PU) transistors (P1 and P2), two pull-down (PD) transistors (N1 and N2), and two access (AC) transistors (A1 and A2). To simplify the process, the access transistors are developed alongside the cross-coupled CMOS inverters. The geometrical parameters of the access transistors are kept identical to those of the n-FET (pull-down transistor) to maintain consistency during process simulation. In this configuration, BL and BLB represent the bit lines, WL denotes the word line, and Q and QB are the data storage nodes. In our design, the spacing between the n-FET and p-FET regions is treated as a gate cut, and the effective transistor width is determined by accounting for the maximum spacing after gate-cut adjustments. It is observed from Fig. 4.1(d) and (e) that a major difference between s-NSH and FSH SRAMs layouts is thin dielectric walls (DIWs), which reduces the p-n separation. Fig. 4.1(c) showcases the CFET layout, where PU transistors are stacked above the PD and AC transistors. This vertical stacking reduces track height and overall cell area. The 6T CFET SRAM cell layout includes PD and AC n-FETs in the first (bottom) layer and PU p-FETs in the second (top) layer. A buried power rail network (BPRN) is incorporated to provide the supply connection through the substrate, which offers significant benefits for power delivery and layout efficiency.

4.2.2 Process Design

The process steps of realizing the 6T SRAM cells are similar to the inverter process flow, except that 6T FSH and CFET SRAMs have the silicon nitride isolation between the access transistors and cross-coupled inverters. The three-channel stacked access (AC) transistors are fabricated together with pull-up (PU) and pull-down (PD) transistors in FSH and s-NSH SRAMs. Further, the silicon nitride is deposited after step (x) of the s-NSH process flow, as mentioned in the Chapter 3. In the case of 6T CFET SRAM, the AC transistors are built side by side with pull-down transistors. After that, silicon nitride is deposited to isolate the PD and AC transistors. Considering the balanced design parameters of the SRAM cell, the transistor strengths are optimized to achieve the PU:PD:AC strength of 1:1:1. Moreover, upon successfully developing the 6T SRAM cells, the transport and correction models are employed similar to those discussed in our Chapter 3 for inverter.

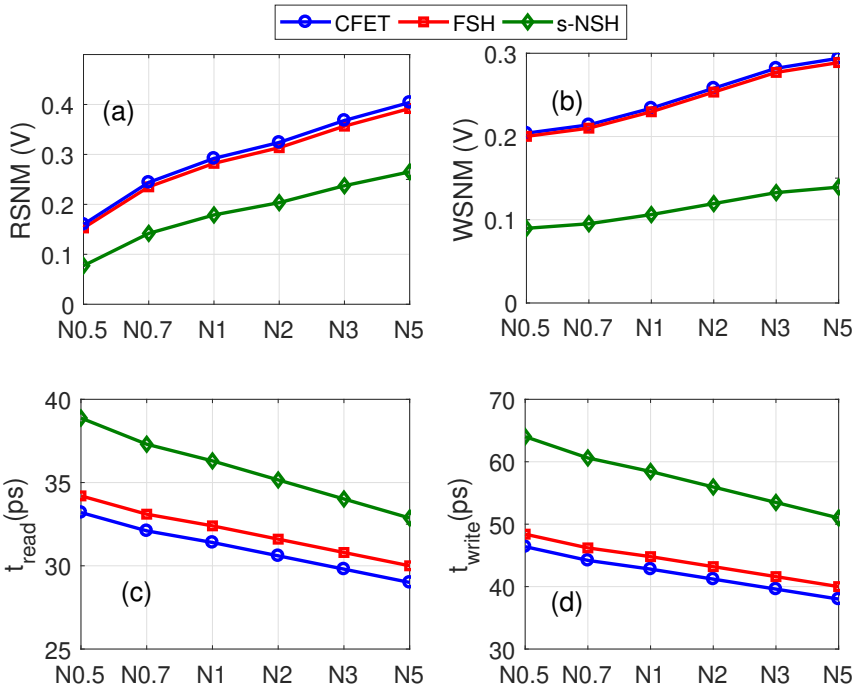

Figure 4.2: Performance of 6T CFET, FSH, and s-NSH SRAM cells at the fixed OFF current of around 5 nA/μm and $V_{DD} = 0.7$ V: (a) read static noise margin (RSNM), (b) write static noise margin (WSNM), (c) read access time (t_{read}), and (d) write access time (t_{write}) as a function of technology node.

4.2.3 Read-Write Performance Analysis

Fig. 4.2(a) illustrates the read static noise margin (RSNM) of the 6T SRAM cell using CFET, FSH, and s-NSH inverters as a function of the technology node (N) at $V_{DD} = 0.7$ V. The RSNM is a crucial stability performance metric that defines the minimum

tolerable noise voltage of the SRAM cell without flipping the state. It is observed that RSNM for the three SRAM cells decreases significantly with decreasing the technology node due to the reduction in the drive current of their n-FET. The CFET and FSH SRAM cells exhibit nearly identical RSNM due to their almost matched cell ratio. The cell ratio is defined as the ratio of pull-down and access transistor strengths [91]. A marginally higher RSNM for CFET SRAM is noted among three SRAMs due to its higher drive current of n-FET, which prevents the flipping of the original state. However, the s-NSH SRAM cell exhibits a markedly lower RSNM compared to the CFET SRAM cell, with approximately -40% degradation observed at N1. A substantial reduction in RSNM with the technology node highlights the challenges in maintaining read stability for s-NSH SRAM as scaling continues.

Fig. 4.2(b) presents the write static noise margin (WSNM) of the 6T SRAM cell using CFET, FSH, and s-NSH inverters as a function of the technology node at $V_{\mathrm{DD}} = 0.7$ V. The WSNM is also a critical stability performance metric that defines the maximum bit-line voltage (BL) required to flip the state of the SRAM cell. At a given technology node, the 6T CFET and FSH SRAM cells exhibit nearly the same WSNM due to their same pull-up ratio. The pull-up ratio is defined as the ratio of the strength of the pull-up transistor to the access transistor [91]. The WSNM of the s-NSH SRAM is found to be around -50% lower than that of the CFET SRAM for all technology nodes. CFET and FSH SRAM cells are found to retain their inverter-level advantages with higher WSNM compared to s-NSH SRAM. This is because the oxide in p-n separation effectively minimizes the fringing field effect. Thus, the 6T CFET SRAM cell demonstrates superior read and write stability over the FSH and s-NSH SRAM cells for sub-5-nm technology nodes.

Fig. 4.2(c) and Fig. 4.2(d) respectively show the read access time (t_{read}) and write access times (t_{write}) of the 6T SRAM cells as a function of the technology node at $V_{\mathrm{DD}} = 0.7$ V. The t_{read} is computed as the time required for achieving the bit-line (BL) voltage difference equals to the 10% of V_{DD} after the word-line (WL) is activated. On the other hand, t_{write} is calculated as the time WL reaches 50% of V_{DD}, which is basically BL and $\overline{\mathrm{BL}}$ reach the same value. It is observed that t_{read} and t_{write} increase significantly with the scaling down technology node due to the increment in C_{BL} and the decrement in the drive currents of the PU and PD transistors. Among the three SRAM cells, 6T CFET SRAM exhibits smaller t_{read} and t_{write} for all the technology nodes because a lower C_{gd} for both PU and PD transistors results in smaller C_{BL} and C_{WL}. In contrast, the

increased capacitance combined with inferior drive currents in 6T s-NSH SRAM leads to slower charging and discharging times for the BLs and WLs, which significantly enhance the t_{read} and t_{write}, respectively. At N1, 6T CFET SRAM exhibits -42.9% and -68.4% lower t_{read} and t_{write}, respectively, compared to 6T s-NSH SRAM. This disparity is due to the marginally higher PD drive current and lower C_{BL} than the 6T s-NSH SRAM. Therefore, the CFET configuration with faster read and write response times could be a more preferable choice for designing high-speed memory.

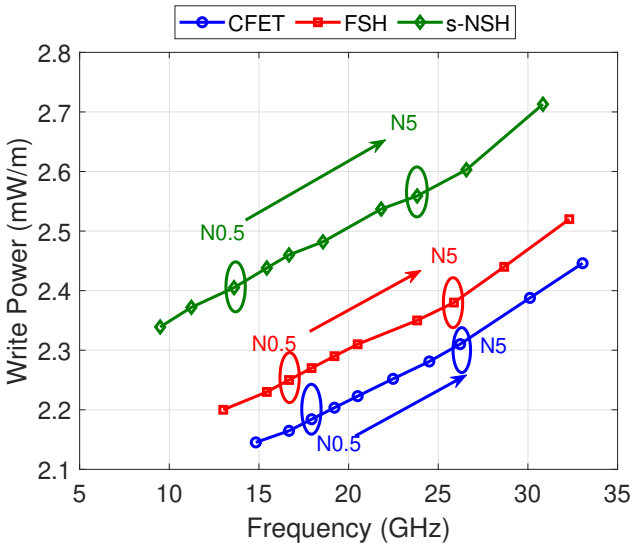

Figure 4.3: Power versus frequency characteristics of 6T CFET, FSH, and s-NSH SRAM cells for varying V_{DD} and technology node.

4.2.4 Power Performance Analysis

Fig. 4.3 shows the power frequency characteristics of a 6T SRAM cell using CFET, FSH, and s-NSH inverters, which are obtained by varying the node of technology and the supply voltages (V_{DD}). It is observed that 6T CFET SRAM exhibits superior power efficiency and high-frequency operation due to their reduced gate-drain capacitance (C_{gd}), which in turn lowers C_{BL} and C_{WL}. At iso-power conditions (2.4×10^{-3} W/m), 6T CFET SRAM shows an operating frequency of approximately 13.33% and 56.67% higher compared to the FSH and s-NSH SRAMs, respectively. Under iso-frequency conditions (25 GHz), 6T CFET SRAM demonstrates write power efficiency improvements of -3.06% and -12.29% relative to FSH and s-NSH SRAMs, respectively. In addition, 6T s-NSH SRAM suffers from increased power consumption and lower frequency operation due to substantial higher values of C_{BL} and C_{WL}. 6T FSH SRAM strikes a balance between CFET and s-NSH SRAMs by offering moderate gain in power consumption and frequency characteristics. FSH SRAM technology effectively suppresses the fringing contribution

in C_{gd}, which reduces power consumption compared to s-NSH SRAM, although not as effectively as CFET SRAM. Compared to inverter-level performance, the 6T CFET SRAM is observed to enhance power consumption by nearly 135× and reduce frequency by 11.7× for the 1 nm technology node. The s-NSH SRAM is found to have a significantly higher degradation in power and frequency compared to its inverter-level performance. Thus, the superior performance metrics of the CFET inverter in 6T SRAM underscore its potential as a promising solution for future SRAM technologies.

4.3 Performance of NSH-based CMOS Inverters in 32-bit Arithmetic Logic Unit (ALU)

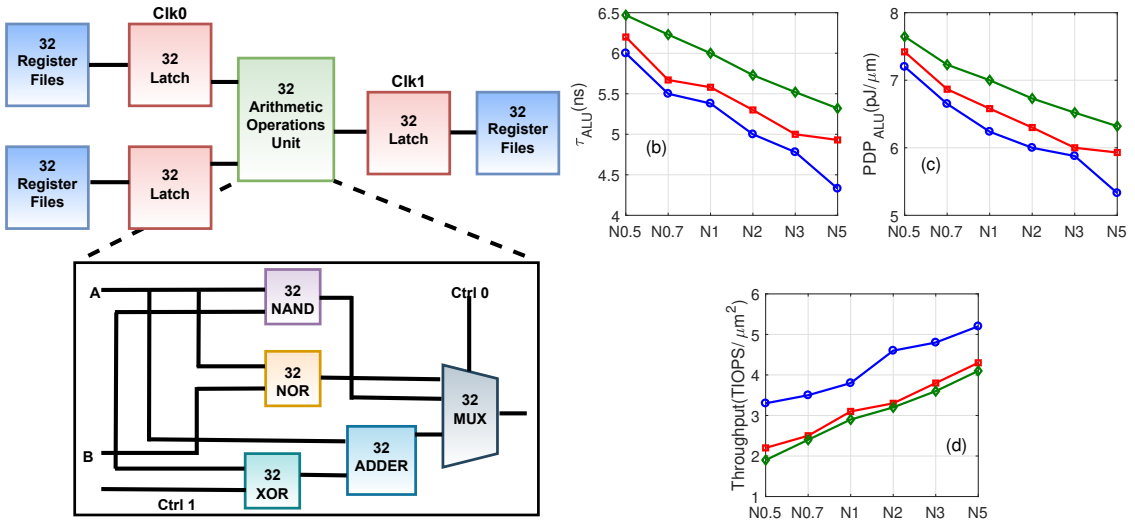

Figure 4.4: Performance of CFET, FSH, and s-NSH inverters in 32-bit arithmetic logic unit (ALU) at V_{DD} = 0.7 V: (a) block-level schematic of 32-bit ALU; and (b) delay of ALU (τ_{ALU}), (c) power delay product ($\mathrm{PDP_{ALU}}$), and (d) throughput (tera-integer-operation-per-second (TIOPS)/μm^2) as a function of technology node.

We here design 32-bit ALU using CFET, FSH, and s-NSH configurations to understand their performance benefits in logic applications. Fig. 4.4(a) shows the schematic of the simulated 32-bit ALU, where the full adder, multiplexer, multi-input NAND, NOR, and XOR gates are developed using CFET, FSH, and s-NSH inverters. The central component of the ALU is the arithmetic operation unit (AOU), which is responsible for performing all arithmetic and logic operations on two 32-bit numbers. The logic operation is performed in parallel, but the adder block, which is developed using a ripple carry adder, limits the operational delay due to carry propagation from one bit to another. The other critical components of the ALU include the register files (RF) and the latches, each organized as 1 × 32 arrays of memory cells. The RFs store input and output data, while the latches transfer and isolate data from the RF in synchronization with the

clock signal. These 32-bit ALU operations are executed by modifying BCB 4.0 [92, 93], where the characteristics of the CFET, FSH and s-NSH inverters are modeled to obtain performance metrics, such as delay, power-delay product and throughput.

Fig. 4.4(b) shows the delay of 32-bit ALU (τ_{ALU}), which is significantly contributed by the delay of the AOU block, as a function of the technology node. It is observed that the τ_{ALU} of CFET, FSH, and s-NSH ALUs increases significantly with decreasing the technology node due to considerable increment in the delay at the inverter level. Interestingly, the CFET configuration is found to preserve their inverter level performance benefits in τ_{ALU} with around -2.39% and -13.7% smaller compared to FSH and s-NSH ALU, respectively, at N1. The τ_{ALU} of CFET configuration is observed to be around 5.45 ns at N1, which is 1475.4× higher than that for their inverter configuration. Moreover, the τ_{ALU} of FSH configuration is found to be marginally higher than CFET configuration, while -11.11% reduced τ_{ALU} is reported compared to s-NSH inverter for N1 due to lower C_L values.

Fig. 4.4(c) shows the PDP of 32-bit ALU ($\mathrm{PDP_{ALU}}$) as a function of the technology node. The trends in $\mathrm{PDP_{ALU}}$ for three configurations have a similar dependence on the technology node as observed for the τ_{ALU}. The $\mathrm{PDP_{ALU}}$ of the CFET configuration is found to be the lowest among the three configurations for all nodes of technology due to their smaller C_L. Furthermore, CFET, FSH, and s-NSH ALU show around -38.4%, -19.35%, and -20.31% degradation in PDP, respectively, when the technology node is reduced from N5 to N0.5. Despite significant degradation in $\mathrm{PDP_{ALU}}$, CFET ALU outperforms FSH and s-NSH ALU for all technology nodes. It is also found that $\mathrm{PDP_{ALU}}$ of CFET ALU is around 6.2 $pJ/\mu m$, which is around -12.9% lower than that for s-NSH ALU cell, at N1.

Fig. 4.4(d) shows the throughput of 32-bit ALU using the CFET, FSH, and s-NSH inverters as a function of the technology node. The throughput is defined as the number of operations executed per second per unit area. It is found that the throughput of the three ALU configurations decreases considerably with scaling down the technology node. The reason for this is that the τ_{ALU} decreases the computation speed of 32-bit ALU. Further, the throughput of CFET ALU drops around -62.50%, while FSH and s-NSH ALUs demonstrate a significant reduction with around -80.4% and -85.7%, respectively, when the technology node is scaled down from N5 to N0.5. At N1, the CFET ALU maintains its advantages, exhibiting nearly 18.75% and 26.67% higher throughput than FSH and s-NSH ALU. Therefore, it is evident that the development of ALU with CFET

could be more beneficial in terms of throughput, speed, and power efficiency compared to FSH and s-NSH ALU counterparts for 5 nm and beyond technology nodes.

Table 4.1: Benchmarking of 6T SRAM and 32-bit arithmetic logic unit (ALU) at $V_{DD} = 0.7$ V for 1 nm technology node.

Attributes	**Delay (ps)**			**PDP** ($fJ/\mu m$)	
	SRAM		**ALU**	**SRAM**	**ALU**
	t_{read}	t_{write}			
CFET	31	42	5450	3.47	6200
FSH	32	44	5580	3.5	6620
s-NSH	36	58	6200	4	7000

4.4 Summary

We conducted a detailed performance analysis of 6T SRAM and 32-bit ALU cells utilizing CFET, FSH, and s-NSH-based inverters for 5 nm and beyond technology nodes. Table 4.1 further summarizes the key switching performance parameters for these configurations at the 1 nm technology node. Our findings reveal that the 6T CFET SRAM significantly enhances operating speed and energy efficiency, with approximately -38.1% lower delay and -15.27% lower power-delay product compared to the 6T s-NSH SRAM cell. The 6T FSH SRAM offers a balanced compromise between CFET and s-NSH SRAMs by providing moderate improvements in both power consumption and frequency performance. Furthermore, the 32-bit ALU with CFET inverters exhibits a 13.7% higher operating speed, -12.9% lower power dissipation, and 26.67% higher throughput compared to ALUs using s-NSH inverters for 1 nm technology node. Notably, CFET inverter demonstrates their suitability for advanced technology nodes with notable enhancements in operating frequency with marginal increment in power consumption than FSH and s-NSH inverters. Overall, our inverter-to-circuit level analysis strongly suggests that CFET inverter configurations are exceptionally well-suited for low-power and high-speed digital IC applications at the ultimate scaling limits.

Chapter 5

Emulation of Synapse using Nanowire based Charge Trap Transistor

5.1 Introduction

Neuromorphic computing system presents a promising solution to circumvent von Neumann architecture limitations, as they offer several advantages, including extensive parallelism, distributed processing, adaptability, self-organization, fault tolerance, stability, energy efficiency, and robustness [94]. The replication of synapse stands as a crucial element in the hardware implementation of a neuromorphic computing system that requires the emulation of synaptic characteristics, including spike-time-dependent plasticity, short-term memory (paired-pulse facilitation and depression), and long-term memory (potentiation and depression) [44]. In recent years, several non-volatile memory devices, such as resistive random access memory (RRAM) [95], ferroelectric field-effect transistor (FeFET) [96], and magnetic tunnel junction (MTJ) [97], have emerged as possible options to develop artificial synapses. However, these devices face major challenges in commercial production within CMOS-compatible processing techniques due to processing temperature requirements and material mismatch, and reliability issues [18]. Moreover, the inherent non-linear and non-uniform conductance modulation of these devices can lead to considerable degradation in learning accuracy and energy efficiency, limiting the potential advantages of such synapses [95]. Hence, it is imperative to tackle these challenges to allow seamless integration of synaptic devices in practical crossbar array size.

A three-terminal charge trap transistor (CTT) with a high-k oxide gate, such as HfO_2, Si_3N_4, and Al_2O_3, has been emerged as a promising synaptic element due to their full CMOS compatibility with three-dimensional (3-D) integration capability, high dynamic range, and superior retention capability [18]. Interestingly, the enhancement of charge trapping using radiation doses in high-k CTT has made significant progress in achieving high threshold voltage modulation (ΔV_{Th}) [18, 21], which renders them potential candidates for facilitating multistate operations in analog synaptic devices. Earlier experimental studies on CTT utilizing HfO_2 trapping oxide layer have reported

excellent weight tunability and weight-dependent plasticity using commercial 32 nm silicon on insulator (SOI) and 14 nm Fin field-effect transistor (Fin-FET) technologies without adding any process complexity or masks steps, which was a critical bottleneck in Flash memory [18, 24]. Further, the 784 × 784 synaptic crossbar array using 28 nm bulk CMOS technology has presented 95% accuracy for handwritten digit recognition with the 8-bits/cell [21]. More interestingly, HfO_2-based fully depleted SOI (FDSOI) demonstrated superior programming efficiency with charge retention of more than 10 years at 125^oC [98].

Despite these advancements, existing CTTs are utilizing planar and Fin-FET device architectures, which are highly susceptible to short-channel effects [18, 24]. This could exacerbate variability and reliability issues in neural network implementation [21]. Therefore, there is a pressing need for the advancement of synaptic devices that can support technology scaling and enable the development of high-density crossbar networks. Silicon nanowire-FET (NW-FETs) with high drive currents and more immunity against the short-channel effects [85], could be a strong CTT candidate. Moreover, Si NW-based charge trap transistor (NW-CTT) could be well-suited for high-density crossbar arrays due to their smaller area footprint over Fin-FET and nanosheet-FET [85]. Previous simulation studies on the NW-FET have demonstrated silicon–oxide–nitride–oxide–silicon (SONOS) memory as a synapse [44], [99], [100]. However, tackling the challenge of decreasing their operational voltage demand and simplifying fabrication steps stands as a crucial endeavor. To tackle these challenges, the conventional HfO_2-based NW-CTT with enhanced interface trap charge density could emerge as a formidable competitor for the synaptic device. However, synaptic characteristics of HfO_2-based NW-CTT have not yet been thoroughly investigated. Therefore, it would be beneficial to investigate the device-to-crossbar performance of HfO_2-based NW-FETs using rigorous models and numerical simulations before undertaking more extensive experimental efforts.

In this chapter, we perform a systematic suitability analysis for HfO_2-based NW-CTT as an artificial synapse in the 5 nm technology node by investigating short-term and long-term memory characteristics with understanding recognition accuracy and energy efficiency in 784 × 100 × 10 neural network. The synaptic characteristics of NW-CTT are examined using a fully calibrated technology computer-aided design (TCAD) tool, based on the self-consistent solutions of Poisson's equation, Boltzmann transport equation, and self-heating equations. Previous simulation studies on CTT have overlooked the self-heating effect [101], but recent experiment demonstration of self-heating induced V_{Th} modulation put the pressing demand for incorporation of this effect [98].

5.2 Simulation Technique

5.2.1 Device Design and Simulation Methodology

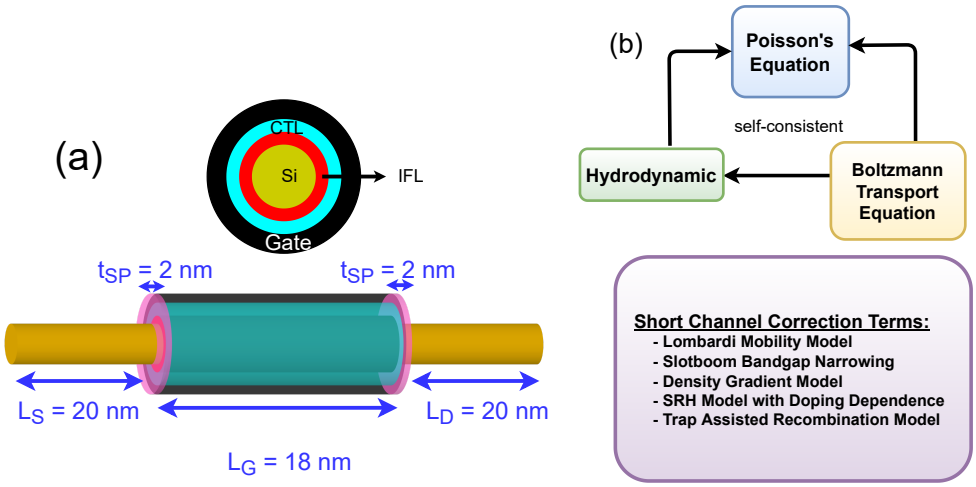

Figure 5.1: Synopsis of modeling methodology and experimental verification: (a) Schematic geometry of NW-CTT at 5 nm technology node (18 nm gate length), and (b) summary of the modeling methodology.

Fig. 5.1(a) shows the schematic of HfO_2-based NW-CTT, where the device design parameters are selected from the IRDS projection for the 5 nm technology node [102]. The gate length (L_g) and spacer length (L_{sp}) of the device are selected around 18 nm and 2 nm, respectively. The source (S) and drain (D) regions ($L_{S/D}$) are considered to be around 20 nm long and doped to n-type with a doping concentration of $N_{S/D} = 1 \times 10^{20}$ cm^{-3}. Further, the diameter (D_{nw}) of the silicon nanowire is selected around 10 nm, which is in line with the experimental achievable value [59]. The gate oxide consists of a stack of 1 nm SiO_2 and 1.25 nm HfO_2, resulting in an effective gate oxide thickness (EOT) of around 1.2 nm. Here, HfO_2 serves as the charge trapping layer (CTL), while SiO_2 functions as the interfacial layer (IFL). Moreover, the chosen thicknesses of SiO_2 and HfO_2 in FDSOI and bulk technology have been reported to provide an excellent charge retention capability of around 10 years [18, 103].

The synaptic characteristics of the NW-CTT are investigated using a fully calibrated 3-D Sentaurus TCAD simulation, based on self-consistent solutions of the Boltzmann transport equation, Poisson's equation, and hydrodynamic, as shown in Fig. 5.1(b). The hydrodynamic model is particularly selected to accurately capture the self-heating effect across the device. The temperature-dependent Shockley-Read-Hall and Auger recombination are incorporated to account the generation and recombination of the carriers in the carrier continuity equation [44, 85]. The non-local band-to-band tunneling

and Hurkx trap-assisted tunneling (TAT) models are included to incorporate the band-to-band tunneling [44]. Moreover, the Density-Gradient model is employed to define the quantum confinement effects in the inversion layer near the Si–SiO_2 interface. Additionally, a low-field ballistic model is integrated to account the quasi-ballistic transport [85]. Several correction models, including Old-Slotboom band gap narrowing, Lombardi mobility, and inversion and accumulation layer mobility, are further included to address bandgap narrowing, doping, and electric-field-dependent mobility degradation, respectively [85]. Further, the interface trap density in the CTL layer is considered to be in the range of $N_{it} = 1\times10^{14}\,cm^{-3}$ to $N_{it} = 1\times10^{17}\,cm^{-3}$ with a capture cross-section area of approximately $1 \times 10^{-14}cm^2$. These interface traps are uniformly situated within the energy levels of 1.2–2.2 eV below the bottom edge of the conduction band (CB) [104]. It is important to note that the selected interface trap charge density is in good agreement with the experimentally reported values in the HfO_2-based FDSOI-CTT using total ionization radiation [18, 24].

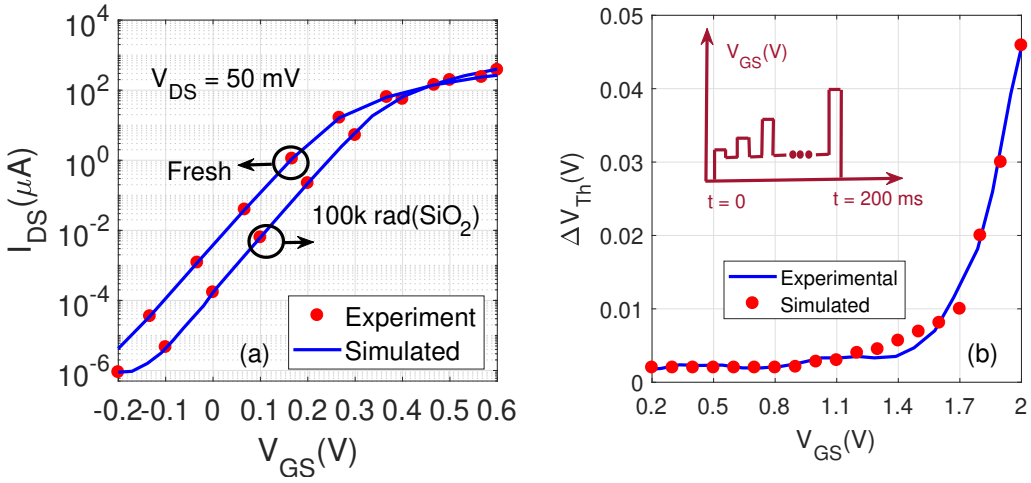

Figure 5.2: Calibration of simulated and experimental characteristics: (a) transfer characteristics (I_{DS}-V_{GS}) of 14 nm technology node Fin-FET for Fresh and 100 krad(SiO_2) irradiation [24] at V_{DS} = 50 mV, and (b) ΔV_{Th}-V_{GS} of FDSOI MOSFET [98] at V_{DS} = 0.5 V for 22 nm technology node. The device design parameters for both Fin-FET and FDSOI are identical to experimental reported device geometry.

5.2.2 Setup and Calibration of TCAD Simulation

To validate the accuracy of the simulation model, Fig. 5.2(a) shows the transfer characteristics (I_{DS}-V_{GS}) of two-fins Fin-FET with a total effective fin width of 150 nm for a 14 nm technology node using our simulation approach and experimental data under Fresh and 100 krad(SiO_2) condition at V_{DS} = 50 mV [24]. It is observed that the simulated I_{DS}-V_{GS} curve, incorporating $N_{it} = 1 \times 10^{16}\,cm^{-3}$ in the CTL layer, exhibits

an excellent agreement with the experimental results. This indicates that our simulation model accurately captures the essential physics of interface trap charges and short-channel effects.

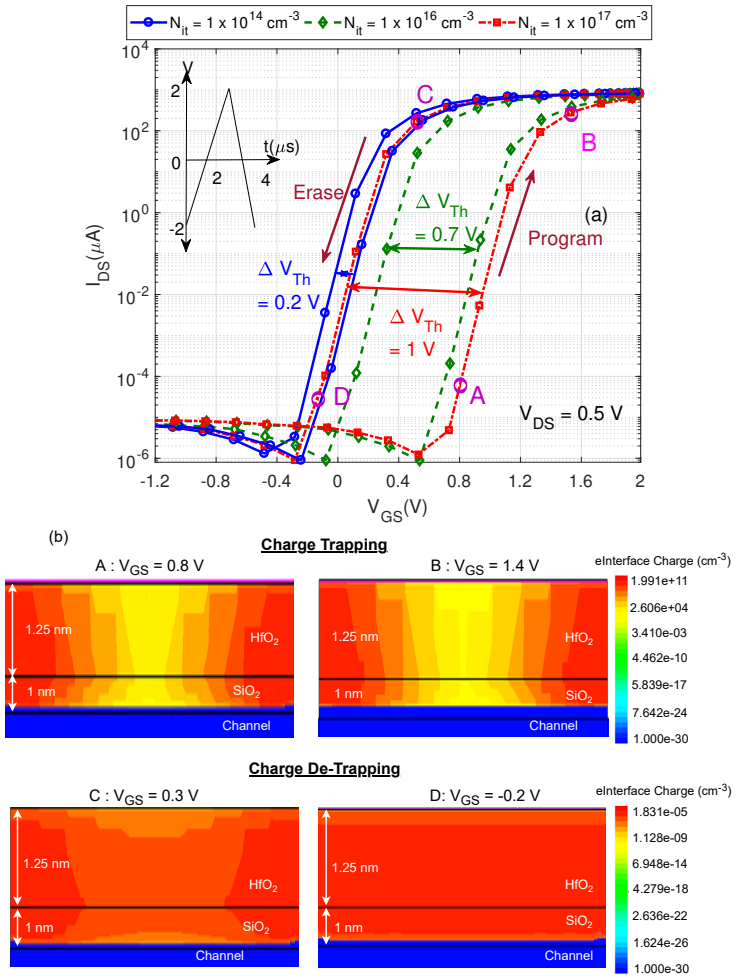

Figure 5.3: Program/erase characteristics of the NW-CTT at $V_{\mathrm{DS}} = 0.5$ V and room temperature: (a) I_{DS}-V_{GS} characteristics under the different N_{it} for the voltage sweep of 2 V/μs, and (b) 2-D electron interface charge profile for $V_{\mathrm{GS}} = 0.8$ V (state A), $V_{\mathrm{GS}} = 1.4$ V (state B), $V_{\mathrm{GS}} = 0.3$ V (state C), and $V_{\mathrm{GS}} = -0.2$ V (state D) at the $N_{\mathrm{it}} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$.

To verify both the program and erase phenomena, we have calibrated the simulation models for 22 nm CTT-based FDSOI technology. Fig. 5.2(b) shows the ΔV_{Th} (memory window), which represents the current difference between the programming and erase cycles. For ΔV_{Th} computation, we apply a Pulsed Gate Voltage Ramp Sweep (PVRS) ranging from 0 V to 2 V with a step size of 50 mV for a duration of 200 ms at $V_{\mathrm{DS}} = 0.5$ V. Importantly, V_{Th} is defined using the constant current method, by setting $V_{\mathrm{GS}} = V_{\mathrm{Th}}$ when $I_{\mathrm{DS}} = 10^{-7}$ A. It is observed that the ΔV_{Th}-V_{GS} characteristics show an excellent match with the experimental results at $V_{\mathrm{DS}} = 0.5$ V [98] . This proves that our simulation accurately captures the essential physics of interface trap charges during the charging and

discharging processes that occur during the program and erase pulses, respectively.

5.3 Non-Volatile Characteristics of NW-CTT

Fig. 5.3(a) illustrates the I_{DS}-V_{GS} characteristics of NW-CTT under PVRS, with a sweep rate of around 2 V/μs, for $N_{it} = 1 \times 10^{14}$cm^{-3}, $N_{it} = 1 \times 10^{16}$cm^{-3}, and $N_{it} = 1 \times 10^{17}$cm^{-3}. The NW-CTT exhibits a significant shift in sub-threshold current when the programming (PRS) and erasing (ERS) operations are performed by applying +2 V and -2 V, respectively. The memory window is observed to be around 0.2 V, 0.7 V, and 1 V for $N_{it} = 1 \times 10^{14}$ cm^{-3}, $N_{it} = 1 \times 10^{16}$ cm^{-3}, and $N_{it} = 1 \times 10^{17}$ cm^{-3}, respectively, at $V_{DS} = 0.5$ V. The ΔV_{Th} shift in NW-CTT is significantly enhanced compared to their Fin-FET counterparts [24, 98]. A higher ΔV_{Th} in NW-CTT is attributed to the improved charge trapping and de-trapping effects during PRS and ERS, respectively.

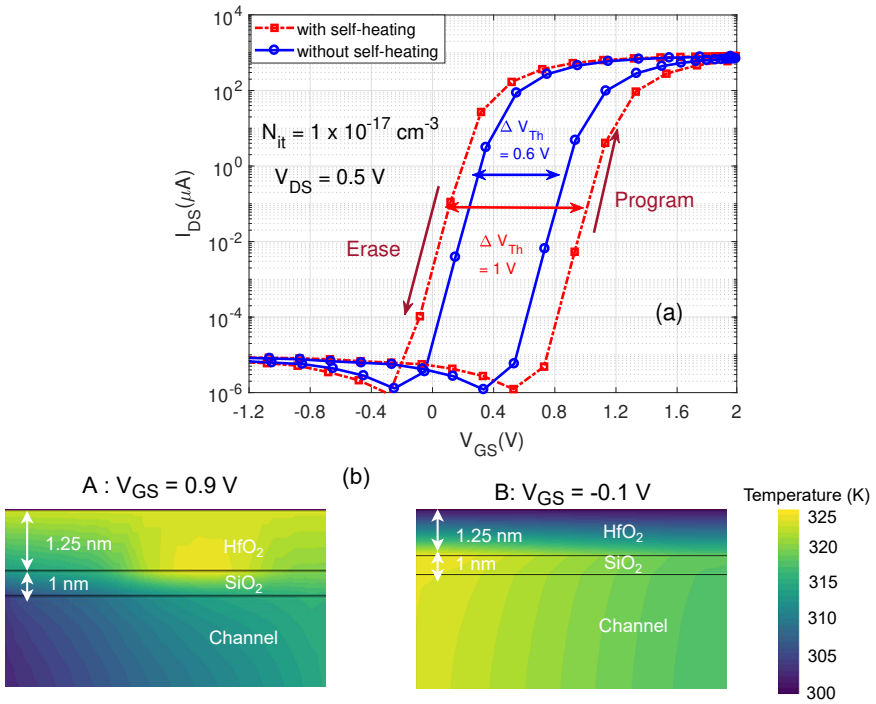

Figure 5.4: Effect of self-heating in non-volatile memory operation: (a) I_{DS}-V_{GS} with and without hydrodynamic model, and (b) 2-D temperature profile at $V_{GS} = 0.9$ V (state A) and $V_{GS} = -0.1$ V (state B) at the $N_{it} = 1 \times 10^{17}$ cm^{-3} for the voltage sweep of 2 V/μs at $V_{DS} = 0.5$ V.

To better understand ΔV_{Th} modulation in NW-CTT, Fig. 5.3(b) displays the electron interface charge profile across the channel-oxide interface for the four bias points, marked in Fig. 5.3(a). At positive V_{GS}, the electron interface charge in the CTL increases because the channel electrons tunnel through IFL and traps in the CTL layer, [see the state A]. As positive V_{GS} cycle increases further, electrons accumulate near the interface due to

enhanced tunneling, increasing the electron interface charge in the CTL layer [see state B]. This leads to considerable positive shift in V_{Th} [see Fig. 5.3(a)]. When the negative gate pulse is applied in state C, electrons migrate back from the CTL to the channel. The interface charges are completely de-trapped at state D, which results in a decrement in the electron interface charge near the interface. This provides a significant negative shift in V_{Th} [see Fig. 5.3(a)]. Therefore, the positive and negative V_{Th} shift exhibits a high memory window, which promises improved non-volatile memory operations with HfO_2-based NW-CTT through interface states.

Fig. 5.4(a) illustrates the non-volatile memory characteristics of NW-CTT with and without considering the self-heating effect for $N_{\mathrm{it}} = 1 \times 10^{17}\mathrm{cm}^{-3}$. It is observed that the ΔV_{Th} is observed approximately 1 V with the self-heating effect, whereas it is found to be around 0.6 V without considering the self-heating effect. From Fig. 5.4(b), it is found that the incorporation of self-heating effect captures the elevation in temperature across the device. This enhancement is attributed to the increment in capture and emission times of interface trapped charges [19], allowing for rapid modulation of charge density with the gate voltage pulse. Therefore, considering the self-heating effects is crucial for accurately describing the charge trapping and de-trapping phenomena in CTT.

5.4 Synaptic Characteristics of NW-CTT

Fig. 5.5(a) shows the schematic representation of a biological synapse using NW-CTT, where the gate and drain terminals serve as the pre-neuron and post-neuron, respectively. An important feature of synapses is weight-dependent plasticity, a characteristic found in biological synapses that may be interesting to replicate in artificial systems. For long-term potentiation (LTP) and long-term depression (LTD) analysis, we apply 106 sets of square voltage pulse trains with a duration of 300 ns. Among these, 53 sets have an incremental amplitude of 0.03 V for LTD, and the remaining 53 sets have an incremental amplitude of -0.03 V for LTP. The V_{DS} terminal bias is considered to be around 0.5 V. The conductance [G(μS)] is computed by taking the derivative of the obtained drain current with the applied pulse voltage. Fig. 5.5(b) shows that the conductance of NW-CTT exhibits linearly increment and decrement for LTP and LTD, respectively. This linear behavior is attributed to the constant rate of electron trapping and de-trapping with positive and negative gate pulses, respectively. The dynamic range for conductance modulation is approximately 12.4 for both LTP and LTD. Meanwhile, the non-linearity is calculated to be 0.08 for LTP and 0.048 for LTD, utilizing the formula

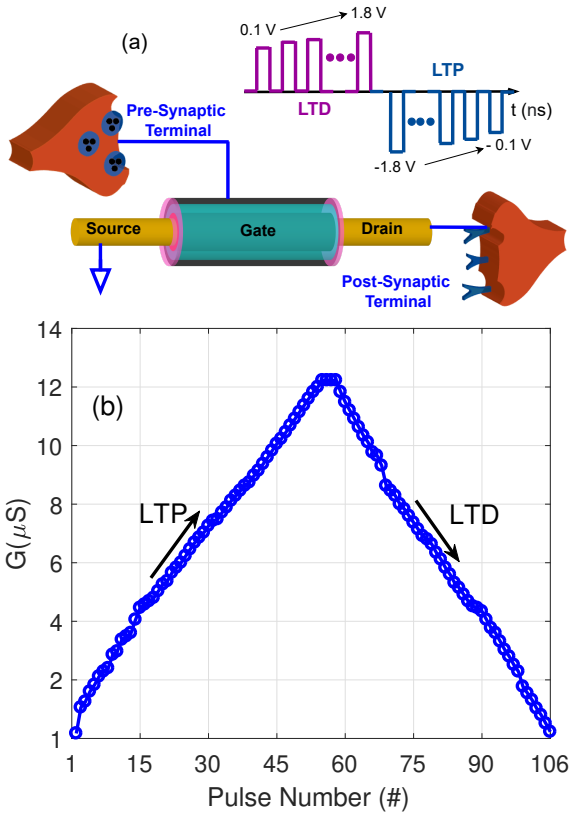

Figure 5.5: Biological synapse for neuromorphic applications: (a) schematic of NW-CTT-based artificial synapse, and (b) conductance as a function of pulse number, indicating the long-term potentiation (LTP) and long-term depression (LTD) behavior of NW-CTT.

provided in [105], which prove to be nearly linear conductance modulation. These findings suggest that the near-linear behavior of conductance modulation with NW-CTT holds promise for enhanced multistate weight update capability.

A multilayer perceptron artificial neural network is designed using NeuroSIM simulator to assess the learning capabilities of the NW-CTT-based synaptic device. Fig. 5.6(a) shows neural network architecture, which comprises an input layer, a hidden layer, and an output layer with the size of 784, 100, and 10 neurons, respectively. These neurons are connected through the NW-CTT-based synaptic crossbar array, as shown in Fig. 5.6(b). The input consists MNIST dataset, which includes 28 × 28 pixels of handwritten digits ranging from "0" to "9". The image undergoes normalization of pixel intensities within the range of 0 and 1. Each normalized pixel is then transformed into a column matrix with 784 elements, which are subsequently fed into the input layer of the neural network. Further, the MNIST dataset consists of 60,000 inference and 10,000 testing handwritten digit images. The conductance values obtained from the NW-CTT are employed as the synaptic weights, which connect three-layer neurons. During the

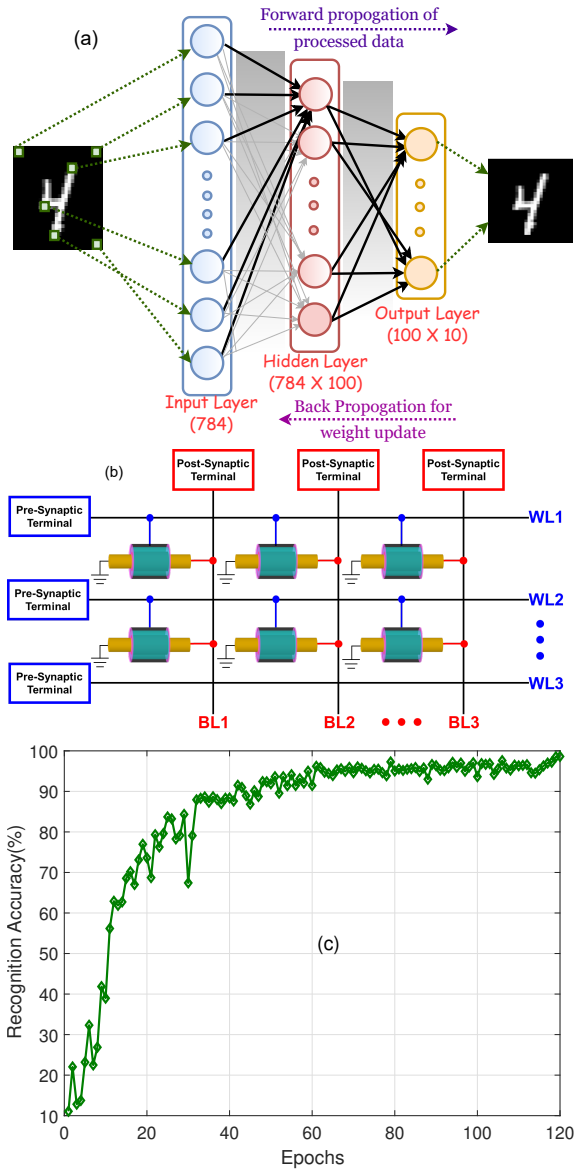

Figure 5.6: Pattern recognition accuracy: (a) schematic of the multilayer perceptron neural network, (b) crossbar array architecture with NW-CTT as the synaptic element that is utilized within the input, hidden, and output layers, and (c) MNIST digit recognition accuracy with the number of training epoch.

inference stage, the neural network computes the loss, which is a difference between the expected and calculated errors, and propagates backward to the individual layers. The rectified linear unit (ReLU) activation and Adam optimizer are incorporated to account for non-linearity and weight updates, respectively. After that, our simulation computes the weight gradients and optimizes the parameters accordingly. Upon completion of the inference stage, the testing images are feeded as inputs to the input layer of the neural network. The output layer then compares the network's predictions with the target output, thereby providing the recognition accuracy of the NW-CTT-based system for MNIST digit classification. Fig. 5.6(c) reveals that the artificial neural network achieves a recognition

accuracy of around 94.7% using NW-CTT after 100 epochs due to superior dynamic range and near-linear conductance modulation. This shows that NW-CTT exhibits excellent capability in recognizing all ten input digits and distinguishing various details within each digit.

5.4.1 Influence of Nanowire Diameter

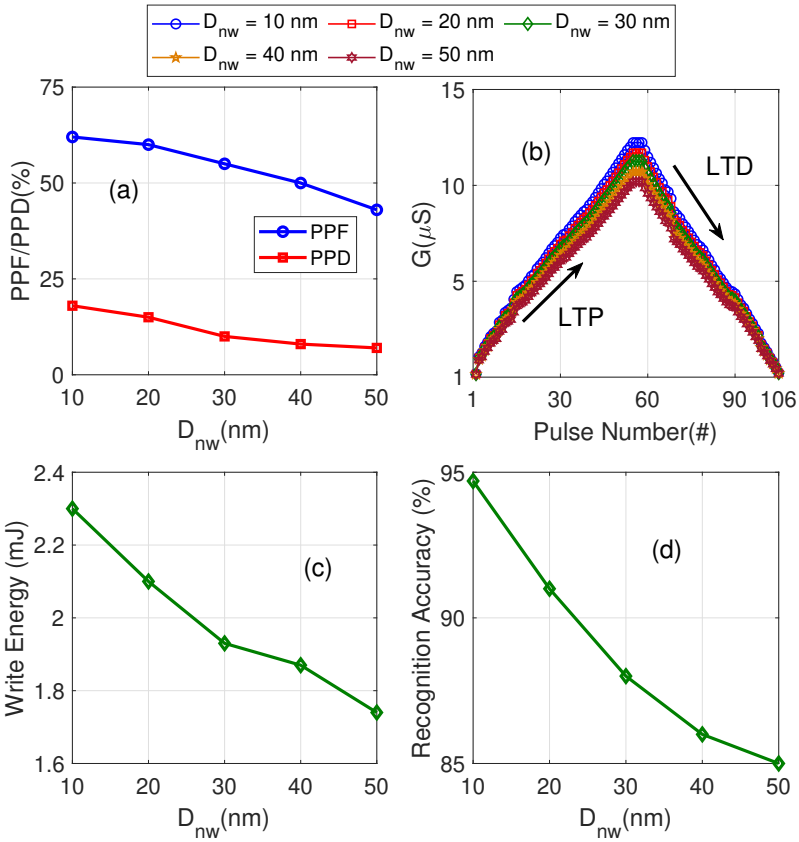

Figure 5.7: Impact of nanowire diameter (D_{nw}) on synaptic functionality at $V_{DS} = 0.5$ V: (a) paired-pulse facilitation (PPF) and paired-pulse depression (PPD) indexes, (b) LTP and LTD with pulse number, (c) write energy consumption, and (d) recognition accuracy after the 100^{th} epoch of the MNIST dataset as a function of D_{nw}.

We now explore the synaptic behavior of NW-CTT with variation in the nanowire diameter (D_{nw}) as achieving uniformity and consistency in nanowire dimensions is still a crucial factor [106]. The D_{nw} is here varied in the range of 10 nm to 50 nm by keeping other parameters fixed. Fig. 5.7(a) shows paired-pulse facilitation (PPF) and paired-pulse depression (PPD) index, which demonstrates the short-term memory capability of the artificial synapse. The PPF and PPD are computed as 100% × ((A_2 - A_1)/ A_1), where A_1 and A_2 are the amplitude of the first and second output current for the two consecutive identical pulses on the pre-neuron where |0.1| V amplitude pulse is used in this work. In particular, the increment in PPF and decrement in PPD index represent the excitatory and

inhibitory neurotransmitter release, respectively. The PPF and PPD for $D_{nw} = 10$ nm are observed to be approximately 68% and 18%, respectively. This notable difference in PPF and PPD is attributed to the rapid modulation in current resulting from the enhanced charge trapping effect. It is also observed that the PPF and PPD decrease significantly with increasing the D_{nw}. This is due to the considerable reduction in the charge-trapping and de-trapping effects in the drain-to-source current for larger diameters. Fig. 5.7(b) shows that the dynamic range of $D_{nw} = 50$ nm for LTP and LTD is attained around 1.34× and 1.4× lower than $D_{nw} = 10$ nm, respectively. Further, the non-linearity of $D_{nw} = 50$ nm for LTP and LTD is found around 1.3× and 1.04× lower than $D_{nw} = 10$ nm, respectively. The reason for a considerable decrement in dynamic range and non-linearity is that a larger D_{nw} considerably decreases the inversion charge in the channel region, which decreases the interface charge density.

Fig. 5.7(c) and Fig. 5.7(d) demonstrate the impact of D_{nw} on the write energy consumption and recognition accuracy after the 100^{th} epoch, respectively. The write energy consumption of neural network is computed by $E_{\text{cell}} = G{V_{\text{W}}}^2 N T_{\text{pulse}}$, where G represents the conductance values, V_{W} represents the write voltage, N signifies the number of applied write pulses, and T_{pulse} indicate the pulse width. It is observed that the write energy consumption and recognition accuracy decreases with increasing the D_{nw}. Notably, the write energy consumption and recognition accuracy for $D_{nw} = 50$ nm are found around 1.75 mJ and 85%, respectively, which are nearly 1.34× and 1.12× lower than $D_{nw} = 10$ nm, respectively. This considerable reduction in recognition accuracy and energy efficiency is due to a considerable increment in non-linearity and decrement in dynamic range for both LTP and LTD. Therefore, a larger nanowire diameter might improve energy efficiency, but it causes a significant reduction in recognition accuracy.

5.4.2 Influence of Thickness of Charge Trap Layer

In this section, we examine the synaptic behavior of NW-CTT with variations in the thickness of the CTL (t_{CTL}) layer, which is a critical parameter for enhancing the charge retention capability. The t_{CTL} is here varied in the range of 1 nm to 5 nm by keeping other parameters constant. Fig. 5.8(a) shows that the PPD and PPF decrease with increasing the t_{CTL}. This is due to a significant reduction in the drain-to-source current modulation for the same interface trap charges. Fig. 5.8(b) reveals that NW-CTT with thicker t_{CTL} exhibits lower dynamic range and higher non-linearity for both LTP and LTD compared to thinner counterparts. Additionally, Fig. 5.8(c) and Fig. 5.8(d) show that the write energy consumption drops from 2.3 mJ to 1.7 mJ, while the recognition accuracy degrades from

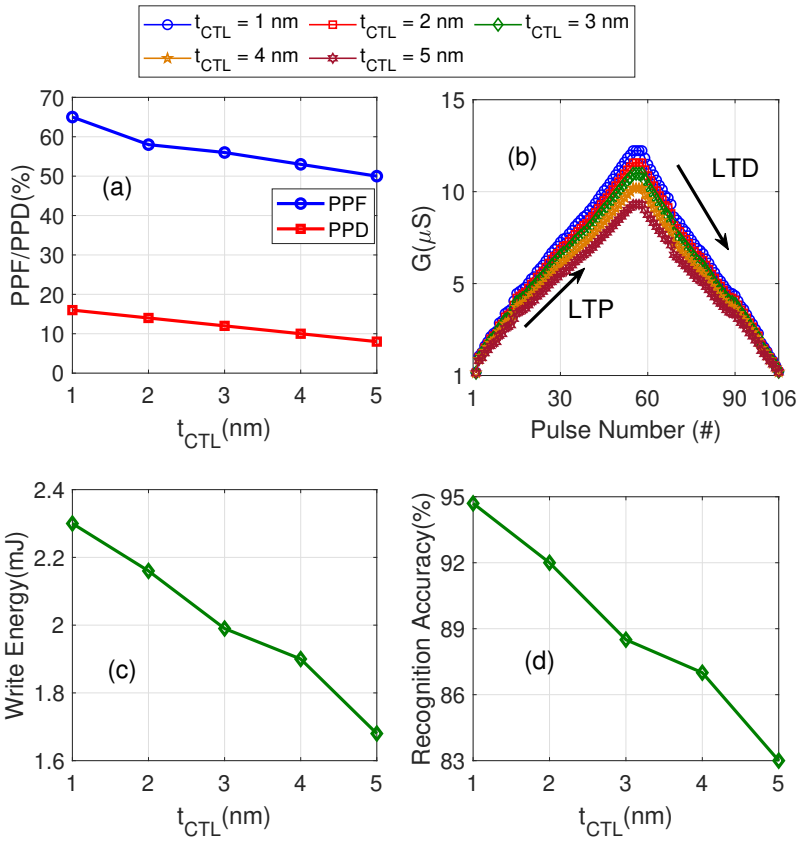

Figure 5.8: Impact of the charge trap layer thickness (t_{CTL}) on synaptic behavior at V_{DS} = 0.5 V: (a) PPF and PPD indexes, and (b) LTP and LTD with pulse number, (c) write energy consumption, and (d) recognition accuracy after the 100^{th} epoch of MNIST dataset as a function of CTL thickness.

94.7% to 83% when the t_{CTL} is scaled up from 1 nm to 5 nm. This is due to the significant enhancement in the non-linearity in conductance modulation. Therefore, it is evident that the optimal choice of t_{CTL} could offer sufficient dynamic range and near-linear behavior, leading to high recognition accuracy for neuromorphic applications.

5.4.3 Influence of Gate Length

Fig. 5.9 shows the synaptic characteristics and neural network performance of NW-CTT as a function of the gate length (L_g) at V_{DS} = 0.5 V. The L_g is varied in the range of 10 nm to 22 nm according to the IRDS 2022 projection for 1 nm to 5 nm technology nodes [102]. As observed in Fig. 5.9(a), PPF and PPD increase with decreasing L_g due to a significant enhancement in gate efficiency. The PPF and PPD are observed to be approximately 78% and 25%, respectively, at L_g = 10 nm, which indicates superior temporal detection capability. Fig. 5.9(b) demonstrates that the conductance has a higher dynamic range and is modulated more linearly with pulse number in LTP and LTD as L_g decreases. The reduction in L_g increases the electric field in the channel

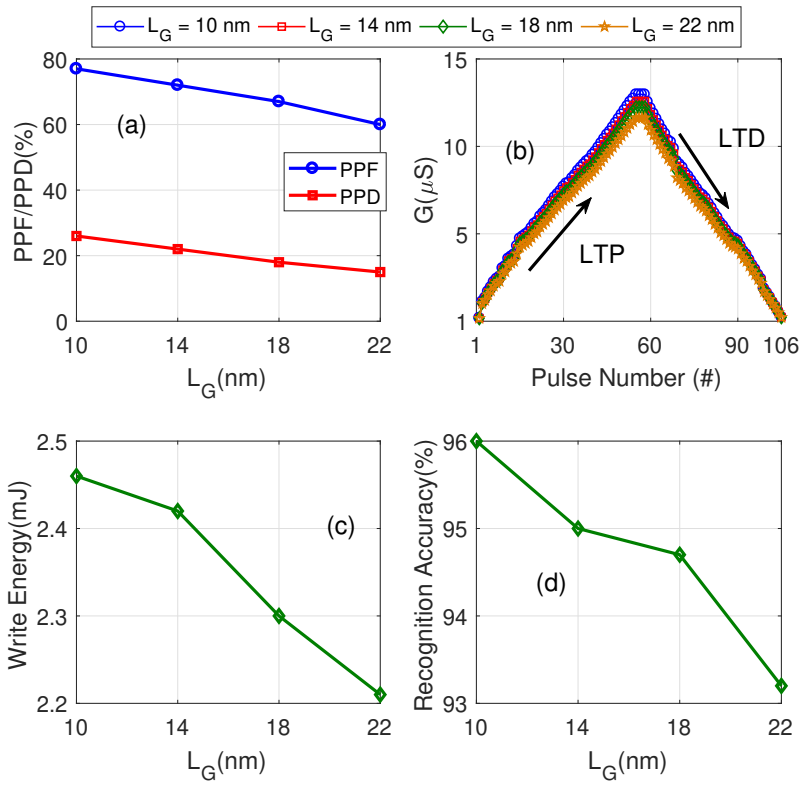

Figure 5.9: Impact of the gate length (L_g) on synaptic behavior at $V_{\mathrm{DS}} = 0.5$ V: (a) PPF and PPD indexes, and (b) LTP and LTD with pulse number, (c) write energy consumption, and (d) recognition accuracy after the 100^{th} epoch of MNIST dataset as a function of gate length.

region, which lowers the potential barrier for inversion charges. This enhances the charge trapping/de-trapping phenomenon of electrons to/from spatially distributed interface trap sites.

It is observed from Fig. 5.9(c) that the write energy consumption increases marginally from 2.2 mJ to 2.47 mJ as L_g decreases from 22 nm to 10 nm due to an enhancement in I_{DS}. Additionally, the recognition accuracy improves from 93.2% to 96% when the gate length is scaled down from 22 nm to 10 nm, as shown in Fig. 5.9(d). Therefore, NW-CTT with a shorter gate length proves to be a more efficient synaptic device for offering a high dynamic range and more linear conductance modulation, which promises higher recognition accuracy in neural networks.

5.4.4 Influence of Metal Gate Work Function

Fig. 5.10 shows the impact of the metal gate work function on synaptic behavior and crossbar array performance of NW-CTT at $V_{\mathrm{DS}} = 0.5$ V. Here the selected gate work functions represent the following metals: 3.1 eV (Yttrium), 4.28 eV (Aluminium), 4.35 eV (Titanium nitride), 4.7 eV (Copper), and 5.1 eV (Gold). Fig. 5.10(a) shows that

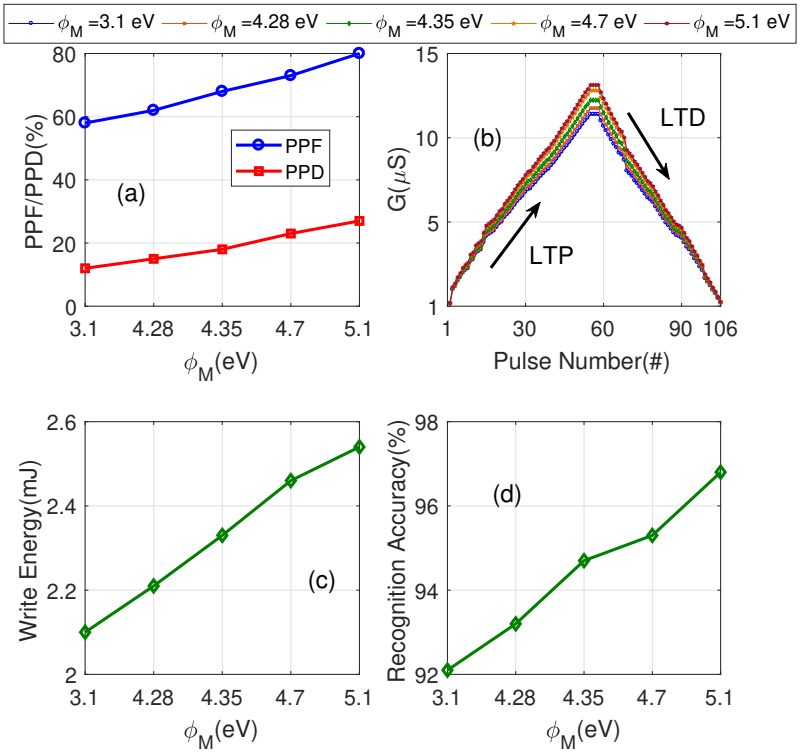

Figure 5.10: Impact of the gate work function (ϕ_M) on synaptic behavior at $V_{DS} = 0.5$ V: (a) PPF and PPD indexes, and (b) LTP and LTD with pulse number, (c) write energy consumption, and (d) recognition accuracy after the 100^{th} epoch of MNIST dataset as a function of gate metal work function.

PPD and PPF increase with increasing the ϕ_M. This is because a higher ϕ_M significantly enhances the inversion charge density in the channel region, which considerably increases the charge trapping/de-trapping into/from the CTL layer. Moreover, the higher PPF and PPD indexes at $\phi_M = 5.1$ eV highlight the substantial charge buildup capability of NW-CTT.

It is observed from Fig. 5.10(b) that dynamic range and linearity in conductance modulation improve with increasing ϕ_M due to the enhancement in drain-to-source current modulation efficiency with increasing the interface trap states. Moreover, the non-linearity in LTP and LTD remains in a narrow range of 0.08-0.09 and 0.048-0.051, respectively, with a dynamic range of 12.4-13.5. Thus, the improvement in synaptic characteristics of NW-CTT suggests that a higher ϕ_M could increase the multi-bit storage capability of the device.

Fig. 5.10(c) shows that the write energy consumption exhibits a marginal increment of around 1.21×, which increases from approximately 2.1 mJ to 2.55 mJ when ϕ_M rises from 3.1 eV to 5.1 eV. From Fig. 5.10(c), it is seen that recognition accuracy significantly enhances from 92% to 96.8% with increasing ϕ_M from 3.1 eV to 5.1 eV. This signifies that even a marginal improvement in dynamic range and linearity in conductance modulation

can significantly enhance recognition accuracy, while energy consumption exhibits only a slight increment. Therefore, tailoring the ϕ_M could be a suitable choice for attaining superior neural network performance with NW-CTT.

5.5 Performance Benchmarking

Table 5.1: Comparison of performance metrics of NW-CTT with the state-of-art non-volatile memory devices.

Device	**Switching Mechanism**	**STM**	**Voltage[V]**	**Dynamic Range**	**States/Device**	**Energy[fJ]†**	**RA**(%)
MgO [97]	Stochastic	No	1	14	NA	1×10^7	57
In_2Se_3[96]	Ferroelectric	No	15	3	113	792×10^8	NA
$Pt/Co/SiO_2$[107]	Ferromagnetic	No	20 mA^+	3	90	3×10^{11}	82.8
GeTe[108]	Phase changing	No	7	8	10	12.1	NA
HfO_x[95]	Resistive	No	0.8	3	40	NA	83
TaO_x[109]	Resistive	No	5	7	40	NA	96.4
QW[110]	Charge Trapping	Yes	7	7	20	0.766	NA
MoS_2[111]	Charge Trapping	Yes	4	NA	300	1×10^4	35.6
Si-Nanosheet-SONOS [100]	Charge Trapping	No	10	2×10^3	40	NA	93.3
Si-FDSOI-CTT [20]	Charge Trapping	No	2.5	150	256	5×10^5	NA
Si-PDSOI-SONOS [112]	Charge Trapping	Yes	2	175	50	4500	NA
Si-Nanowire-SONOS [44]	Charge Trapping	Yes	4	NA	NA	0.02	NA
Si-FDSOI-CTT[21]	Charge Trapping	No	2	NA	NA	14.8 mW*	95.7
This work	**Charge Trapping**	**Yes**	**1.8**	**12.4**	**53**	**0.13**	**94.7**

STM: Short-Term Memory (PPF and PPD); RA: Recognition Accuracy after 100^{th} epoch; QW: Quantum-Well; NA: Not Available; †: Device Switching Energy; *: power consumption; $^+$: current supply.

Table 5.1 compares our HfO_2-based NW-CTT with state-of-the-art synaptic devices [20], [21], [44], [95], [96], [97], [100], [107], [108], [109], [110], [111], [112] in terms of key device and neural network performance metrics. Since most of the emerging non-volatile memories have computed the device switching energy, we here present the device switching energy of HfO_2-based NW-CTT, that is calculated as $E = I_{\text{DS}} \times V_{\text{applied}} \times t_{\text{switching}}$, where I_{DS}, V_{applied}, and $t_{\text{switching}}$ represent the drain-to-source current, applied pulse bias, and switching time, respectively. It is evident that the emerging non-volatile memories, such as MgO-based MTJ [97], In_2Se_3-based FeFET [96], HfO_x-based RRAM [95], TaO_x-based RRAM [109], Si-Nanosheet-SONOS [100], Si-FDSOI-CTT [21], Si-FDSOI-CTT [20], and GeTe-based PCM [108], primarily demonstrate long-term memory characteristics over short-term memory, which often requires large operating voltages. Interestingly, the proposed Si NW-CTT offers both short-term and long-term memory with relatively lower operating voltage. NW-CTT not only offers significantly lower device switching energy of 0.13 fJ, but also exhibits superior recognition accuracy (94.7%) compared with

MoS_2-CTT [111], MgO-based MTJ [97], and HfO_x-based RRAM [95], $Pt/Co/SiO_2$-based ferromagnetic [107]. Therefore, the proposed HfO_2-based NW-CTT holds promise to develop high-density non-volatile memory and synaptic crossbar array with superior learning accuracy and energy efficiency.

5.6 Summary

Using a fully calibrated TCAD simulation, this chapter presented a comprehensive performance analysis of HfO_2-based NW-CTT to mimic the multilevel dynamics of biological synapse. The charge trapping and de-trapping of interface states has demonstrated the memory window of around 1 V between programming and erase pulse when the $N_{it} = 1 \times 10^{17}$ cm^{-3} present in HfO_2 layer. Further, NW-CTT exhibited asymmetric conductance modulation of LTD and LTP with around non-linearity of around 0.08 and 0.048, respectively. A close to linear conductance modulation with NW-CTT has shown superior recognition accuracy (94.7%) and write energy (2.3 mJ) in $784 \times 100 \times 10$ neural network for handwritten digits. Furthermore, our device design parameter optimization results have provided a valuable guideline for selecting the NW diameter, thickness of CTL, gate length, and metal gate work function to achieve enhanced learning accuracy and energy efficiency. Thus, the proposed NW-CTT closely mimics both short-term and long-term synaptic characteristics, making it suitable for future applications in neuromorphic computing.

Chapter 6

Fully NW-CTT-based Spiking Neural Network with Unsupervised Learning

6.1 Introduction

The cognitive functions of the human brain, including learning and memory, arise from a complex network of approximately one hundred billion neurons interconnected by synapses [89]. Neurons process pre-synaptic input stimuli to generate electrical impulses, while synapses facilitate signal transmission between neighboring neurons. The functionality of these neurons and synapses can be modified based on prior experiences, leading to the reorganization of neural pathways [113]. In biological systems, changes in synaptic weight are influenced by the concentrations of various ionic species, such as Ca^{2+}, Na^{+}, K^{+}, which regulate the release of neurotransmitters from the pre-synaptic to the post-synaptic terminal [114]. Neural synaptic functions, including excitatory/inhibitory post-synaptic current (EPSC/IPSC), pair-pulse facilitation/depression (PPF/PPD), long-term potentiation/depression (LTP/LTD), and spike-timing-dependent plasticity (STDP) are crucial for executing computational tasks and memory functions [44]. Recent studies indicate that neurons are not only involved in information processing but also play a pivotal role in memory formation [115]. Furthermore, neuronal inhibition and the tunability of firing threshold voltage are essential for developing reliable and energy-efficient neural networks [116]. Synaptic plasticity and neuronal plasticity occur simultaneously during significant learning processes, which allows the brain to perform intelligent tasks and participate in effective probabilistic processing. To replicate such cognitive efficiency in artificial neuromorphic systems, it is vital to select the appropriate synaptic and neuronal devices. Thus, it becomes important for creating energy-efficient neuromorphic chips that can mimic biological computation, which thereby requires a deeper investigation into synaptic and neuronal device design and functionality.

In recent years, significant progress has been made in the hardware implementation of artificial neural networks (ANNs) using non-volatile memory devices, such as redox memristors [117], phase-change memristors [108], organic transistors [118], and CMOS-based emulator circuits [119]. However, ANNs typically process information

continuously and synchronously, leading to inefficiencies in power consumption and limited biological realism [120]. Spiking Neural Networks (SNNs) offer solutions to these limitations by simulating neurons that communicate through discrete spikes, enabling event-driven and energy-efficient processing that more closely mirrors the brain's functionality [113]. SNNs also leverage temporal coding, capturing the precise timing of spikes to enhance learning and memory representation [121]. Notably, several CMOS-based neuron and synapse emulators have been developed for SNN implementation, such as Intel Loihi [122], IBM TrueNorth [120], and SynSense chips [123]. These chips support on-chip learning, event-driven processing, offline training, and unsupervised learning algorithms. However, they face scalability, training efficiency, energy consumption, and crossbar limitations as they strive to emulate brain-like computing [124].

To improve area efficiency, alternative SNN architectures have been explored by integrating novel memory and synaptic technologies, such as magnetic random-access memory (MRAM) [125], ferroelectric field-effect transistors (FeFETs) [126], threshold-switching (TS) devices [127], and phase-change memory (PCM) [128]. Despite their potential, these technologies face substantial barriers to commercial viability, particularly in achieving CMOS compatibility due to issues like high processing temperatures, material mismatches, and reliability concerns [95]. Recently, CTT, featuring high-k oxide gates, have emerged as promising synaptic elements due to their full CMOS compatibility and potential for three-dimensional (3D) integration [18, 19]. Recently, the 784 $\times$ 784 synaptic crossbar array using 28 nm bulk CMOS technology has presented 95% accuracy for handwritten digit recognition with the 8-bits/cell [21]. More interestingly, the winner-take-all neural network using 22nm HfO_2-based fully depleted SOI (FDSOI) has presented the exceptional learning capability of CTT as a synapse [20]. However, the implementation of homo-typic CTT-based SNN is still missing. Despite these promising experimental and theoretical developments, the detailed design and development of spiking neural networks (SNNs) using CTT remain largely underexplored.

Several experimental efforts have successfully emulated synaptic behavior using silicon-based CTT for low-power, high-retention in-memory applications [19]. However, few studies have explored the neuronal capability using MOSFET devices [129, 130]. Recently, partially depleted silicon-on-insulator (PD-SOI) MOSFETs have been used to implement leaky integrate-and-fire (LIF) neurons, achieving spiking frequencies in the MHz range with energy consumption as low as $13{\times}10^{-12}$ J/spike [129]. More recently,

bulk Fin-FET have demonstrated even more energy-efficient integration and firing, with an energy consumption of 6.3×10^{-15} J/spike, highlighting the need for low-energy neuron circuit designs [130]. Additionally, silicon-oxide-nitride-oxide-semiconductor (SONOS) devices have demonstrated functioning as both neurons and synapses [115]. However, these CMOS technologies rely on impact ionization to implement neuronal behavior. Moreover, no qualitative studies have been conducted to properly investigate the neuronal behavior of CTT. Therefore, there is a pressing need to explore CTT as a neuron to achieve area and energy efficiency in neuromorphic systems.

NW-CTT, with their highly linear conductance modulation and wide dynamic range, have emerged as promising candidates for achieving multistate operation capabilities, making them ideal for electronic synapses, as discussed in the previous chapter [131]. Furthermore, extending this device to implement artificial neurons by achieving leaky integrate-and-fire (LIF) functionality could pave the way for highly scalable and energy-efficient spiking neural networks that are fully CMOS-compatible. This approach has significant potential for the advancement of neuromorphic computing systems and in-memory processing architectures. Therefore, further exploration into the design and optimization of NW-CTT-based spiking neural networks is critical for realizing low-power, high-performance neuromorphic systems.

In this chapter, we design and investigate a fully NW-CTT-based spiking neural network for digit pattern recognition applications. First, we explore the neuronal capabilities of NW-CTT by designing integrate-and-reset circuits. In the initial performance analysis, we evaluate the neuronal behavior of NW-CTT under various pulse schemes. Subsequently, NW-CTT devices, serving both as neurons and synapses, are co-integrated into a single-layer 15×6 crossbar array for spiking neural network development. The performance of both the device and the crossbar array is thoroughly examined using a fully calibrated three-dimensional TCAD tool. Our studies not only demonstrate the performance advantages of NW-CTT as a neuron but also guide designing a homo-typic, energy-efficient, and area-optimized spiking neural network. The key contributions of this paper are threefold:

- To the best of our knowledge, this work presents the first implementation of a SNN using a calibrated TCAD simulation tool. The NW-CTT is initially modeled using a physics-based approach that includes self-consistent solutions of the 3D Poisson's equation, the Boltzmann transport equation, and the self-heating equation, with corrections for interface trap charges. The synaptic behavior of the NW-CTT is

thoroughly investigated, as reported in our previous work [131], followed by a detailed analysis of its neuron-like functionality. Furthermore, we designed a 15×6 crossbar array utilizing mixed-mode simulations.

- This work explores the ability of the NW-CTT to exhibit neuronal behavior by simulating various neuron firing patterns, including tonic, irregular, adaptive, and mixed modes. Unlike previous studies where non-volatile devices were primarily used as neurons for data storage and recording over extended periods, thereby leading to significantly higher energy consumption [132, 133, 134]. Our study emphasizes the direct integration of spikes in the NW-CTT. This approach reduces energy consumption while enabling more efficient real-time neural activity analysis.

- The co-integration of neurons and synapses using NW-CTT is demonstrated in a single-layer 15 × 6 crossbar array. In previous experimental and simulation studies on neural networks [135, 136], the neurons and synapses typically involved hetero-typic devices, significantly increasing the chip area and energy consumption. While some studies have employed homo-typic CMOS-compatible devices, these often require additional fabrication steps and reduce the pattern recognition accuracy [115]. Our study introduces an area- and energy-efficient integration of homo-typic devices within the crossbar array, achieved without any extra fabrication steps or loss in pattern recognition accuracy at the nanoscale gate length. Additionally, our system demonstrates robust pattern detection capabilities even under noisy conditions and process-voltage-temperature variations.

6.2 Device Geometry & Simulation Methodology

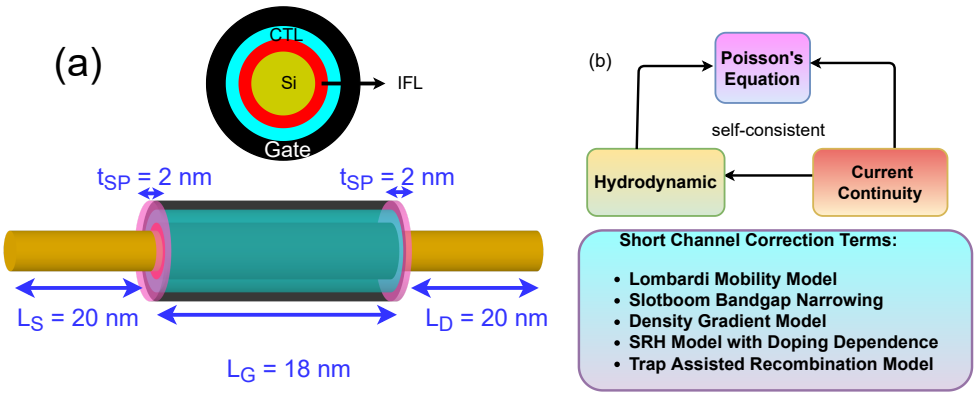

Figure 6.1: Synopsis of modeling methodology and experimental verification: (a) Schematic geometry of NW-CTT at 5 nm technology node (18 nm gate length), and (b) summary of the modeling methodology.

Fig. 6.1(a) shows the schematic of HfO_2-based NW-CTT, which is utilized as an artificial synapse and subsequently modified to function as a neuron. A more detailed discussion of device dimensions and simulation methodology can be found in our previous chapter. Following this, neurons and synapses are integrated to develop SNN in s-device file, and the mixed mode simulation is carried out to simulate the interaction between device-level physical characteristics and circuit-level behavior in an integrated environment.

6.3 Results

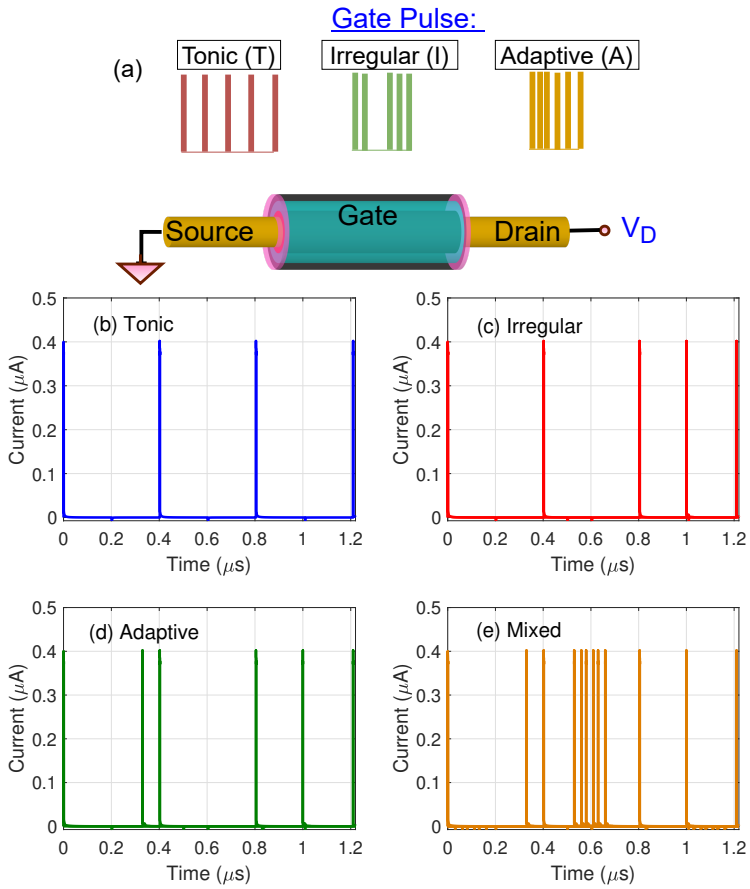

Figure 6.2: (a) Schematic of artificial neuron response with analysis of: (b) Tonic, (c) Irregular, (d) Adaptive, and (e) Mixed firing pulse train at room temperature.

6.3.1 Neuronal Capability of NW-CTT

Fig. 6.2(a) shows the NW-CTT utilized to replicate neuron behavior. To understand the behavior of NW-CTT as a bio-neuron, we initially apply four distinct neural firing patterns: "Tonic," "Irregular," "Adaptive," and "Mixed." Fig. 6.2(a) shows applied input to neuro circuit as rectangular pulses with an amplitude of 0.7 V and a width of 0.1 μs with four different firing patterns. Specifically, the "Tonic" pattern consists of evenly

spaced pulse trains; the "Irregular" pattern consists of spikes firing at irregular intervals; the "Adaptive" pattern shows spikes with gradually increasing intervals; and the "Mixed" pattern is a combination of tonic, irregular, and adaptive firing behaviors.

Fig. 6.2(b)-(e) shows the simulated output current neuron with four input voltage schemes for verifying the LIF functionality. It is evident that output current spikes occur only when pulses are applied. This is mirroring the behavior observed in biological spike trains. The distinct responses to these four different spike train patterns highlight the NW-CTT's capability to process a variety of firing patterns, akin to the neural processing seen in the human brain.

6.3.2 Implementation of STDP with NW-CTT Synapse

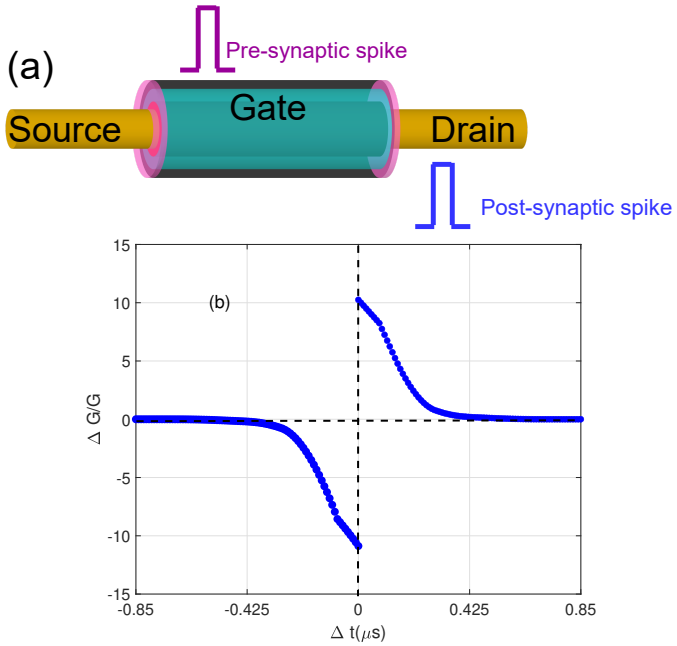

Figure 6.3: Spike timing dependent plasticity (STDP): (a) schematic of NW-CTT-based artificial synapse, and (b) change in conductance state (ΔG/G) as a function of time interval, indicating the long-term potentiation (LTP) and long-term depression (LTD) behavior of NW-CTT.

We next investigate the spike-timing-dependent plasticity (STDP) of NW-CTTs to explore their capability for synaptic weight updates, which depend critically on the relative timing between the spikes of pre-synaptic and post-synaptic neurons. When the pre-synaptic neuron fires before the post-synaptic neuron within a specific time window, the synaptic weight between the two neurons is strengthened, resulting in long-term potentiation (LTP). Conversely, if the post-synaptic neuron fires before the pre-synaptic neuron, the synaptic weight is weakened, leading to long-term depression (LTD).

To implement STDP, we applied pre-synaptic and post-synaptic pulses at the gate

and drain terminals, respectively. Fig. 6.3(a) shows that 0.7 V and -0.7 V amplitudes are applied for the pre-synaptic and post-synaptic pulses, respectively, with a pulse width of 0.1 μs. The different pulse time intervals (Δt) are chosen to achieve LTP and LTD. Fig. 6.3(b) shows the change in the conductance of NW-CTT as a function of the time difference between the pre-synaptic and post-synaptic spikes (Δt). It is observed that when Δt is lower than a positive threshold ($\Delta t < t_{\mathrm{maxpot}}$), it leads to long-term potentiation (LTP), which strengthens the synaptic connection. Conversely, when the post-synaptic spikes occur before the pre-synaptic spikes, and the delay (Δt) is less than t_{maxdep}, long-term depression (LTD) is induced, which weakens the synaptic connection.

According to the Hebbian learning rule, an increment in synaptic weight increases the excitability of post-neurons. To prevent excessive neuronal excitability, synaptic weight potentiation must reach a saturation point. As shown in Fig. 6.3(b), the change in conductance reaches saturation behavior under a sequence of positive and negative pulses with varying voltage amplitudes is evident. These findings demonstrate that the device successfully mimics the long-term potentiation and depression functions of biological synapses.

6.3.3 Implementation of Spiking Neural Network for Pattern Recognition

Fig. 6.4 shows the single-layer neural network, which utilizes 15×6 SNN for classifying grayscale input images, particularly focusing on six digital digits ("0" to "5"). Each digit consists of 5×3 grayscale pixels. The pixel intensities of these grayscale images are encoded into 15 input voltage vectors. These 15 input voltages are fed into the SNN through 15 input neurons, while 6 output neurons correspond to the 6 output digits. Each synaptic crossbar column is dedicated to one of the six digits. Consequently, the network has 90 synaptic elements, determined by the number of input and output neurons. Notably, the grayscale pixels are represented by four input voltage levels: black, dark gray, light gray, and white pixels corresponding to input voltages of 1 V, 0.8 V, 0.6 V, and 0.4 V, respectively. These voltages are applied to the pre-synaptic neurons. The pre-synaptic neuron circuitry consists of a series combination of an NW-CTT and an output resistor (R_{out}). The NW-CTT integrates and generates the spikes, whereas the output resistor converts current into voltage, which is then applied to the system. Further, the output of the pre-synaptic and post-synaptic neuron ($\mathrm{V}_{in,synapse}$) is applied to the NW-CTT-based synaptic crossbar array. The crossbar array consists of CTT between horizontal word lines (WLs) and vertical bit lines (BLs).

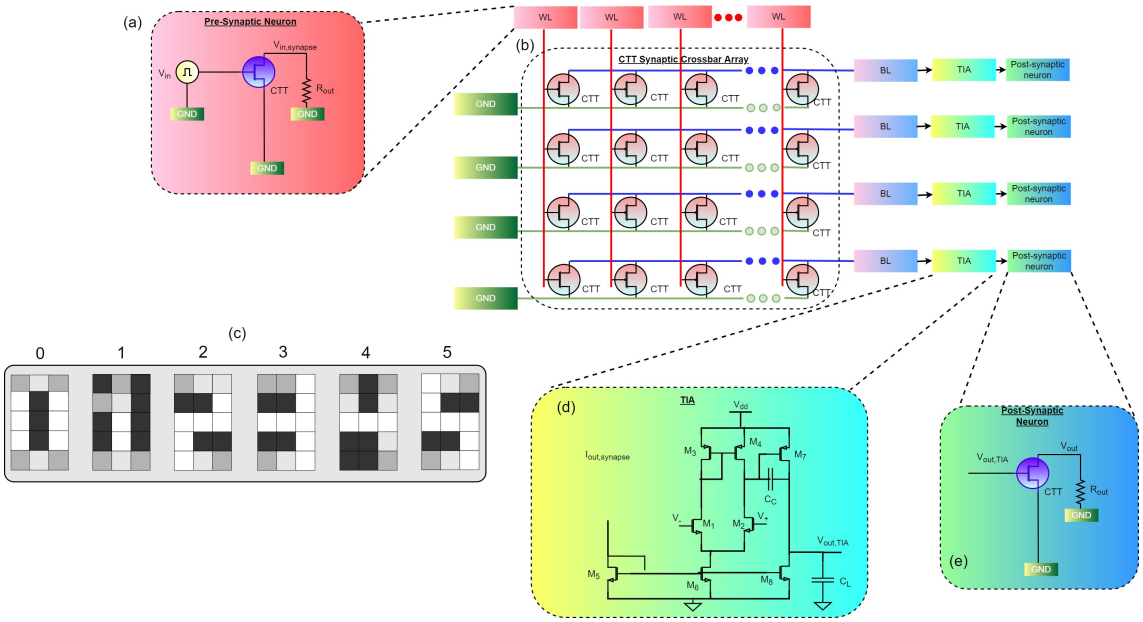

Figure 6.4: The proposed NW-CTT based spiking neural network architecture consisting of: (a) 15 input pre-synaptic neurons, (b) 15×6 synaptic crossbar array, (c) input patterns of six digit, (d) 2 stage operational trans-impedance amplifier, and (e) 6 output post-synaptic neurons.

The rate-encoded spike trains for each pixel are applied to NW-CTT to implement the potentiation and depression mechanisms. The conductance states resulting from these mechanisms are stored in the NW-CTT and used to evaluate its pattern recognition capabilities. Further, a two-stage operational trans-impedance amplifier (TIA) is selected at the output wordline (WL) of the synaptic crossbar array that converts the weighted sum of the output current from the 15×6 crossbar array (CPA) into a voltage. The output of TIA reflects the result of the vector-matrix multiplication (VMM) for the post-synaptic neuron. The post-synaptic neuron then generates spikes based on the input voltage applied to the NW-CTT. To ensure only one output neuron fires at a time, a winner-take-all strategy is employed, allowing the winning neuron to inhibit the others, thereby identifying the recognized pattern.

Fig. 6.5 shows the unique output of post-synaptic neuronal current spikes for six digital digits ("0" to "5"). It observed that digit "0" shows the least spikes, whereas digit "1" presents the highest number. The reason for this behavior is that digit "0" consists of the least number of black pixels, whereas digit "1" consists of a maximum number of black pixels. These black pixels correspond to maximum V_{GS}, which leads to maximum conductance state values, as shown in Fig. 6.4. Moreover, digit "2", "3", "4" and "5" presents 5, 7, 8 and 3 spikes, respectively. Therefore, unique spikes, depending upon the input pattern, could be achieved through NW-CTT based spiking neural network.

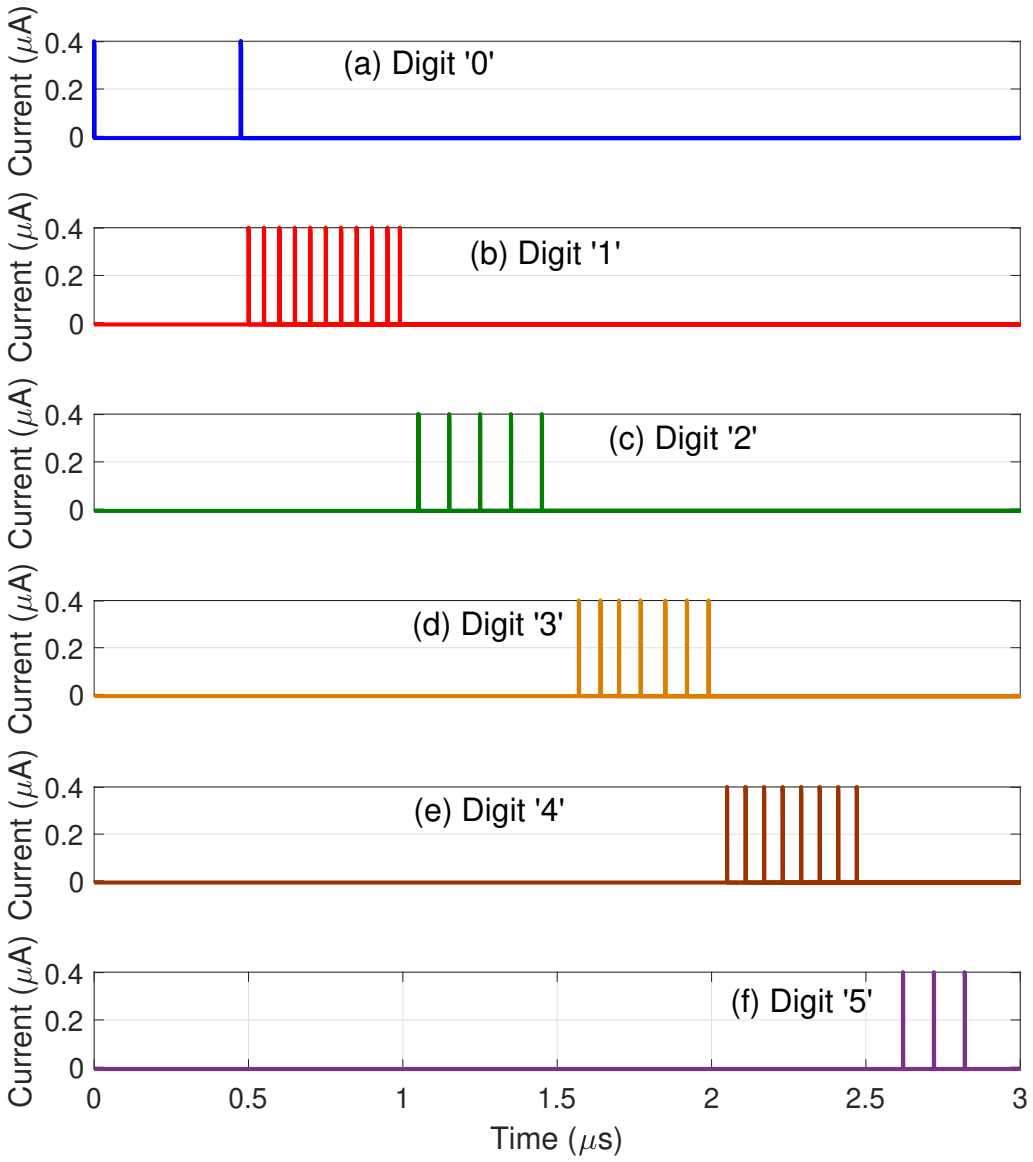

Figure 6.5: Response of firing output neuron for digits: (a) "0", (b) "1", (c) "2", (d) "3", (e) "4" and (f) "5" at room temperature.

6.3.4 Energy Consumption for Each Digit Recognition

Fig. 6.6 presents the energy consumption of SNN for the six digital digits. The energy consumption is calculated as the product of current, voltage, and the number of spikes. It is found that digit "1" exhibits a maximum energy consumption of 0.308 pJ due to the maximum number of spikes in neuron output. However, digit "0" presents the least energy consumption of 0.056 pJ. The energy consumption behavior of digital digits aligns with the number of output spikes for each digit, as shown in Fig. 6.5. Moreover, digit "1" exhibits 5.5×, 2.2×, 1.57×, 1.37×, and 3.67× higher energy consumption than "0", "2", "3", "4" and "5", respectively. Interestingly, our NW-CTT as a synapse and neuron could be a potential candidate for implementing a spiking neuron network as it demonstrates

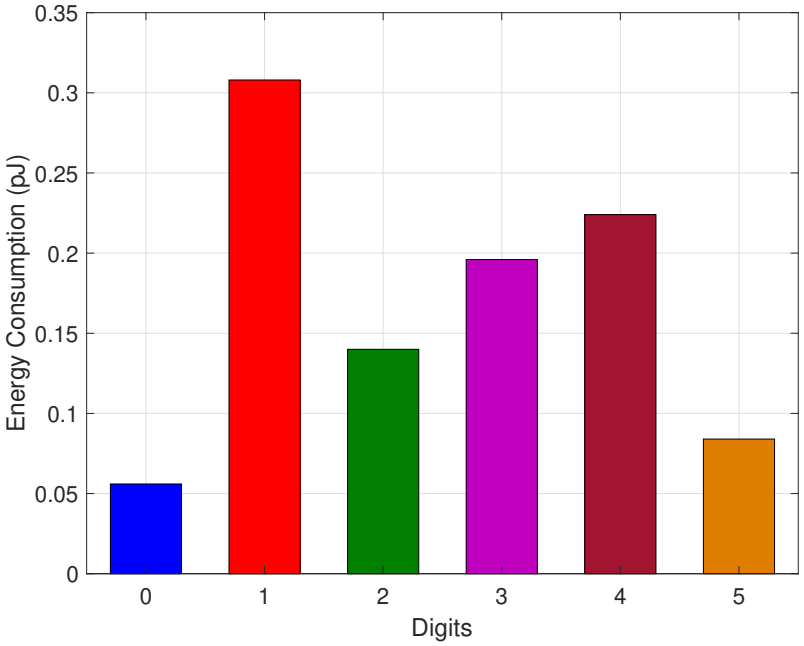

Figure 6.6: Energy consumption for six digits "0" -"5" at room temperature.

significantly lower energy than existing CTT devices as a neuron and synapse [129, 130].

Table 6.1: Comparison of performance metrics of NW-CTT-based spiking neural networks with the state-of-art.

Neuron Type	**Neuron Circuit**	**Synapse**	**Energy/spike (Neuron Circuit)**	**Reference**
LIF	CMOS Analog, mixed signal	CMOS	10 nW †	Indiveri *et al.* [137]
Multiply-accumulate	CMOS analog, mixed-signal	CMOS	125 nW †	Amravati *et al.* [138]
LIF	1 Transistor+ 1 FeFET	FeFET	3.6 nW †	Wang *et al.* [126]
LIF	PCM	PCM	-	Pantazi *et al.* [128]
F	MTJ	CMOS	52.4 nJ	Wu *et al.* [139]
IF	1 SOI-MOSFET+ 2 R+ 2 Op-Amp + 1 p-FET	CMOS	0.3 nJ	Dutta *et al.* [129]
IF	1 capacitor+ 1 NbO_2	CMOS	2.18 pJ	Wang *et al.* [127]
F	1 capacitor+ 1 VO_2	CMOS	0.2 μJ	Jerry *et al.*[140]
LIF	1 **NW-CTT+ 1 R**	**NW-CTT**	**0.028 pJ**	**Our Work**

LIF: leaky integrate fire; IF: integrate fire; F: fire; PCM: phase change memory; FeFET: ferroelectric FET; MTJ: magnetic tunnel junction; R: resistor; †: Power.

6.4 Performance Benchmarking

Table 6.1 compares the performance metrics of our developed NW-CTT-based SNN with the state-of-the-art [126, 127, 128, 129, 137, 138, 139, 140] in terms of neuron and synapse type and energy/power efficiency. It is evident that CMOS-based systems [137, 138] and FeFET-based neuron units [126] demonstrate significantly high power consumption. Moreover, SOI-MOSFET-based neuronal circuits [129] mimic the integrate-and-fire capability of neurons, but they require high operating voltage and a large circuit area. Additionally, threshold-switching-based artificial neurons have shown the lowest power consumption, but they still need high operating voltages [127]. Interestingly, our proposed architecture not only utilizes NW-CTT as both synapse and neuron but also offers energy efficiency with area-saving benefits.

6.5 Conclusion

This chapter presents the implementation of a fully NW-CTT-based spiking neural network (SNN) for recognizing six digital digits. The NW-CTT has demonstrated exceptional performance as an artificial neuron, responding to input stimuli with rate-encoded spiking capabilities. Additionally, the charge-trapping phenomenon in NW-CTT-based neurons regulates the excitatory/inhibitory functions and modulates the firing response based on the threshold voltage. In a 15×6 crossbar array, the NW-CTT serves as both a synapse and a neuron, showcasing superior recognition accuracy and energy efficiency (0.028 pJ/spike). Thus, the proposed NW-CTT-based spiking neural network demonstrates significant advantages and holds great potential for constructing efficient neuromorphic machines

Chapter 7

Conclusion

7.1 Summary

The thesis presents the physical insight into the benefits of GAA devices and their performance exploration for sub-5 nm technology nodes in four topics: (I) single channel multi-gate FETs analysis, including Fin-FET, NS-FET and NW-FET, for RF applications, (II) novel CMOS inverter configurations implementation for design technology co-optimization, (III) demonstration of NW-CTT as an artificial synapse and neuron, and (IV) NW-CTT for attaining a fully CMOS-based spiking neural network. The major contributions and respective conclusions are as follows:

- The initial work involves the exploration of silicon-based multigate devices (Fin-FET, NW-FET, NS-FET) with a focus on finding suitable multigate devices for 5 nm and beyond technology nodes.
  - Among Fin-FET, NW-FET, and NS-FET, NS-FET exhibits excellent current characteristics with a larger voltage gain (32 V/V), transconductance (1.8 mS/μm), output conductance ($10^3\mu$S/μm), cut-off frequency (373 GHz), and maximum oscillation frequency (389 GHz) at 5 nm technology node.
  - Our findings indicate that RF performance metrics of multigate devices have been significantly enhanced by decreasing the channel length and increasing the geometrical parameters, while the voltage gain could be maximized by increasing the channel length, selecting proper surface orientation, and reducing the width and height/thickness of the channel.
  - Our performance analysis identifies the proper directions to optimizations for achieving high-frequency and high-gain RF operations with multigate devices.
- To determine the performance of GAA devices for digital ICs, careful performance analysis and benchmarking of stacked NS-FET-based CMOS inverters with buried power delivery network (BPDN), including complementary field effect transistor (CFET), forksheet (FSH), and conventional stacked nanosheet (s-NSH) are presented using process simulation for sub-5 nm technology node.

  - Our findings reveal that the CFET inverter offers approximately a 3.7% higher operating frequency and a -3.7% lower dynamic power consumption, with a -60.8% smaller area footprint compared to the s-NSH inverter counterpart for the 1 nm technology node.
  - The results show that the device gate capacitance and the fringing field play an essential role in the inverter-level performance degradation that can be minimized by optimizing the p-n separation.
  - Our device performance analysis and benchmarking demonstrate that the CFET inverter delivers optimal and robust switching performance at the ultimate scaling limits.

- With the ever-increasing demand for power and area-efficient memory and logic applications, the device-to-circuit level performance of stacked NS-FET is assessed by developing six transistors static random access memory (6T SRAM) and 32-bit arithmetic logic unit (ALU) using process simulation for sub-5 nm technology node.
  - Our findings reveal that dielectric isolation with 6T CFET and FSH SRAMs significantly enhances read and write margins, and enables faster read and write operations compared to s-NSH SRAM.
  - The 6T CFET SRAM achieves significant power performance improvements, with approximately -12.29% reduction in write power consumption and 38.10% increment in operating frequency compared to s-NSH SRAM for 1 nm technology node. While 6T FSH SRAM exhibits nearly identical read and write abilities compared to CFET SRAM, it offers significant improvements, approximately 31.8% better operating frequency and 12% improved power efficiency over s-NSH SRAM at the 1 nm technology node.
  - Our study indicates that CFET ALU significantly outperforms their FSH and s-NSH counterparts, exhibiting smaller delay and power-delay products with higher throughput.
  - Our device-to-circuit performance analysis and benchmarking show that the CFET inverter configuration is well suited for designing energy-efficient memory and logic integrated circuits in the sub-5 nm regime.

- To develop a CMOS-compatible non-volatile memory, this research present the charge trap transistors (CTT) using silicon nanowire field-effect transistor (NW-FET) using fully calibrated TCAD simulation.

  - The charge trapping and de-trapping of interface states has demonstrated the memory window of around 1 V between programming and erase pulse when the $N_{\text{it}} = 1 \times 10^{17}\ \text{cm}^{-3}$ present in HfO_2 layer.
  - The NW-CTT has attained asymmetric conductance modulation of LTD and LTP with non-linearity of around 0.08 and 0.048, respectively.
  - Our findings indicate that a close to linear conductance modulation with NW-CTT has shown superior recognition accuracy (94.7%) and write energy (2.3 mJ) in $784 \times 100 \times 10$ neural network for handwritten digits.
  - Our device design parameter optimization results have provided a valuable guideline for selecting the NW diameter, thickness of CTL, gate length, and metal gate work function to achieve enhanced learning accuracy and energy efficiency.
  - Our results provide valuable insights into the synaptic behavior of conventional NW-CTTs and offer guidance for further harnessing their weight-update capabilities in neuromorphic computing applications.

- To determine the feasibility and performance of silicon NW-CTT in neuromorphic applications, we have designed a fully CMOS-compatible SNN.
  - The charge-trapping phenomenon in NW-CTT-based neurons effectively regulates the excitatory/inhibitory functions and modulates the firing response based on the threshold voltage.
  - It is evident that NW-CTT-based neurons achieve energy efficiency of around 0.028 pJ, which is the lowest among reported neurons based on CMOS, SOI, FinFET, and threshold-switching technologies [126, 127, 128, 129, 137, 138, 139, 140].
  - Our results show that the integration of NW-CTT in advanced neuroelectronic systems holds the potential to enable energy-efficient neural signal analysis with high spatiotemporal precision, positioning it as a promising candidate for brain-inspired neuromorphic applications.

The TCAD simulation framework developed in this thesis for gate-all-around devices addresses three distinct topics, providing device designers with the ability to design optimized devices that balance power, performance, area, and process considerations. The comprehensive analysis presented here offers valuable insights into the performance

of gate-all-around devices, which could potentially drive significant enhancements in the silicon nanoscale regime. This work not only deepens the understanding of gate-all-around device performance but also sets the stage for future advancements, encouraging further improvements in the power and efficiency of next-generation semiconductor technologies.

7.2 Scope for Future Research

There are mainly four major topics for the future works: (1) the electrothermal analysis for the exploration of the impact of device temperature on the parasitic resistance and capacitance of novel CMOS inverters with buried power delivery networks; (2) the reliability analysis of novel CMOS inverters with power, performance, and area device, circuit and block level metrics; (3) hardware implementation of spiking neural network with charge trap transistors, and (4) exploration of spiking neural networks using complex datasets, such as CIFAR 10, CIFAR 100 and implementing using charge trap transistors.

7.2.1 Electro-thermal Analysis of Novel CMOS Inverters with Buried Power Delivery Network

With the incorporation of metal lines in the buried power delivery network, there is an increase in the Joule heating in the novel CMOS inverter configurations as the device dimensions get reduced. This presence of self-heating might alter the parasitic and, subsequently, the performance characteristics of the inverter configurations [141, 142]. Therefore, the important directions for future researchers here include (i) the incorporation of self-heating for analyzing the effect of temperature on parasitic resistances and capacitances for further power-performance-area optimizations at device, circuit, and block level and (ii) developing a process to simulation framework considering the capturing of temperature effect on Monolithic and Sequential CFET, Forksheet and conventional stacked nanosheet with the scaling of technology node.

7.2.2 Reliability Analysis of Novel CMOS Inverters with Buried Power Delivery Network

The development of CMOS inverter configurations at the device, circuit, and block levels inherently requires a more complex and increased number of process steps. Due to the complex architecture, there is a higher probability of occurrence of defects, electromigration, soft errors, and aging effects, which can significantly impact the reliability of these configurations [142, 143, 144]. To mitigate these reliability challenges, a novel simulation approach is necessary to comprehensively account for these reliability effects. The proposed approach integrates detailed modeling of defect formation,

electromigration pathways, and the potential for soft errors, while also considering aging mechanisms such as Bias Temperature Instability (BTI) and Time-Dependent Dielectric Breakdown (TDDB). The simulation results with incorporating these factors, could help designers to achieve a more robust understanding of the potential failure mechanisms within CMOS inverters. This enhanced insight could enable the optimization of performance, reliability, and lifespan within the design and system technology paradigm, thereby encouraging the development of more resilient CMOS technologies.

7.2.3 Hardware Implementation of Spiking Neural Network with Charge Trap Transistors

Although CTTs have shown promising benefits, their application in SNNs remains under-explored, with limited research focusing on their simulation implementations [44, 100]. Further, their hardware implementations are still missing. To advance CMOS-compatible neuromorphic applications, it is crucial to pursue the hardware implementation of SNNs using charge trap transistors. Such an implementation would bridge the gap between theoretical simulations and practical applications, providing a viable pathway for integrating neuromorphic systems into conventional silicon-based technologies.

7.2.4 Exploration and Implementation of Charge Trap Transistors-based Spiking Neural Networks using Complex Datasets, such as CIFAR 10, CIFAR 100

Charge trap transistor-based spiking neural networks (SNNs) have been explored using simpler datasets like MNIST, which has provided initial insights into their potential for neuromorphic computing [20]. However, the application of these SNNs to more complex datasets, such as CIFAR-10 and CIFAR-100, remains unexplored. To address this gap, it is essential to extend the investigation of charge trap transistor-based SNNs to these challenging datasets. The CIFAR-10 and CIFAR-100 datasets present a higher level of complexity and variability compared to MNIST, making them ideal candidates for testing the scalability and robustness of charge trap transistor-based SNNs. By adapting these networks to process and classify data from CIFAR-10 and CIFAR-100, the research would aim to evaluate the true potential of charge trap transistors in handling more demanding, real-world tasks. This exploration will involve fine-tuning the SNN architecture and optimizing the integration of charge trap transistors to ensure that the networks can efficiently manage the increased computational load. Through this work, the existing gap in the literature on charge trap transistor-based SNNs can be effectively reduced, paving

the way for their application in more advanced neuromorphic systems.

7.2.5 Improvement in Fabrication Complexity and Scalability of NW-CTT for Large Scale Neuromorphic Systems

The fabrication of complex GAA structures presents several challenges [145], [146]. To address these, emerging techniques such as directed self-assembly, atomic layer deposition, and advanced lithography may be employed. Additionally, bottom-up nanowire and nanosheet synthesis along with self-aligned processing methods, can be incorporated to achieve highly precise device architectures with enhanced uniformity and reduced defect densities. Furthermore, a silicon interconnect fabric may be essential for addressing interconnect complexity and thermal management to enable energy-efficient scaling in very large-scale integrated neuromorphic systems.

References

[1] Yuan Taur and Tak H Ning. *Fundamentals of modern VLSI devices*. Cambridge university press, 2021. doi: 10.1017/cbo9781139195065.008.

[2] G. K. Celler and Sorin Cristoloveanu. Frontiers of silicon-on-insulator. *Journal of Applied Physics*, 93(9):4955–4978, May 2003. ISSN 1089-7550. doi: 10.1063/1.1558223.

[3] J-P Colinge. *Silicon-on-insulator technology: materials to VLSI*. Springer Science & Business Media, 2012. doi: 10.1007/978-1-4419-9106-5.

[4] Ali Razavieh, Peter Zeitzoff, and Edward J Nowak. Challenges and limitations of CMOS scaling for FinFET and beyond architectures. *IEEE Transactions on Nanotechnology*, 18:999–1004, 2019. doi: 10.1109/tnano.2019.2942456.

[5] J Ryckaert, MH Na, P Weckx, D Jang, P Schuddinck, B Chehab, S Patli, S Sarkar, O Zografos, R Baert, et al. Enabling sub-5nm CMOS technology scaling thinner and taller! In *2019 IEEE International Electron Devices Meeting (IEDM)*, pages 29–4. IEEE, 2019. doi: 10.1109/iedm19573.2019.8993631.

[6] Uttam Kumar Das and Tarun Kanti Bhattacharyya. Opportunities in Device Scaling for 3-nm Node and Beyond: FinFET Versus GAA-FET Versus UFET. *IEEE Transactions on Electron Devices*, 67(6):2633–2638, 2020. doi: 10.1109/ted.2020.2987139.

[7] Wei Cao, Huiming Bu, Maud Vinet, Min Cao, Shinichi Takagi, Sungwoo Hwang, Tahir Ghani, and Kaustav Banerjee. The future transistors. *Nature*, 620(7974): 501–515, 2023. doi: 10.1038/s41586-023-06145-x.

[8] N Loubet, T Hook, P Montanini, C-W Yeung, S Kanakasabapathy, M Guillom, T Yamashita, J Zhang, X Miao, J Wang, et al. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In *2017 Symposium on VLSI Technology*, pages T230–T231. IEEE, 2017. doi: 10.23919/VLSIT.2017.7998183.

[9] A. Veloso, G. Eneman, T. Huynh-Bao, A. Chasin, E. Simoen, E. Vecchio, K. Devriendt, S. Brus, E. Rosseel, A. Hikavyy, R. Loo, V. Paraschiv, B. T. Chan, D. Radisic, W. Li, J. J. Versluijs, L. Teugels, F. Sebaai, P. Favia, H. Bender, E. Vancoille, J. E. Scheerder, C. Fleischmann, N. Horiguchi, and P. Matagne.

Vertical Nanowire and Nanosheet FETs: Device Features, Novel Schemes for Improved Process Control and Enhanced Mobility, Potential for Faster amp; More Energy Efficient Circuits. In *2019 IEEE International Electron Devices Meeting (IEDM)*, pages 11.1.1–11.1.4, 2019. doi: 10.1109/IEDM19573.2019.8993602.

[10] Ramendra Singh, Kritika Aditya, Anabela Veloso, Bertrand Parvais, and Abhisek Dixit. Experimental evaluation of self-heating and analog/RF FOM in GAA-nanowire FETs. *IEEE Transactions on Electron Devices*, 66(8):3279–3285, 2019. doi: 10.1109/ted.2019.2924439.

[11] S Barraud, B Previtali, C Vizioz, J-M Hartmann, J Sturm, J Lassarre, C Perrot, Ph Rodriguez, V Loup, A Magalhaes-Lucas, et al. 7-levels-stacked nanosheet GAA transistors for high performance computing. In *2020 IEEE Symposium on VLSI Technology*, pages 1–2. IEEE, 2020. doi: 10.1109/vlsitechnology18217.2020.9265025.

[12] Chun-Lin Chu, Shu-Han Hsu, Wei-Yuan Chang, Guang-Li Luo, and Szu-Hung Chen. Stacked SiGe nanosheets p-FET for Sub-3 nm logic applications. *Scientific Reports*, 13(1):9433, 2023. doi: 10.1038/s41598-023-36614-2.

[13] J. Ryckaert, P. Schuddinck, P. Weckx, G. Bouche, B. Vincent, J. Smith, Y. Sherazi, A. Mallik, H. Mertens, S. Demuynck, T. Huynh Bao, A. Veloso, N. Horiguchi, A. Mocuta, D. Mocuta, and J. Boemmels. The Complementary FET (CFET) for CMOS scaling beyond N3. In *2018 IEEE Symposium on VLSI Technology*. IEEE, jun 2018. doi: 10.1109/vlsit.2018.8510618.

[14] P. Weckx, J. Ryckaert, E. Dentoni Litta, D. Yakimets, P. Matagne, P. Schuddinck, D. Jang, B. Chehab, R. Baert, M. Gupta, Y. Oniki, L.-A. Ragnarsson, N. Horiguchi, A. Spessot, and D. Verkest. Novel forksheet device architecture as ultimate logic scaling device towards 2nm. In *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, dec 2019. doi: 10.1109/iedm19573.2019.8993635.

[15] Jaewan Lim, Jinsu Jeong, Junjong Lee, Seunghwan Lee, Sanguk Lee, Yonghwan Ahn, and Rock-Hyun Baek. Investigation of Electrothermal Characteristics in Silicon Forksheet FETs for Sub-3-nm Node. *IEEE Transactions on Electron Devices*, 2023. doi: 10.1109/ted.2023.3326786.

[16] Seung-Geun Jung, Dongwon Jang, Seong-Ji Min, Euyjin Park, and Hyun-Yong Yu. Performance Analysis on Complementary FET (CFET) Relative to Standard CMOS

With Nanosheet FET. *IEEE Journal of the Electron Devices Society*, 10:78–82, 2021. doi: 10.1109/jeds.2021.3136605.

[17] R. Ritzenthaler, H. Mertens, G. Eneman, E. Simoen, E. Bury, P. Eyben, F. M. Bufler, Y. Oniki, B. Briggs, B.T. Chan, A. Hikavyy, G. Mannaert, B. Parvais, A. Chasin, J. Mitard, E. Dentoni Litta, S. Samavedam, and N. Horiguchi. Comparison of Electrical Performance of Co-Integrated Forksheets and Nanosheets Transistors for the 2nm Technological Node and Beyond. In *2021 IEEE International Electron Devices Meeting (IEDM)*. IEEE, dec 2021. doi: 10.1109/iedm19574.2021.9720524.

[18] Xuefeng Gu. *Charge-trap transistors for neuromorphic computing*. University of California, Los Angeles, 2018.

[19] Faraz Khan. *Charge Trap Transistors (CTT): Turning Logic Transistors into Embedded Non-Volatile Memory for Advanced High-k/Metal Gate CMOS Technologies*. University of California, Los Angeles, 2020.

[20] Xuefeng Gu and Subramanian S. Iyer. Unsupervised Learning Using Charge-Trap Transistors. *IEEE Electron Device Letters*, 38(9):1204–1207, sep 2017. doi: 10.1109/led.2017.2723319.

[21] Yuan Du, Li Du, Xuefeng Gu, Jieqiong Du, X. Shawn Wang, Boyu Hu, Mingzhe Jiang, Xiaoliang Chen, Subramanian S. Iyer, and Mau-Chung Frank Chang. An Analog Neural Network Computing Engine Using CMOS-Compatible Charge-Trap-Transistor (CTT). *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 38(10):1811–1819, oct 2019. doi: 10.1109/tcad.2018.2859237.

[22] Xuefeng Gu, Zhe Wan, and Subramanian S. Iyer. Charge-Trap Transistors for CMOS-Only Analog Memory. *IEEE Transactions on Electron Devices*, 66(10): 4183–4187, oct 2019. doi: 10.1109/ted.2019.2933484.

[23] Faraz Khan, Eduard Cartier, Jason C. S. Woo, and Subramanian S. Iyer. Charge trap transistor (CTT): An embedded fully logic-compatible multiple-time programmable non-volatile memory element for high- k -metal-gate CMOS technologies. *IEEE Electron Device Letters*, 38(1):44–47, jan 2017. doi: 10.1109/led.2016.2633490.

[24] Rachel M. Brewer, En Xia Zhang, Mariia Gorchichko, Peng Fei Wang, Jonathan Cox, Steven L. Moran, Dennis R. Ball, Brian D. Sierawski, Daniel M. Fleetwood,

Ronald D. Schrimpf, Subramanian S. Iyer, and Michael L. Alles. Total Ionizing Dose Responses of 22-nm FDSOI and 14-nm Bulk FinFET Charge-Trap Transistors. *IEEE Transactions on Nuclear Science*, 68(5):677–686, may 2021. doi: 10.1109/tns.2021.3059594.

[25] International Roadmap for Devices and Systems. More moore. https://irds.ieee.org/editions/2023/more-moore, 2023. [Online; accessed 15-January-2023].

[26] Danijela Marković, Alice Mizrahi, Damien Querlioz, and Julie Grollier. Physics for neuromorphic computing. *Nature Reviews Physics*, 2(9):499–510, 2020. doi: 10.1038/s42254-020-0208-2.

[27] Mohammed A Zidan, John Paul Strachan, and Wei D Lu. The future of electronics based on memristive systems. *Nature electronics*, 1(1):22–29, 2018. doi: 10.1038/s41928-017-0006-8.

[28] Jason K Eshraghian, Xinxin Wang, and Wei D Lu. Memristor-based binarized spiking neural networks: Challenges and applications. *IEEE Nanotechnology Magazine*, 16(2):14–23, 2022. doi: 10.1109/mnano.2022.3141443.

[29] Doyoung Jang, Dmitry Yakimets, Geert Eneman, Pieter Schuddinck, Marie Garcia Bardon, Praveen Raghavan, Alessio Spessot, Diederik Verkest, and Anda Mocuta. Device exploration of NanoSheet transistors for sub-7-nm technology node. *IEEE Transactions on Electron Devices*, 64(6):2707–2713, 2017. doi: 10.1109/ted.2017.2695455.

[30] Daniel Nagy, Gabriel Espineira, Guillermo Indalecio, Antonio J Garcia-Loureiro, Karol Kalna, and Natalia Seoane. Benchmarking of FinFET, nanosheet, and nanowire FET architectures for future technology nodes. *IEEE Access*, 8: 53196–53202, 2020. doi: 10.1109/access.2020.2980925.

[31] Giuliano Sisto, Odysseas Zografos, Bilal Chehab, Naveen Kakarla, Yang Xiang, Dragomir Milojevic, Pieter Weckx, Geert Hellings, and Julien Ryckaert. Evaluation of Nanosheet and Forksheet Width Modulation for Digital IC Design in the Sub-3 nm Era. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pages 1–10, 2022. doi: 10.1109/tvlsi.2022.3190080.

[32] P. Weckx, J. Ryckaert, V. Putcha, A. De Keersgieter, J. Boemmels, P. Schuddinck, D. Jang, D. Yakimets, M. G. Bardon, L.-A. Ragnarsson, P. Raghavan, R. R. Kim,

A. Spessot, D. Verkest, and A. Mocuta. Stacked nanosheet fork architecture for SRAM design and device co-optimization toward 3nm. In *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, dec 2017. doi: 10.1109/iedm.2017.8268430.

[33] Hsiao-Hsuan Liu, Pieter Schuddinck, Zhenlin Pei, Lynn Verschueren, Hans Mertens, Shairfe M. Salahuddin, Gaspard Hiblot, Yang Xiang, Boon Teik Chan, Sujith Subramanian, Pieter Weckx, Geert Hellings, Marie Garcia Bardon, Julien Ryckaert, Chenyun Pan, and Francky Catthoor. CFET SRAM With Double-Sided Interconnect Design and DTCO Benchmark. *IEEE Transactions on Electron Devices*, 70(10):5099–5106, October 2023. ISSN 1557-9646. doi: 10.1109/ted.2023.3305322.

[34] Hsiao-Hsuan Liu, Shairfe M. Salahuddin, Boon Teik Chan, Pieter Schuddinck, Yang Xiang, Geert Hellings, Pieter Weckx, Julien Ryckaert, and Francky Catthoor. CFET SRAM DTCO, Interconnect Guideline, and Benchmark for CMOS Scaling. *IEEE Transactions on Electron Devices*, 70(3):883–890, March 2023. ISSN 1557-9646. doi: 10.1109/ted.2023.3235701.

[35] S.-W. Chang, J.-H. Li, M.-K. Huang, Y.-C. Huang, S.-T. Huang, H.-C. Wang, Y.-J. Huang, J.-Y. Wang, L. W Yu, Y.-F. Huang, F. K. Hsueh, P.-J. Sung, C.-T. Wu, W. C.-Y. Ma, K.-H. Kao, Y. J. Lee, C.-L. Lin, R. W. Chuang, K.-P. Huang, S. Samukawa, Y. Li, W. H. Lee, T-Y. Chu, T.-S. Chao, G. W. Huang, W.-F. Wu, J. Y. Li, J.-M. Shieh, W. K. Yeh, Y.-H. Wang, D. D. Lu, C.-J. Wang, N.-C. Lin, C.-J. Su, S.-H. Lo, and H.-F. Huang. First Demonstration of CMOS Inverter and 6T-SRAM Based on GAA CFETs Structure for 3D-IC Applications. In *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, dec 2019. doi: 10.1109/iedm19573.2019.8993525.

[36] Julien Ryckaert, Pieter Weckx, and Shairfe Muhammad Salahuddin. *SRAM technology status and perspectives*, page 55–86. Elsevier, 2022. ISBN 9780128207581. doi: 10.1016/b978-0-12-820758-1.00010-8.

[37] P. Schuddinck, F. M. Bufler, Y. Xiang, A. Farokhnejad, G. Mirabelli, A. Vandooren, B. Chehab, A. Gupta, C. Roda Neve, G. Hellings, and J. Ryckaert. PPAC of sheet-based CFET configurations for 4 track design with 16nm metal pitch. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, June 2022. doi: 10.1109/vlsitechnologyandcir46769.2022.9830492.

[38] P. Schuddinck, O. Zografos, P. Weckx, P. Matagne, S. Sarkar, Y. Sherazi, R. Baert, D. Jang, D. Yakimets, A. Gupta, B. Parvais, J. Ryckaert, D. Verkest, and A. Mocuta. Device-, Circuit− &; Block-level evaluation of CFET in a 4 track library. In *2019 Symposium on VLSI Technology*. IEEE, June 2019. doi: 10.23919/vlsit.2019.8776513.

[39] C. Y. Huang, G. Dewey, E. Mannebach, A. Phan, P. Morrow, W. Rachmady, I. C. Tung, N. Thomas, U. Alaan, R. Paul, N. Kabir, B. Krist, A. Oni, M. Mehta, M. Harper, P. Nguyen, R. Keech, S. Vishwanath, K. L. Cheong, J. S. Kang, A. Lilak, M. Metz, S. Clendenning, B. Turkot, R. Schenker, H. J. Yoo, M. Radosavljevic, and J. Kavalieros. 3-D Self-aligned Stacked NMOS-on-PMOS Nanoribbon Transistors for Continued Moore's Law Scaling. In *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE, dec 2020. doi: 10.1109/iedm13553.2020.9372066.

[40] Xiaona Zhu, Rongzheng Ding, Ouwen Tao, Yage Zhao, Peishun Tang, David Wei Zhang, Ye Lu, and Shaofeng Yu. A combined N/PFET CFET based design and logic technology framework for CMOS applications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2023. doi: 10.1109/tcad.2023.3282576.

[41] Junjong Lee, Jun-Sik Yoon, Jaewan Lim, and Rock-Hyun Baek. Electrical Coupling Effect of Forksheet FET for Power, Performance, and Area Analysis. *IEEE Transactions on Electron Devices*, 69(12):7096–7101, December 2022. ISSN 1557-9646. doi: 10.1109/ted.2022.3215657.

[42] Chung-Kuan Cheng, Chia-Tung Ho, Daeyeal Lee, and Bill Lin. Multirow Complementary-FET (CFET) Standard Cell Synthesis Framework Using Satisfiability Modulo Theories (SMTs). *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, 7(1):43–51, June 2021. ISSN 2329-9231. doi: 10.1109/jxcdc.2021.3092769.

[43] Md. Hasan Raza Ansari, Nupur Navlakha, and Nazek El-Atab. Engineered vertically stacked nsfet charge-trapping synapse for neuromorphic applications. *ACS Applied Electronic Materials*, December 2023. ISSN 2637-6113. doi: 10.1021/acsaelm.3c01420.

[44] Md. Hasan Raza Ansari, Seongjae Cho, Jong-Ho Lee, and Byung-Gook Park. Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic

Application. *IEEE Journal of the Electron Devices Society*, 9:1282–1289, 2021. doi: 10.1109/jeds.2021.3111343.

[45] Pai-Yu Chen, Xiaochen Peng, and g Yu. Neurosim+: An integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures. In *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, December 2017. doi: 10.1109/iedm.2017.8268337.

[46] Jun-Sik Yoon, Jinsu Jeong, Seunghwan Lee, and Rock-Hyun Baek. Systematic DC/AC performance benchmarking of sub-7-nm node FinFETs and nanosheet FETs. *IEEE Journal of the Electron Devices Society*, 6:942–947, 2018. doi: 10.1109/jeds.2018.2866026.

[47] Vikram Passi and Jean-Pierre Raskin. Review on analog/radio frequency performance of advanced silicon MOSFETs. *Semiconductor Science and Technology*, 32(12):123004, 2017. doi: 10.1088/1361-6641/aa9145.

[48] A Veloso, T Huynh-Bao, P Matagne, D Jang, G Eneman, N Horiguchi, and J Ryckaert. Nanowire & nanosheet FETs for ultra-scaled, high-density logic and memory applications. *Solid-State Electronics*, 168:107736, 2020. doi: 10.1016/j.sse.2019.107736.

[49] Jagar Singh, Jerome Ciavatti, Kumaran Sundaram, Jen Shuang Wong, Anirban Bandyopadhyay, Xiaoqiang Zhang, Shuang Li, Abdellatif Bellaouar, Josef Watts, Joseph G Lee, et al. 14-nm FinFET technology for analog and RF applications. *IEEE Transactions on electron devices*, 65(1):31–37, 2017. doi: 10.1109/ted.2017.2776838.

[50] Jiabi Zhang, Guofu Niu, Will Cai, Weike Wang, and Kimihiko Imura. Intermodulation linearity characteristics of 14-nm RF FinFETs. *IEEE Transactions on Electron Devices*, 66(6):2520–2526, 2019. doi: 10.1109/ted.2019.2912516.

[51] Jun-Sik Yoon and Rock-Hyun Baek. Device design guideline of 5-nm-node FinFETs and nanosheet FETs for analog/RF applications. *IEEE Access*, 8:189395–189403, 2020. doi: 10.1109/access.2020.3031870.

[52] Ke Han, Yannan Zhang, and Zhongliang Deng. A simulation study of gate-all-around nanowire transistor with a core-substrate. *IEEE Access*, 8:62181–62190, 2020. doi: 10.1109/access.2020.2983724.

[53] Pragya Kushwaha, Avirup Dasgupta, Ming-Yen Kao, Harshit Agarwal, Sayeef Salahuddin, and Chenming Hu. Design optimization techniques in nanosheet transistor for RF applications. *IEEE Transactions on Electron Devices*, 67(10): 4515–4520, 2020. doi: 10.1109/ted.2020.3019022.

[54] Hsin-Cheng Lin, Tao Chou, Chia-Che Chung, Chia-Jung Tsen, Bo-Wei Huang, and CW Liu. RF performance of stacked Si nanosheet nFETs. *IEEE Transactions on Electron Devices*, 68(10):5277–5283, 2021. doi: 10.1109/ted.2021.3106287.

[55] Leland Chang, Meikei Ieong, and Min Yang. CMOS circuit performance enhancement by surface orientation optimization. *IEEE Transactions on Electron Devices*, 51(10):1621–1627, 2004. doi: 10.1007/978-3-7091-0624-2$_$14.

[56] International Roadmap for Devices and Systems. More moore. https://irds.ieee.org/editions/2020/more-moore, 2020. [Online; accessed 15-January-2021].

[57] International Technology Roadmap for Semiconductors. Process integration, devices and structures. http://www.itrs2.net/2013-itrs.html, 2013. [Online; accessed 15-December-2020].

[58] C. Auth, A. Aliyarukunju, M. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik, M. Buehler, V. Chikarmane, G. Ding, Q. Fu, H. Gomez, W. Han, D. Hanken, M. Haran, M. Hattendorf, R. Heussner, H. Hiramatsu, B. Ho, S. Jaloviar, I. Jin, S. Joshi, S. Kirby, S. Kosaraju, H. Kothari, G. Leatherman, K. Lee, J. Leib, A. Madhavan, K. Marla, H. Meyer, T. Mule, C. Parker, S. Parthasarathy, C. Pelto, L. Pipes, I. Post, M. Prince, A. Rahman, S. Rajamani, A. Saha, J. Dacuna Santos, M. Sharma, V. Sharma, J. Shin, P. Sinha, P. Smith, M. Sprinkle, A. St. Amour, C. Staus, R. Suri, D. Towner, A. Tripathi, A. Tura, C. Ward, and A. Yeoh. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects. In *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, dec 2017. doi: 10.1109/iedm.2017.8268472.

[59] Vaibhav Rana, Gufran Ahmad, Akhil K Ramesh, Samaresh Das, and Pushpapraj Singh. Diameter-Dependent Piezoresistive Sensing Performance of Junctionless Gate-All-Around Nanowire FET. *IEEE Transactions on Electron Devices*, 67(7): 2884–2889, 2020. doi: 10.1109/ted.2020.2991140.

[60] Wen Liu, Juin J Liou, Y Jiang, N Singh, GQ Lo, J Chung, and YH Jeong. Investigation of Sub-10-nm Diameter, Gate-All-Around Nanowire Field-Effect Transistors for Electrostatic Discharge Applications. *IEEE Transactions on Nanotechnology*, 9(3):352–354, 2010. doi: 10.1109/tnano.2009.2038225.

[61] Synopsys Inc. Mountain View, CA, USA, Version O-2018.06, 2019.

[62] Sungman Rhee, Daewon Kim, Kyeongyeon Kim, Seongwook Choi, Byung-Gook Park, and Young June Park. Extension of the Density-Gradient Model to the Second-Order Quantum Correction for Analysis of the Single-Charge Effect in Sub-10-nm MOS Devices. *IEEE Journal of the Electron Devices Society*, pages 1–1, 2020. doi: 10.1109/jeds.2020.2971426.

[63] D.B.M.Klaassen, J.W.Slotboom, and H.C.de Graaff. Unified apparent bandgap narrowing in n- and p-type silicon. *Microelectronics Reliability*, 32(12):1797, dec 1992. doi: 10.1016/0026-2714(92)90401-6.

[64] John Bardeen. Surface states and rectification at a metal semi-conductor contact. *Physical Review*, 71(10):717, 1947. doi: 10.1016/b978-0-08-006511-3.50009-x.

[65] Brajesh Rawat. *Numerical modeling and analysis of graphene-based field-effect transistors*. PhD thesis, 2017.

[66] Hidenori Yamada and Prabhakar R Bandaru. Enhanced electrical current densities in electrochemical systems through the use of nanostructured electrodes. *Applied Physics Letters*, 104(21):213901, 2014. doi: 10.1063/1.4879837.

[67] Vanessa CP Silva, Welder F Perina, Joao A Martino, Eddy Simoen, Anabela Veloso, and Paula GD Agopian. Analog Figures of Merit of Vertically Stacked Silicon Nanosheets nMOSFETs With Two Different Metal Gates for the Sub-7 nm Technology Node Operating at High Temperatures. *IEEE Transactions on Electron Devices*, 2021. doi: 10.1109/ted.2021.3077349.

[68] Isabelle Ferain, Cynthia A Colinge, and Jean-Pierre Colinge. Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature*, 479(7373):310–316, 2011. doi: 10.1038/nature10676.

[69] Hidenori Yamada and Prabhakar R Bandaru. Limits to the magnitude of capacitance in carbon nanotube array electrode based electrochemical capacitors. *Applied Physics Letters*, 102(17):173113, 2013. doi: 10.1063/1.4803925.

[70] Jiaxin Yao, Jun Li, Kun Luo, Jiahan Yu, Qingzhu Zhang, Zhaozhao Hou, Jie Gu, Wen Yang, Zhenhua Wu, Huaxiang Yin, et al. Physical insights on quantum confinement and carrier mobility in Si, Si 0.45 Ge 0.55, Ge gate-all-around NSFET for 5 nm technology node. *IEEE Journal of the Electron Devices Society*, 6:841–848, 2018. doi: 10.1109/jeds.2018.2858225.

[71] Pedram Razavi, Giorgos Fagas, Isabelle Ferain, Ran Yu, Samaresh Das, and Jean-Pierre Colinge. Influence of channel material properties on performance of nanowire transistors. *Journal of Applied Physics*, 111(12):124509, 2012. doi: 10.1063/1.4729777.

[72] Mohit Kumar Gupta, Pieter Weckx, Pieter Schuddinck, Doyoung Jang, Bilal Chehab, Stefan Cosemans, Julien Ryckaert, and Wim Dehaene. A Comprehensive Study of Nanosheet and Forksheet SRAM for Beyond N5 Node. *IEEE Transactions on Electron Devices*, 68(8):3819–3825, August 2021. ISSN 1557-9646. doi: 10.1109/ted.2021.3088392.

[73] Dongwon Jang, Seung-Geun Jung, Seong-Ji Min, and Hyun-Yong Yu. Electrothermal Characterization and Optimization of Monolithic 3D Complementary FET (CFET). *IEEE Access*, 9:158116–158121, 2021. doi: 10.1109/access.2021.3130654.

[74] Xiaoqiao Yang, Yabin Sun, Ziyu Liu, Yanling Shi, and Xiaojin Li. Performance Trade-offs in Complementary FET (CFET) Device Architectures for 3nm-node and Beyond. In *2021 5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, page 1–3. IEEE, April 2021. doi: 10.1109/edtm50988.2021.9420820.

[75] Jung, Seung-Geun and Jang, Dongwon and Min, Seong-Ji and Park, Euyjin and Yu, Hyun-Yong. Device design guidelines of 3-nm node complementary FET (CFET) in perspective of electrothermal characteristics. *IEEE Access*, 10:41112–41118, 2022. doi: 10.1109/access.2022.3166934.

[76] Natalia Seoane, Julian G Fernandez, Karol Kalna, Enrique Comesana, and Antonio Garcia-Loureiro. Simulations of statistical variability in n-type FinFET, nanowire, and nanosheet FETs. *IEEE Electron Device Letters*, 42(10):1416–1419, 2021. doi: 10.1109/led.2021.3109586.

[77] Xiaoqiao Yang, Xianglong Li, Ziyu Liu, Yabin Sun, Yun Liu, Xiaojin Li, and Yanling Shi. Impact of process variation on nanosheet gate-all-around complementary FET

(CFET). *IEEE Transactions on Electron Devices*, 69(7):4029–4036, 2022. doi: 10.1109/ted.2022.3176835.

[78] Akhilesh Rawat and Brajesh Rawat. Multichannel Two-Dimensional MoS2 Nanosheet MOSFET for Future Technology Node. *IEEE Transactions on Electron Devices*, 2024. doi: 10.1109/ted.2024.3384136.

[79] International Roadmap for Devices and Systems. MORE MOORE. https://irds.ieee.org/editions/2021/more-moore, 2021.

[80] Yanna Luo, Qingzhu Zhang, Lei Cao, Weizhuo Gan, Haoqing Xu, Yu Cao, Jie Gu, Renren Xu, Gangping Yan, Jiali Huo, Zhenhua Wu, and Huaxiang Yin. Investigation of Novel Hybrid Channel Complementary FET Scaling Beyond 3-nm Node From Device to Circuit. *IEEE Transactions on Electron Devices*, 69(7):3581–3588, jul 2022. doi: 10.1109/ted.2022.3176843.

[81] Xiaoqiao Yang, Xianglong Li, Ziyu Liu, Yabin Sun, Yun Liu, Xiaojin Li, and Yanling Shi. Impact of Process Variation on Nanosheet Gate-All-Around Complementary FET (CFET). *IEEE Transactions on Electron Devices*, 69(7):4029–4036, jul 2022. doi: 10.1109/ted.2022.3176835.

[82] Peng Zheng, Daniel Connelly, Fei Ding, and Tsu-Jae King Liu. FinFET Evolution Toward Stacked-Nanowire FET for CMOS Technology Scaling. *IEEE Transactions on Electron Devices*, 62(12):3945–3950, dec 2015. doi: 10.1109/ted.2015.2487367.

[83] Hans Mertens, Romain Ritzenthaler, Yusuke Oniki, Basoene Briggs, BT Chan, Andriy Hikavyy, Toby Hopf, Geert Mannaert, Zheng Tao, Farid Sebaai, et al. Forksheet FETs for Advanced CMOS Scaling: Forksheet-Nanosheet Co-Integration and Dual Work Function Metal Gates at 17nm NP Space. In *2021 Symposium on VLSI Technology*, pages 1–2. IEEE, 2021.

[84] B. Vincent, J. Boemmels, J. Ryckaert, and J. Ervin. A Benchmark Study of Complementary-Field Effect Transistor (CFET) Process Integration Options Done by Virtual Fabrication. *IEEE Journal of the Electron Devices Society*, 8:668–673, 2020. doi: 10.1109/jeds.2020.2990718.

[85] Anjali Goel, Akhilesh Rawat, and Brajesh Rawat. Benchmarking of Analog/RF Performance of Fin-FET, NW-FET, and NS-FET in the Ultimate Scaling Limit. *IEEE Transactions on Electron Devices*, 69(3):1298–1305, mar 2022. doi: 10.1109/ted.2021.3140158.

[86] Md Obaidul Hossen, Bharani Chava, Geert Van der Plas, Eric Beyne, and Muhannad S. Bakir. Power Delivery Network (PDN) Modeling for Backside-PDN Configurations With Buried Power Rails and μ TSVs. *IEEE Transactions on Electron Devices*, 67(1):11–17, January 2020. ISSN 1557-9646. doi: 10.1109/ted.2019.2954301.

[87] Scott R Stiffler, Ravikumar Ramachandran, W Kirklen Henson, ND Zamdmer, Kevin McStay, Giuseppe La Rosa, Kevin M Boyd, Sungjae Lee, Claude Ortolland, and Paul C Parries. Process technology for IBM 14-nm processor designs featuring silicon-on-insulator FinFETs. *IBM Journal of Research and Development*, 62(2/3): 11–1, 2018.

[88] Aoxiang Tang and Niraj K Jha. Design space exploration of FinFET cache. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 9(3):1–16, 2013. doi: 10.1145/2491678.

[89] See-On Park, Hakcheon Jeong, Jongyong Park, Jongmin Bae, and Shinhyun Choi. Experimental demonstration of highly reliable dynamic memristor for artificial neuron and neuromorphic computing. *Nature Communications*, 13(1), June 2022. ISSN 2041-1723. doi: 10.1038/s41467-022-30539-6.

[90] Mohit Kumar Gupta, Pieter Weckx, Pieter Schuddinck, Doyoung Jang, Bilal Chehab, Stefan Cosemans, Julien Ryckaert, and Wim Dehaene. The Complementary FET (CFET) 6T-SRAM. *IEEE Transactions on Electron Devices*, 68(12):6106–6111, December 2021. ISSN 1557-9646. doi: 10.1109/ted.2021.3121349.

[91] Jan M Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. *Digital integrated circuits*, volume 2. Prentice hall Englewood Cliffs, 2002.

[92] Jim Esch. Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking. *Proceedings of the IEEE*, 101(12):2495–2497, dec 2013. doi: 10.1109/jproc.2013.2286655.

[93] Dmitri E. Nikonov and Ian A. Young. Uniform methodology for benchmarking beyond-CMOS logic devices. In *2012 IEEE International Electron Devices Meeting (IEDM)*, pages 25.4.1–25.4.4. IEEE, 2012. doi: 10.1109/iedm.2012.6479102.

[94] A. Mehonic and A. J. Kenyon. Brain-inspired computing needs a master plan. *Nature*, 604(7905):255–260, April 2022. ISSN 1476-4687. doi: 10.1038/s41586-021-04362-w.

[95] Jiyong Woo, Kibong Moon, Jeonghwan Song, Sangheon Lee, Myounghun Kwak, Jaesung Park, and Hyunsang Hwang. Improved Synaptic Behavior Under Identical Pulses Using AlO_x/HfO_2 Bilayer RRAM Array for Neuromorphic Systems. *IEEE Electron Device Letters*, 37(8):994–997, August 2016. ISSN 1558-0563. doi: 10.1109/led.2016.2582859.

[96] Bin Tang, Sabir Hussain, Rui Xu, Zhihai Cheng, Jianhui Liao, and Qing Chen. Novel Type of Synaptic Transistors Based on a Ferroelectric Semiconductor Channel. *ACS Appl. Mater. Interfaces*, 12(22):24920–24928, May 2020. ISSN 1944-8252. doi: 10.1021/acsami.9b23595.

[97] Gopalakrishnan Srinivasan, Abhronil Sengupta, and Kaushik Roy. Magnetic Tunnel Junction Based Long-Term Short-Term Stochastic Synapse for a Spiking Neural Network with On-Chip STDP Learning. *Scientific Reports*, 6(1), July 2016. ISSN 2045-2322. doi: 10.1038/srep29545.

[98] Faraz Khan, Eduard Cartier, Chandrasekara Kothandaraman, J. Campbell Scott, Jason C. S. Woo, and Subramanian S. Iyer. The Impact of Self-Heating on Charge Trapping in High-k-Metal-Gate nFETs. *IEEE Electron Device Letters*, 37(1):88–91, jan 2016. doi: 10.1109/led.2015.2504952.

[99] E. Gnani, S. Reggiani, A. Gnudi, G. Baccarani, J. Fu, N. Singh, G.Q. Lo, and D.L. Kwong. Modeling of nonvolatile gate-all-around charge-trapping SONOS memory cells. In *2009 Proceedings of the European Solid State Device Research Conference*. IEEE, September 2009. doi: 10.1109/essderc.2009.5331609. doi: 10.1109/essderc.2009.5331609.

[100] Md. Hasan Raza Ansari, Hanrui Li, and Nazek El-Atab. Vertically Stacked Nanosheet FET: Charge- Trapping Memory and Synapse With Linear Weight Adjustability for Neuromorphic Computing Applications. *IEEE Transactions on Electron Devices*, 70(3):1344–1350, March 2023. ISSN 1557-9646. doi: 10.1109/ted.2023.3234018.

[101] Abhash Kumar, Alok Kumar Kamal, Jawar Singh, and Bharat Gupta. Ultra Low Energy Charge Trapping MOSFET With Neuro-Inspired Learning Capabilities. *IEEE Transactions on Nanotechnology*, 22:266–272, 2023. ISSN 1941-0085. doi: 10.1109/tnano.2023.3283987.

[102] International Roadmap for Devices and Systems. More moore. https://irds.ieee.org/editions/2022/more-moore, 2022. [Online; accessed 15-January-2022].

[103] Faraz Khan, Min Soo Han, Dan Moy, Robert Katz, Liu Jiang, Edmund Banghart, Norman Robson, Toshiaki Kirihata, Jason C. S. Woo, and Subramanian S. Iyer. Design Optimization and Modeling of Charge Trap Transistors (CTTs) in 14 nm FinFET Technologies. *IEEE Electron Device Letters*, 40(7):1100–1103, jul 2019. doi: 10.1109/led.2019.2919871.

[104] F. Cerbu, O. Madia, D. V. Andreev, S. Fadida, M. Eizenberg, L. Breuil, J. G. Lisoni, J. A. Kittl, J. Strand, A. L. Shluger, V. V. Afanas'ev, M. Houssa, and A. Stesmans. Intrinsic electron traps in atomic-layer deposited HfO_2 insulators. *Applied Physics Letters*, 108(22), May 2016. ISSN 1077-3118. doi: 10.1063/1.4952718.

[105] Shi-Jie Li, Bo-Yi Dong, Biao Wang, Yi Li, Hua-Jun Sun, Yu-Hui He, Nuo Xu, and Xiang-Shui Miao. Alleviating Conductance Nonlinearity via Pulse Shape Designs in TaO_x Memristive Synapses. *IEEE Transactions on Electron Devices*, 66(1):810–813, January 2019. doi: 10.1109/ted.2018.2876065.

[106] Jean-Pierre Colinge and James C. Greer. *Nanowire Transistors*, page 18–53. Cambridge University Press, January 2016. doi: 10.1017/cbo9781107280779.003.

[107] Ram S. Yadav, Pankhuri Gupta, Amod Holla, Kacho Imtiyaz Ali Khan, Pranaba K. Muduli, and Debanjan Bhowmik. Demonstration of synaptic behavior in a heavy-metal-ferromagnetic-metal-oxide-heterostructure-based spintronic device for on-chip learning in crossbar-array-based neural networks. *ACS Applied Electronic Materials*, 5(1):484–497, January 2023. ISSN 2637-6113. doi: 10.1021/acsaelm.2c01488.

[108] Manan Suri, Olivier Bichler, Damien Querlioz, Olga Cueto, Luca Perniola, Veronique Sousa, Dominique Vuillaume, Christian Gamrat, and Barbara DeSalvo. Phase change memory as synapse for ultra-dense neuromorphic systems: Application to complex visual pattern extraction. In *2011 International Electron Devices Meeting*. IEEE, December 2011. doi: 10.1109/iedm.2011.6131488.

[109] Minjae Kim, Dong-eun Kim, Yue Wang, Donghyun Lee, Dong-Hyeok Lim, Haryeong Choi, Ioannis Kymissis, J. Joshua Yang, Joonki Suh, Hong-Sub Lee, and Hyung-Ho Park. Forming-less flexible memristor crossbar array for neuromorphic computing applications produced using low-temperature atomic layer deposition. *Applied*

Materials Today, 38:102204, June 2024. ISSN 2352-9407. doi: 10.1016/j.apmt.2024.102204.

[110] Eunseon Yu, Seongjae Cho, Kaushik Roy, and Byung-Gook Park. A Quantum-Well Charge-Trap Synaptic Transistor With Highly Linear Weight Tunability. *IEEE Journal of the Electron Devices Society*, 8:834–840, 2020. ISSN 2168-6734. doi: 10.1109/jeds.2020.3011409.

[111] Min Zhang, Zehui Fan, Xixi Jiang, Hao Zhu, Lin Chen, Yidong Xia, Jiang Yin, Xinke Liu, Qingqing Sun, and David Wei Zhang. MoS_2-based Charge-trapping synaptic device with electrical and optical modulated conductance. *Nanophotonics*, 9(8): 2475–2486, February 2020. ISSN 2192-8606. doi: 10.1515/nanoph-2019-0548.

[112] Neha Kamal, Jawar Singh, Avinash Lahgere, and Pramod Kumar Tiwari. Ultra-Low Power Reconfigurable Synaptic and Neuronal Transistor for Spiking Neural Network. *IEEE Transactions on Nanotechnology*, 22:245–251, 2023. ISSN 1941-0085. doi: 10.1109/tnano.2023.3273624.

[113] Zhongrui Wang, Saumil Joshi, Sergey Savel'ev, Wenhao Song, Rivu Midya, Yunning Li, Mingyi Rao, Peng Yan, Shiva Asapu, Ye Zhuo, Hao Jiang, Peng Lin, Can Li, Jung Ho Yoon, Navnidhi K. Upadhyay, Jiaming Zhang, Miao Hu, John Paul Strachan, Mark Barnell, Qing Wu, Huaqiang Wu, R. Stanley Williams, Qiangfei Xia, and J. Joshua Yang. Fully memristive neural networks for pattern classification with unsupervised learning. *Nature Electronics*, 1(2):137–145,, February 2018. ISSN 2520-1131. doi: 10.1038/s41928-018-0023-2.

[114] H Matthies. Long-term synaptic potentiation and macromolecular changes in memory formation. In *Synaptic Plasticity in the Hippocampus*, pages 119–121. Springer, 1988. doi: 10.1007/978-3-642-73202-7_35.

[115] Joon-Kyu Han, Jungyeop Oh, Gyeong-Jun Yun, Dongeun Yoo, Myung-Su Kim, Ji-Man Yu, Sung-Yool Choi, and Yang-Kyu Choi. Cointegration of single-transistor neurons and synapses by nanoscale cmos fabrication for highly scalable neuromorphic hardware. *Science Advances*, 7(32), August 2021. ISSN 2375-2548. doi: 10.1126/sciadv.abg8836.

[116] Xiaojian Zhu, Qiwen Wang, and Wei D. Lu. Memristor networks for real-time neural activity analysis. *Nature Communications*, 11(1), May 2020. ISSN 2041-1723. doi: 10.1038/s41467-020-16261-1.

[117] Mani Shankar Yadav, Kanupriya Varshney, and Brajesh Rawat. Memory switching versus threshold memory switching: Finding a promising synaptic device for brain-inspired artificial learning systems. *ACS Applied Engineering Materials*, 2 (8):2131–2142, July 2024. ISSN 2771-9545. doi: 10.1021/acsaenm.4c00307.

[118] Yoeri van de Burgt, Ewout Lubberman, Elliot J. Fuller, Scott T. Keene, Grégorio C. Faria, Sapan Agarwal, Matthew J. Marinella, A. Alec Talin, and Alberto Salleo. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nature Materials*, 16(4):414–418, February 2017. ISSN 1476-4660. doi: 10.1038/nmat4856.

[119] Giacomo Indiveri, Bernabé Linares-Barranco, Tara Julia Hamilton, André van Schaik, Ralph Etienne-Cummings, Tobi Delbruck, Shih-Chii Liu, Piotr Dudek, Philipp Häfliger, Sylvie Renaud, Johannes Schemmel, Gert Cauwenberghs, John Arthur, Kai Hynna, Fopefolu Folowosele, Sylvain Saighi, Teresa Serrano-Gotarredona, Jayawan Wijekoon, Yingxue Wang, and Kwabena Boahen. Neuromorphic silicon neuron circuits. *Frontiers in Neuroscience*, 5, 2011. ISSN 1662-4548. doi: 10.3389/fnins.2011.00073.

[120] Paul A. Merolla, John V. Arthur, Rodrigo Alvarez-Icaza, Andrew S. Cassidy, Jun Sawada, Filipp Akopyan, Bryan L. Jackson, Nabil Imam, Chen Guo, Yutaka Nakamura, Bernard Brezzo, Ivan Vo, Steven K. Esser, Rathinakumar Appuswamy, Brian Taba, Arnon Amir, Myron D. Flickner, William P. Risk, Rajit Manohar, and Dharmendra S. Modha. A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science*, 345(6197):668–673, August 2014. ISSN 1095-9203. doi: 10.1126/science.1254642.

[121] Chao Du, Fuxi Cai, Mohammed A. Zidan, Wen Ma, Seung Hwan Lee, and Wei D. Lu. Reservoir computing using dynamic memristors for temporal information processing. *Nature Communications*, 8(1), December 2017. ISSN 2041-1723. doi: 10.1038/s41467-017-02337-y.

[122] Mike Davies, Narayan Srinivasa, Tsung-Han Lin, Gautham Chinya, Yongqiang Cao, Sri Harsha Choday, Georgios Dimou, Prasad Joshi, Nabil Imam, Shweta Jain, Yuyun Liao, Chit-Kwan Lin, Andrew Lines, Ruokun Liu, Deepak Mathaikutty, Steven McCoy, Arnab Paul, Jonathan Tse, Guruguhanathan Venkataramanan, Yi-Hsin Weng, Andreas Wild, Yoonseok Yang, and Hong Wang. Loihi: A neuromorphic

manycore processor with on-chip learning. *IEEE Micro*, 38(1):82–99, January 2018. ISSN 1937-4143. doi: 10.1109/mm.2018.112130359.

[123] Hannah Bos and Dylan Muir. *Sub-mW Neuromorphic SNN Audio Processing Applications with Rockpool and Xylo*, page 69–78. River Publishers, March 2023. ISBN 9781003394440. doi: 10.1201/9781003394440-7.

[124] Yesheng Li and Kah-Wee Ang. Hardware implementation of neuromorphic computing using large-scale memristor crossbar arrays. *Advanced Intelligent Systems*, 3(1), November 2020. ISSN 2640-4567. doi: 10.1002/aisy.202000137.

[125] Ming-Hung Wu, Ming-Chun Hong, Chih-Cheng Chang, Paritosh Sahu, Jeng-Hua Wei, Heng-Yuan Lee, Shyh-Shyuan Shcu, and Tuo-Hung Hou. Extremely compact integrate-and-fire stt-mram neuron: A pathway toward all-spin artificial deep neural network. In *2019 Symposium on VLSI Technology*, volume i, page T34–T35. IEEE, June 2019. doi: 10.23919/vlsit.2019.8776569.

[126] Zheng Wang, Brian Crafton, Jorge Gomez, Ruijuan Xu, Aileen Luo, Zoran Krivokapic, Lane Martin, Suman Datta, Arijit Raychowdhury, and Asif Islam Khan. Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In *2018 IEEE International Electron Devices Meeting (IEDM)*, volume 345, pages 13.3.1–13.3.4. IEEE, December 2018. doi: 10.1109/iedm.2018.8614586.

[127] Xinxin Wang, Mohammed A. Zidan, and Wei D. Lu. A crossbar-based in-memory computing architecture. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(12):4224–4232, dec 2020. doi: 10.1109/tcsi.2020.3000468.

[128] Angeliki Pantazi, Stanisław Woźniak, Tomas Tuma, and Evangelos Eleftheriou. All-memristive neuromorphic computing with level-tuned neurons. *Nanotechnology*, 27(35):355205, July 2016. ISSN 1361-6528. doi: 10.1088/0957-4484/27/35/355205.

[129] Sangya Dutta, Vinay Kumar, Aditya Shukla, Nihar R. Mohapatra, and Udayan Ganguly. Leaky integrate and fire neuron by charge-discharge dynamics in floating-body mosfet. *Scientific Reports*, 7(1), August 2017. ISSN 2045-2322. doi: 10.1038/s41598-017-07418-y.

[130] Dibyendu Chatterjee and Anil Kottantharayil. A cmos compatible bulk finfet-based ultra low energy leaky integrate and fire neuron for spiking neural networks. *IEEE*

Electron Device Letters, 40(8):1301–1304, August 2019. ISSN 1558-0563. doi: 10.1109/led.2019.2924259.

[131] Anjali Goel, Md. Hasan Raza Ansari, Nazek El-Atab, and Brajesh Rawat. Unraveling the Dynamics of HfO_2-Based NW-CTT as an Artificial Synapse. *IEEE Transactions on Electron Devices*, page 1–8, 2024. ISSN 1557-9646. doi: 10.1109/ted.2024.3418726.

[132] Jeffrey Abbott, Tianyang Ye, Ling Qin, Marsela Jorgolli, Rona S. Gertner, Donhee Ham, and Hongkun Park. Cmos nanoelectrode array for all-electrical intracellular electrophysiological imaging. *Nature Nanotechnology*, 12(5):460–466, February 2017. ISSN 1748-3395. doi: 10.1038/nnano.2017.3.

[133] Peter B. Kruskal, Zhe Jiang, Teng Gao, and Charles M. Lieber. Beyond the patch clamp: Nanotechnologies for intracellular recording. *Neuron*, 86(1):21–24, April 2015. ISSN 0896-6273. doi: 10.1016/j.neuron.2015.01.004.

[134] Emery N Brown, Robert E Kass, and Partha P Mitra. Multiple neural spike train data analysis: state-of-the-art and future challenges. *Nature Neuroscience*, 7(5): 456–461, April 2004. ISSN 1546-1726. doi: 10.1038/nn1228.

[135] Fuxi Cai, Justin M. Correll, Seung Hwan Lee, Yong Lim, Vishishtha Bothra, Zhengya Zhang, Michael P. Flynn, and Wei D. Lu. A fully integrated reprogrammable memristor–cmos system for efficient multiply–accumulate operations. *Nature Electronics*, 2(7):290–299, July 2019. ISSN 2520-1131. doi: 10.1038/s41928-019-0270-x.

[136] Peng Lin, Can Li, Zhongrui Wang, Yunning Li, Hao Jiang, Wenhao Song, Mingyi Rao, Ye Zhuo, Navnidhi K. Upadhyay, Mark Barnell, Qing Wu, J. Joshua Yang, and Qiangfei Xia. Three-dimensional memristor circuits as complex neural networks. *Nature Electronics*, 3(4):225–232, April 2020. ISSN 2520-1131. doi: 10.1038/s41928-020-0397-9.

[137] G. Indiveri. A low-power adaptive integrate-and-fire neuron circuit. In *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03.*, volume 4 of *ISCAS-03*, pages IV–820–IV–823. IEEE. doi: 10.1109/iscas.2003.1206342.

[138] Anvesha Amravati, Saad Bin Nasir, Sivaram Thangadurai, Insik Yoon, and Arijit Raychowdhury. A 55nm time-domain mixed-signal neuromorphic accelerator

with stochastic synapses and embedded reinforcement learning for autonomous micro-robots. In *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. IEEE, February 2018. doi: 10.1109/isscc.2018.8310215.

[139] Yi-Ting Wu, Fei Ding, Daniel Connelly, Meng-Hsueh Chiang, Jone F. Chen, and Tsu-Jae King Liu. Simulation-based study of high-density SRAM voltage scaling enabled by inserted-oxide FinFET technology. *IEEE Transactions on Electron Devices*, 66(4):1754–1759, apr 2019. doi: 10.1109/ted.2019.2900921.

[140] M. Jerry, A. Parihar, B. Grisafe, A. Raychowdhury, and S. Datta. Ultra-low power probabilistic imt neurons for stochastic sampling machines. In *2017 Symposium on VLSI Technology*, page T186–T187. IEEE, June 2017. doi: 10.23919/vlsit.2017.7998148.

[141] B. Vermeersch, E. Bury, Y. Xiang, P. Schuddinck, K. K. Bhuwalka, G. Hellings, and J. Ryckaert. Self-heating in in8–in2 cmos logic cells: Thermal impact of architecture (finfet, nanosheet, forksheet and cfet) and scaling boosters. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, volume 101, page 371–372. IEEE, June 2022. doi: 10.1109/vlsitechnologyandcir46769.2022.9830228.

[142] Sunil Rathore, Navjeet Bagga, and S. Dasgupta. Self-heating and process-induced threshold voltage aware reliability and aging analysis of forksheet fet. In *2024 IEEE International Reliability Physics Symposium (IRPS)*, pages P65.TX–1–P65.TX–4. IEEE, April 2024. doi: 10.1109/irps48228.2024.10529473.

[143] Sunil Rathore, Sandeep Kumar, Mohd. Shakir, Navjeet Bagga, and S. Dasgupta. Unveiling the role of interface and dielectric wall traps with self-heating induced aging prediction of forksheet fet. In *2024 8th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, page 1–3. IEEE, March 2024. doi: 10.1109/edtm58488.2024.10511703.

[144] E. Bury, M. Vandemaele, J. Franco, A. Chasin, S. Tyaginov, A. Vandooren, R. Ritzenthaler, H. Mertens, J. Diaz Fortuny, N. Horiguchi, D. Linten, and B. Kaczer. Reliability challenges in forksheet devices: (invited paper). In *2023 IEEE International Reliability Physics Symposium (IRPS)*, volume 1 2, page 1–8. IEEE, March 2023. doi: 10.1109/irps48203.2023.10118269.

[145] Jami Venkata Suman, A. Swetha Priya, G. M. Anitha Priyadarshini, K. Krishnamraju, Akurathi Gangadhar, and Mamidipaka Hema. *Integration Challenges and Opportunities for Gate-All-Around FET (GAA FET) in Next-Generation Electronic Devices*, page 1361–1368. Atlantis Press International BV, 2024. ISBN 9789464634716. doi: 10.2991/978-94-6463-471-6_131.

[146] Rinku Rani Das, T. R. Rajalekshmi, and Alex James. Finfet to gaa mbcfet: A review and insights. *IEEE Access*, 12:50556–50577, 2024. ISSN 2169-3536. doi: 10.1109/access.2024.3384428.

List of Publications

Journals

1. **Anjali Goel**, Akhilesh Rawat, and Brajesh Rawat, "Benchmarking of Analog/RF Performance of Fin-FET, NW-FET, and NS-FET in the Ultimate Scaling Limit," ***IEEE Transactions on Electron Devices*** , vol. 69, no. 7, pp. 1298-1305, March 2022.

2. **Anjali Goel**, Md. Hasan Raza Ansari, Nazek-El Atab, and Brajesh Rawat, "Unraveling the Dynamics of HfO_2-based NW-CTT as an Artificial Synapse," ***IEEE Transactions on Electron Devices*** , vol. 71, no. 8, pp. 5125-5132, August 2024.

3. **Anjali Goel**, Akhilesh Rawat, and Brajesh Rawat, "Finding a Promising CMOS Inverter Architecture with Silicon Nanosheet for Future Technology Node," ***IEEE Transactions on Electron Devices*** , vol. 72, no. 4, pp. 1574-1581, April 2025.

4. **Anjali Goel**, and Brajesh Rawat, "Performance Benchmarking of CFET, FSH, and Stacked Nanosheet Inverters for SRAM and ALU in Future Technology Nodes," under revision in ***IEEE Transactions on Nanotechnology***.

5. Prajjwal Shukla, **Anjali Goel**, Vikas Kumar, Harneet Kaur, Vikas Kumar Malav, and Brajesh Rawat, "Design of Real-Time and Power-Efficient Flue Gas Monitoring System Using IoT Technology," under revision in ***IEEE Sensor Journal***. (All authors have equal contribution)

6. **Anjali Goel**, Mani Shankar Yadav, and Brajesh Rawat, " Energy efficient and Highly Scalable Fully NW-CTT based Spiking Neural Network," under preparation for the submission in ***IEEE Transactions on Electron Devices***.

7. **Anjali Goel**, and Brajesh Rawat, " iFinFET vs FinFET: The Optimal Choice for Future Technology Nodes?," under preparation for the submission in ***IEEE Transactions on Electron Devices***.

Conference Proceedings

1. **Anjali Goel**, Akhilesh Rawat, and Brajesh Rawat, "Finding Analog/RF Performance of Inserted High-K FinFET for Sub-5 nm Technology Node," *6th IEEE International Conference on Emerging Electronics (ICEE)*, Bengaluru, Dec. 2022.

2. **Anjali Goel**, Akhilesh Rawat, and Brajesh Rawat, "Performance Projection of Stacked Silicon Nanosheet-FET Architectures for Future Technology Node," *XXIst International Workshop on Physics of Semiconductor Devices: IWPSD*, Dec. 2021 (Online).

3. Akhilesh Rawat, **Anjali Goel**, and Brajesh Rawat, "Performance of Two-Dimensional MoS_2 Field-Effect Transistor in the Presence of Oxide-Channel Imperfection," *6th IEEE International Conference on Emerging Electronics (ICEE)*, Bengaluru, Dec. 2022. *(Published: Springer Nature Journal, 2023).*

4. Akhilesh Rawat, **Anjali Goel**, and Brajesh Rawat, " Role of Interface Trap Charges in the Performance of Monolayer and Bilayer MoS_2-based Field-Effect Transistors," *35th IEEE International Conference on VLSI Design*, March 2022 (Online).

List of Achievements

1. Received the prestigious Prime Minister Research Fellowship (PMRF) in 2022.

2. Our paper entitled “Finding Analog/RF Performance of Inserted High-K FinFET for Sub-5 nm Technology Node,” has been selected for the best poster prize at the 6th IEEE International Conference on Emerging Electronics (ICEE) in 2022.

3. Our work on “A Portable Flue Gas Analyzer Cum Air Quality Monitoring System“ has won the first prize at the Institute TECHNOLOGY DAY 2022, IIT Ropar.

4. Our work on “Electrochemical Sensor System for Comprehensive Air Quality Assessment“ has won the third prize and “Flue Gas Monitoring System“ has won the second prize at the RESEARCH SCHOLAR FORUM 2023, IIT Ropar.

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Research Interests:

- TCAD Modeling of multigate devices at advanced technology nodes.
- TCAD Modeling of charge trap devices.
- Circuit analysis of spiking neural network using charge trap transistors.